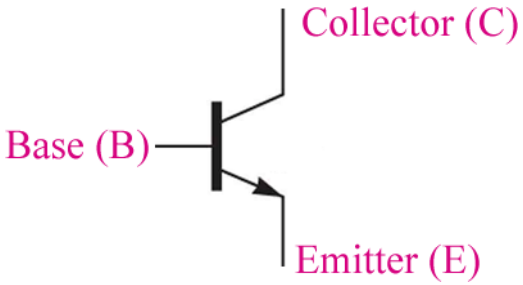
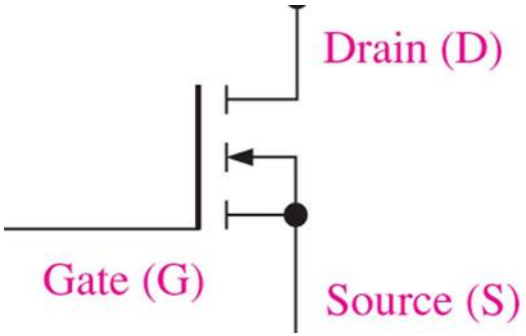
Integrated Circuit Technologies

Two Kinds of Transistors

- Two major classes of transistors:
  - •Bipolar Junction Transistors (BJTs)



  - •Metal-Oxide Semiconductor Field Effect Transistor (MOSFETs)



Logic Families

- Two major logic families:
  - TTL (Transistor-Transistor Logic) based on bipolar junction transistors
  - CMOS (Complementary Metal Oxide Semiconductor) based on MOSFETs
- Within each family are several subfamilies .

- Originally, TTL chips were fast but used lots of power, and CMOS chips used little power but were slow.
- CMOS chips are sensitive to static discharge, and must be handled carefully.

7400 Series and 4000 Series

- A popular series of TTL chips is the 7400 series that you've used in previous courses: Wikipedia's list
- A popular series of CMOS chips is the 4000 series: Wikipedia's list
- To provide part number and pin number compatibility with the 7400 series, a later series of CMOS chips was developed as the 74HC00 series.

Basic Operational Characteristics and Parameters

- Consult datasheets for
  - DC supply voltage
  - Logic levels & noise margin
  - Power dissipation
  - Propagation delay
  - Speed-power product
  - Loading and fan-out
- Example datasheets:
  - 7404 TTL inverter
  - 74HC04 CMOS inverter

DC Supply Voltages

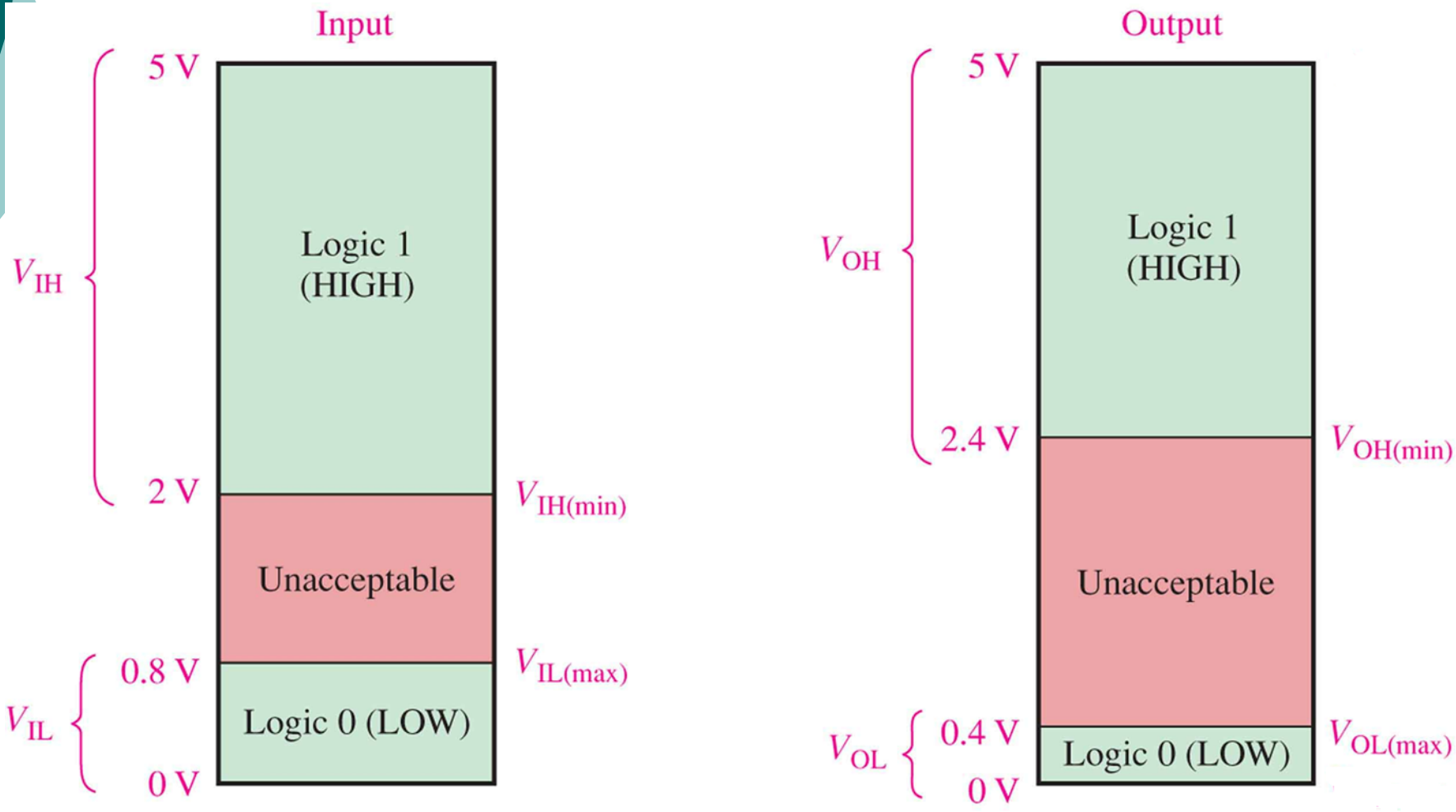
- TTL chips are optimized for 5 V supply, and cannot tolerate voltages far above or below 5 V.
- CMOS chips may be optimized for 5 V, 3.3 V, 2.5 V, or 1.8 V supplies. Most CMOS chips can tolerate a much wider range of supply voltages than TTL chips.

(Floyd, .

Logic Levels

- Four key voltage parameters when you're interfacing logic:
- $V_{IH(min)}$ = the minimum voltage that an **input** pin will recognize as a **HIGH**.
- $V_{IL(max)}$ = the maximum voltage an **input** pin will recognize as a **LOW**.
- $V_{OH(min)}$ = the minimum voltage that can appear on a **HIGH output** pin.
- $V_{OL(max)}$ = the maximum voltage that can appear on a **LOW output** pin.

Logic levels for TTL



Noise Margin

- The **noise margin** is the room for error between the voltage that an output pin produces and the voltage that an input pin expects.

- $V_{NH} = V_{OH(min)} - V_{IH(min)}$
- $V_{NL} = V_{IL(max)} - V_{OL(max)}$

Power Dissipation

- Recall that power equals current times voltage ($P=IV$).
- So a gate's power dissipation is given by its supply voltage (V_{CC}) times its supply current (I_{CC}).
- A lower-power device wastes less energy, generates less heat, and costs less to run than a higher-power device.

Propagation Delay

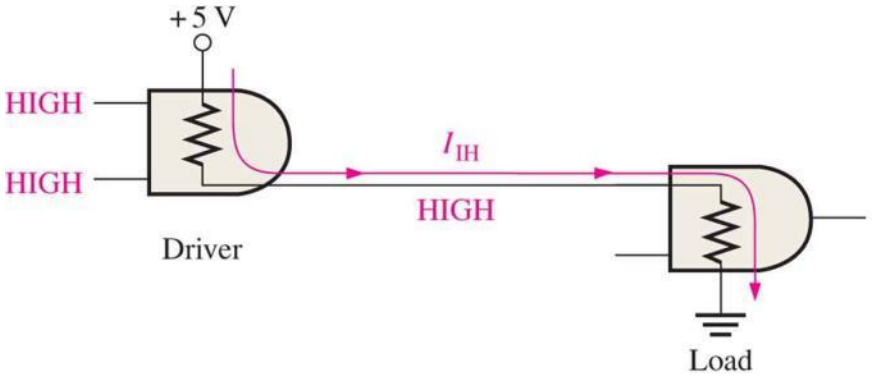
- Recall that data sheets specify propagation delays for low-to-high transitions (t_{PLH}) and high-to-low transitions (t_{PHL}).
- A device with a smaller propagation delay can run faster (at a higher frequency) than a device with a higher propagation delay.

Speed-Power Product

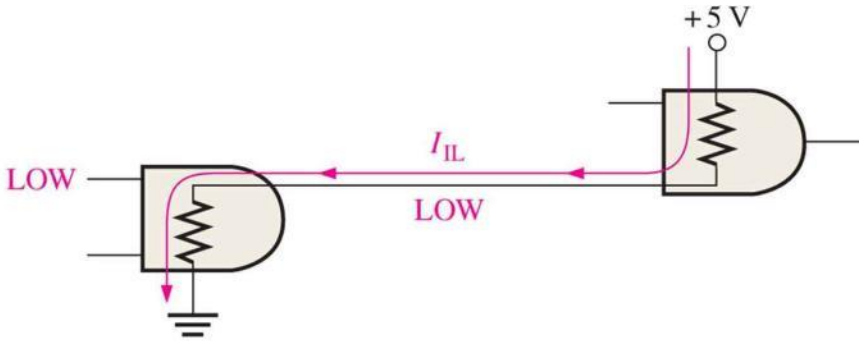
- A useful overall measure of a device's performance is its **speed-power product**, found by multiplying its average power dissipation times its average propagation delay.
- The lower the speed-power product, the better.

Current-Sourcing and Current-Sinking

- For TTL:
  - A HIGH output sources current
  - A LOW output sinks current.



(a) Current sourcing



(b) Current sinking

Fan-out

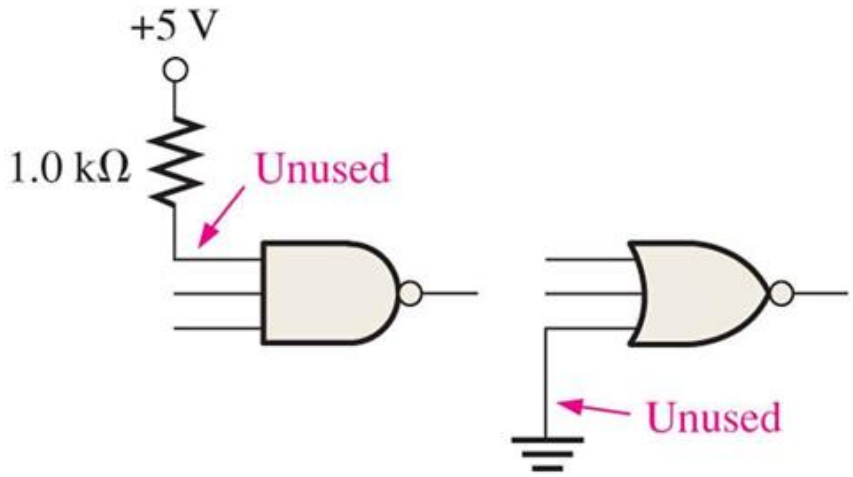
- **Fan-out** means the number of load inputs that a given output can drive.
- With TTL, current is the limiting factor in determining fan-out.
- With CMOS, capacitance is the limiting factor.

Calculating TTL Fan-out

- For a standard TTL gate:
  - A LOW input sources up to 1.6 mA.
  - A LOW output can sink up to 16 mA.
- Also:
  - A HIGH input sinks up to 40 μA.
  - A HIGH output can source up to 400 μA.
- Thus, standard TTL has a fan-out of 10.
- See Wisconsin Online's Fan-out Lesson

Unused Inputs

- Recall that unused inputs should not be left floating. Either tie them to V_{CC} through a 1-kΩ resistor or tie them to ground.



Three Kinds of Outputs

- TTL chips can have three kinds of outputs:
  - Totem-pole (the most common)
  - Open-collector
  - Three-state

Totem-Pole Output

- Most chips you've used up to now have had totem-pole outputs.

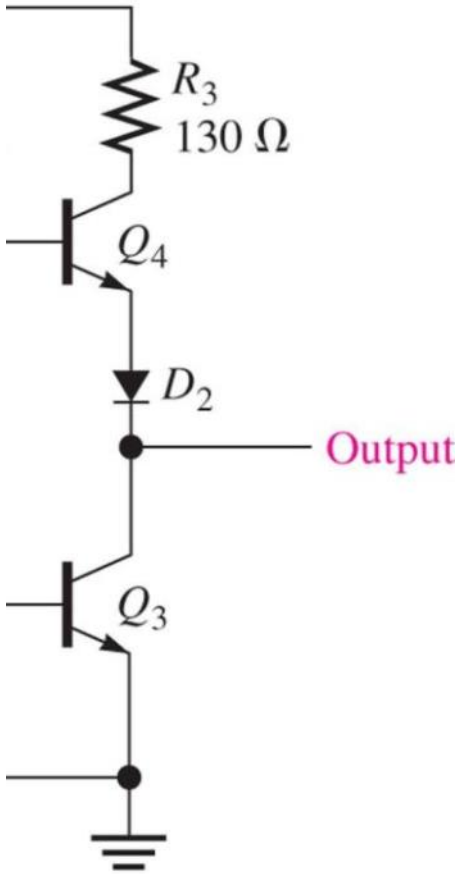
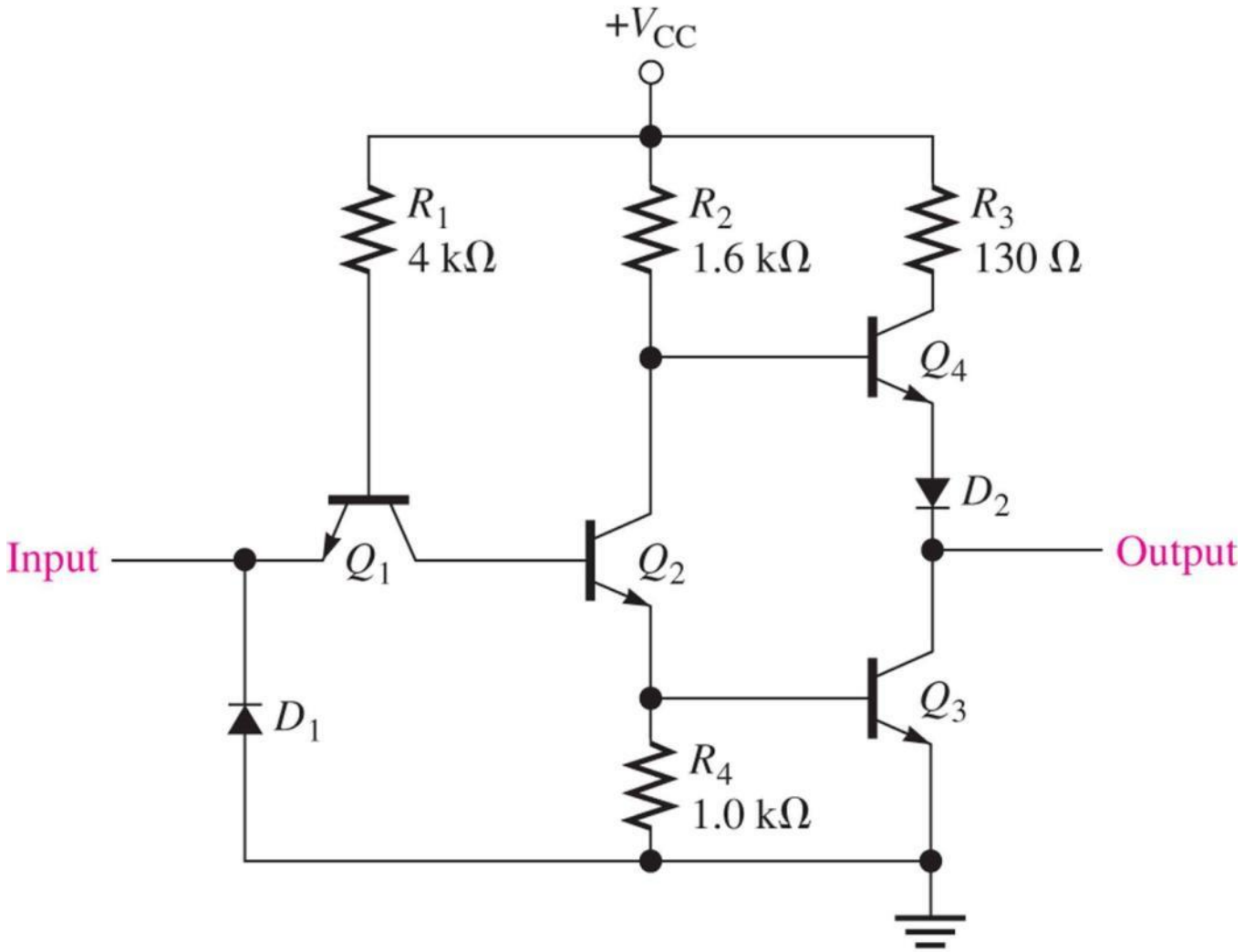


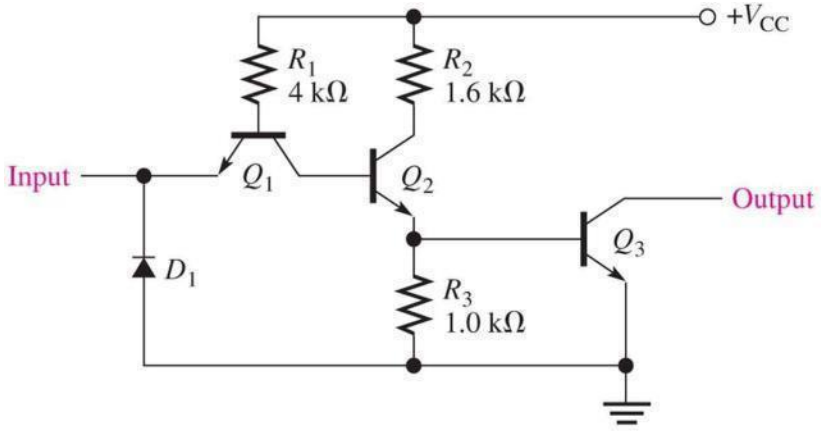
Figure 14.27 A standard TTL inverter circuit.



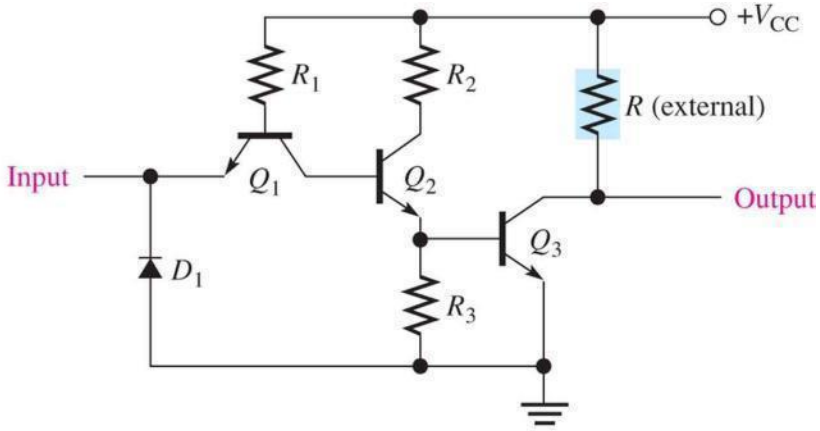
Open-Collector Output

- Missing a transistor internally, so you must provide an external pull-up resistor.
- Allows for the use of higher-than-usual voltages and currents.
- Allows a trick called "wired-AND," which means you can AND the outputs of two chips by tying them directly together. (Never tie totem-pole outputs together.)

Figure 14.31 TTL inverter with open-collector output.

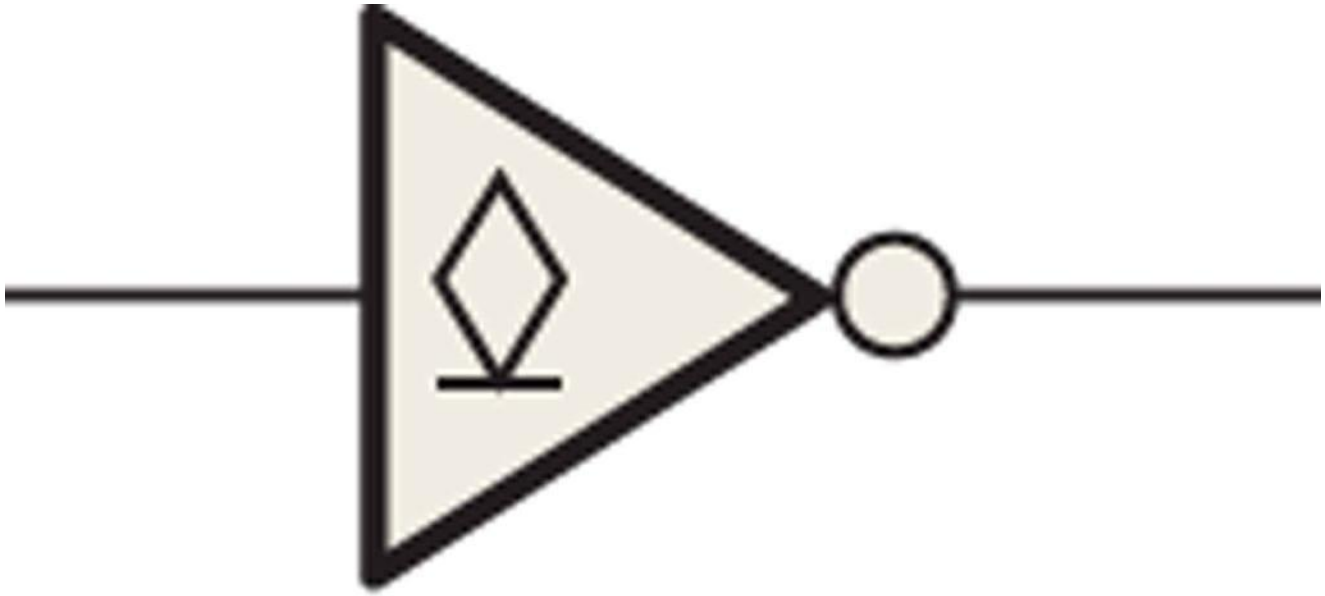


(a) Open-collector inverter circuit



(b) With external pull-up resistor

Figure 14.32 Open-collector symbol in an inverter.



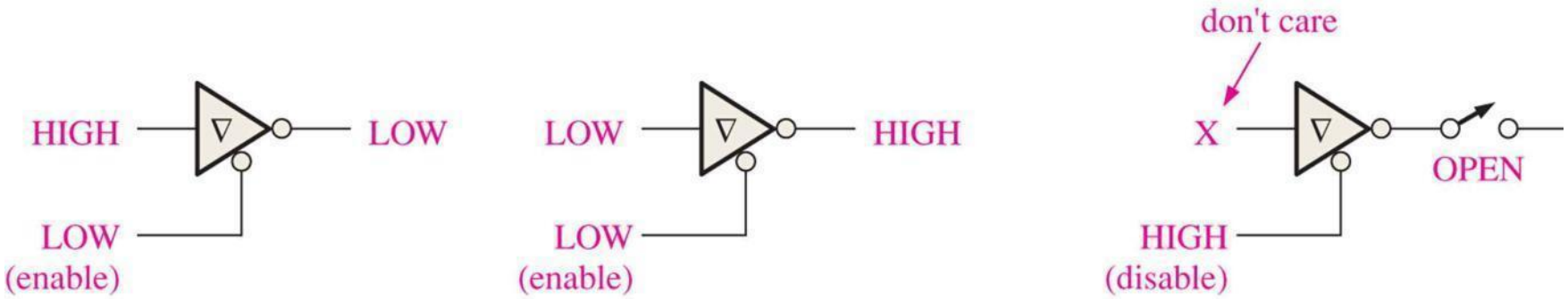
Some Open-Collector Chips

- 7405 (Hex Inverters with Open-Collector Outputs)
- 7409 (Quad 2-Input AND with Open-Collector Outputs)
- 7412 (Triple 3-Input NAND with Open-Collector Outputs)

Three-State Output

- In addition to the two usual output states (HIGH and LOW), has a third output state called high-impedance (“high-Z”).
- In the high-Z state, the output is disconnected from the external circuit.
- Useful when the outputs of many chips are tied to the same bus: at any time, only one of them should be connected to the bus.

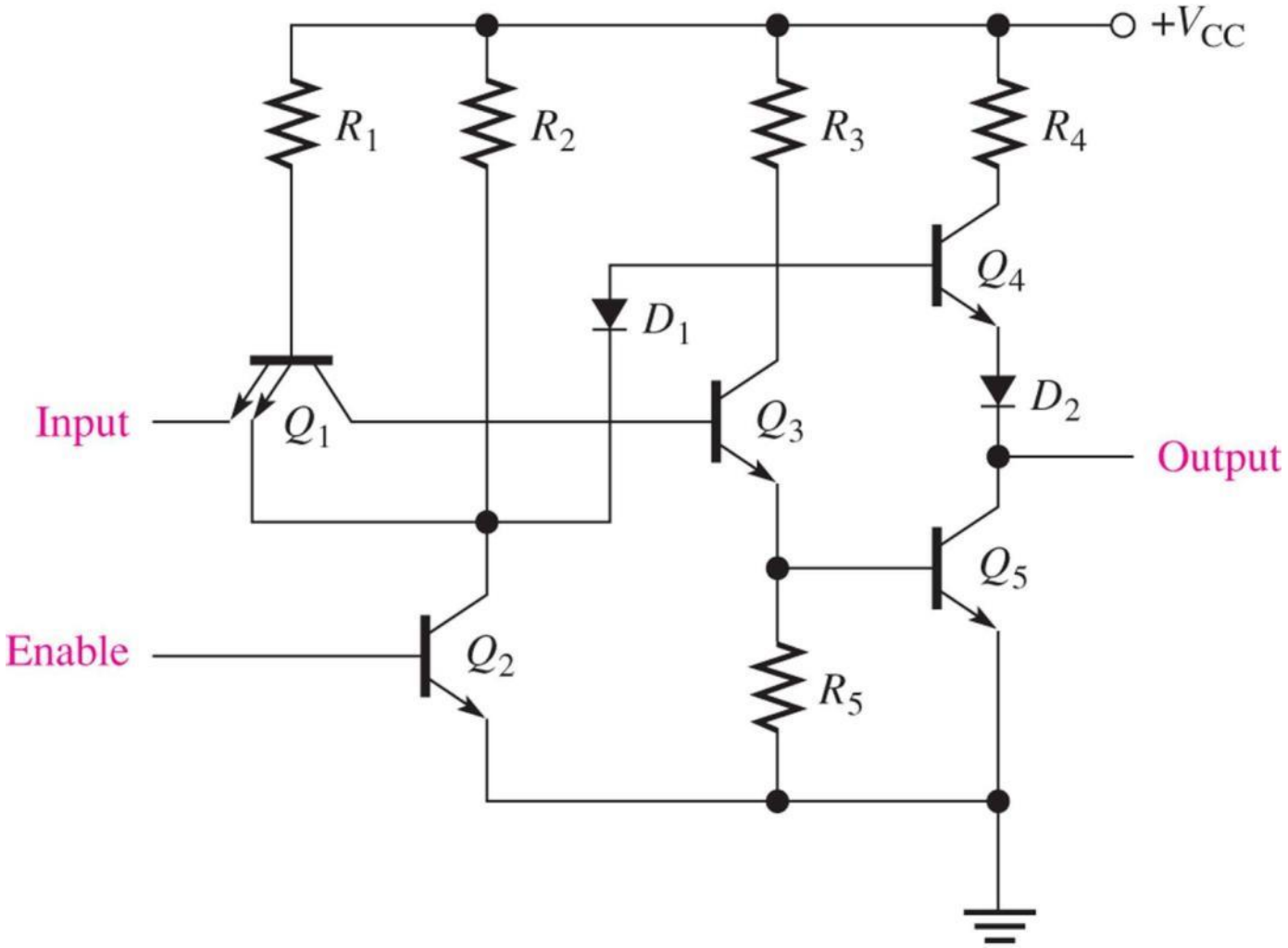
Figure 14.22 The three states of a tristate circuit.



(a) Enabled for normal logic operation

(b) High-*Z* state

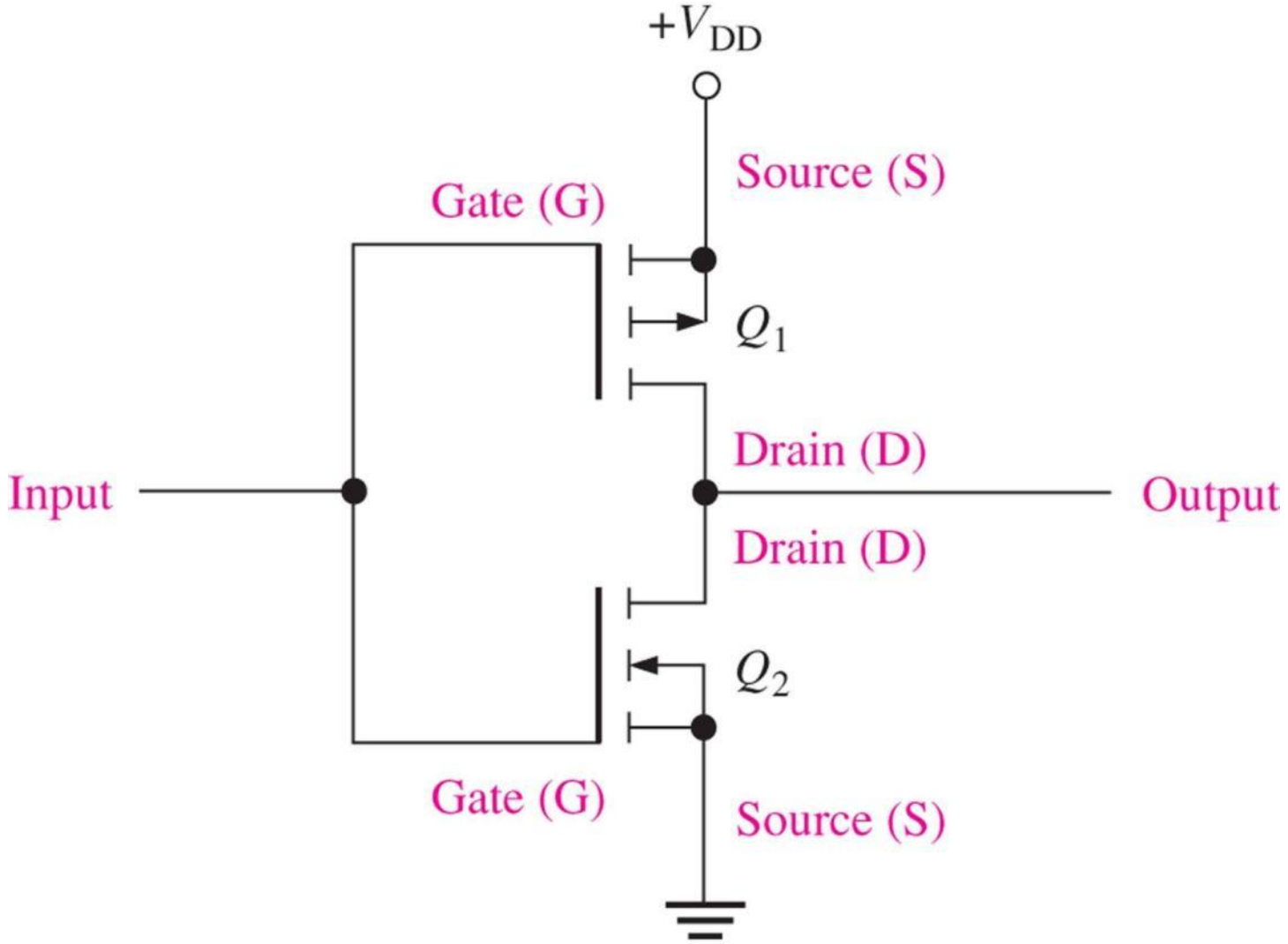
Figure 14.33 Basic tristate inverter circuit.



Some Three-State Chips

- 74251 (Data Selectors/Multiplexers with 3-State Outputs)
- 74LS295 (4-Bit Right-Shift Left-Shift Registers With 3-State Outputs)
- 74LS348 (8-Line To 3-Line Priority Encoders With 3-State Outputs)

Figure 14.17 A CMOS inverter circuit.



Three Kinds of CMOS Outputs

- Like TTL chips, CMOS chips can have two kinds of special-purpose outputs instead of the usual outputs:
  - Open-drain
    - Similar to open-collector in TTL
    - Requires an external pull-up resistor
  - Three-state

Other Logic Families

- ECL (Emitter-Coupled Logic): The fastest logic family
- PMOS (p-Channel MOS)
- NMOS (n-Channel MOS)
- E^2CMOS (Electrically Erasable CMOS)