Chapter 13: Basic Op-Amp Circuits

- In the last chapter, you learned about the principles, operation, and characteristics of the operational amplifier.
- Op-amps are used in such a wide variety of circuits and applications that it is impossible to cover all of them in one chapter, or even in one book. Therefore, in this chapter, four fundamentally important circuits are covered to give you a foundation in op-amp circuits.
- The basic circuits for op-amp's are

1- Comparators
2- Summing Amplifiers
3- Integrators and Differentiators

13.1: Comparators

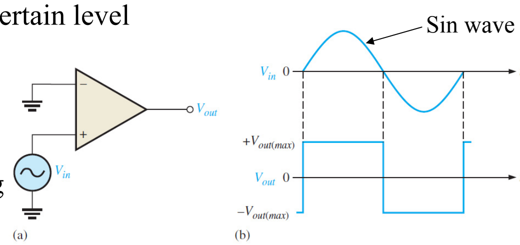
- A **comparator** is a specialized *nonlinear* op-amp circuit that compares between two input voltages and produces an output state that indicates which one is greater. Comparators are designed to be fast and frequently have other capabilities to optimize the comparison function.

- In this application, the op-amp is used in the open-loop configuration, with the input voltage on one input and a reference voltage on the other.

13.1: Comparators

- One application of an op-amp used as a comparator is to determine when an input voltage exceeds a certain level

Zero-Level Detection



- The figure shown is the zero-level detector circuit; the inverting (-) input is grounded to produce a zero level (reference to compare with), and the input signal voltage is applied to the noninverting (+) input

- Since V_{in} is at noninverting input As shown in figure;

→Any V_{in} above the zero will produce a +ve saturated output ($+V_{out(max)}$)

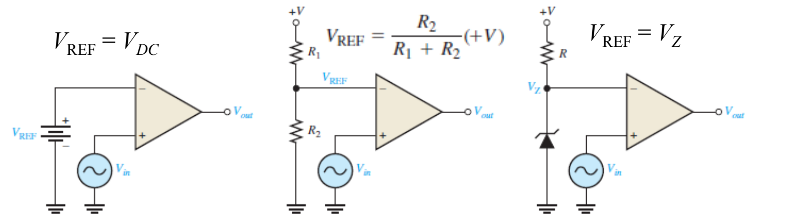
→ any V_{in} below the zero will produce a –ve saturated output ($-V_{out(min)}$)

- Saturation of the output is due to the open-loop op-amp that have a very high voltage gain → very small difference voltage between the two inputs drives the amplifier into saturation (non linear operation)

13.1: Comparators

Nonzero-Level Detection

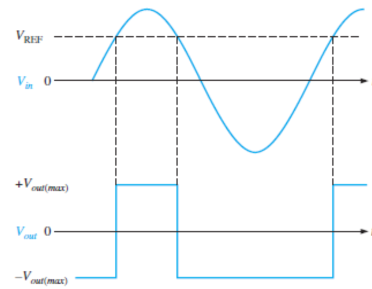
- The reference voltage can be set to non zero voltage (+ve ot -ve) by adding a dc voltage or voltage divider or zener or ….



- As shown in the output voltage for given input (sinewave)

→Any voltage above V_{REF} → V_{out} will be saturated +ve ($V_{out(max)}$)

→ Any voltage Below V_{REF} → V_{out} will be saturated -ve ($V_{out(min)}$)



(d) Waveforms

13.1: Comparators

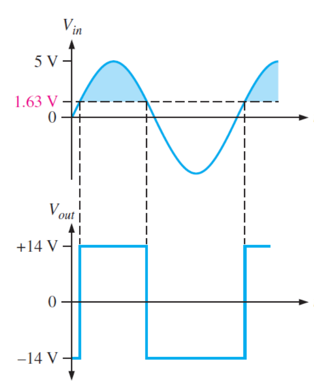
Nonzero-Level Detection: Example

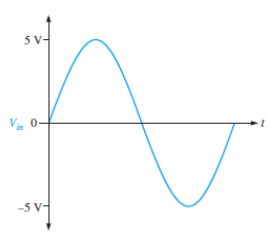
For the given comparator and input signal, draw the output showing its proper relationship to the input signal. Assume the maximum output levels of the comparator are ; ±14 V.

$$V_{REF} = \frac{R_2}{R_1 + R_2}(+V)$$

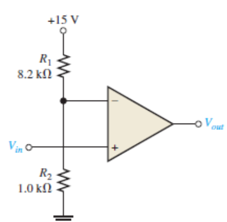
$$= \frac{1.0\,k\Omega}{8.2\,k\Omega + 1.0\,k\Omega}(+15\text{ V})$$

$$= 1.63\text{ V}$$





(a)



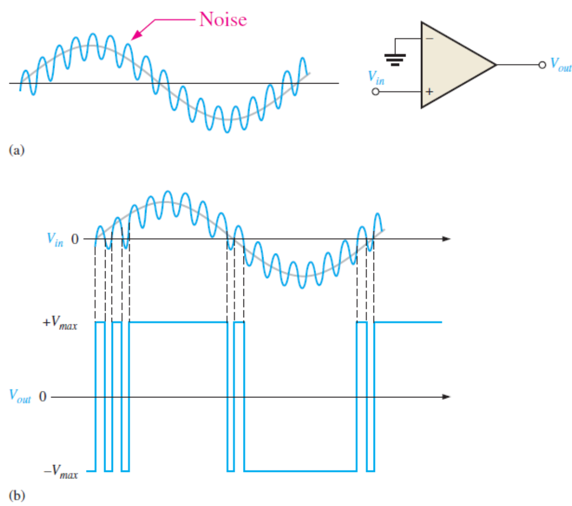
(b)

13.1: Comparators

Effects of Input Noise on Comparator Operation

In many practical situations, noise (unwanted voltage fluctuations) appears (superimposed) on the input line → we will have an erratic (شاذ) output voltage

- When the sine wave approaches 0, the fluctuations due to noise may cause the total input to vary above and below 0 several times, thus producing an erratic output voltage as shown



13.1: Comparators

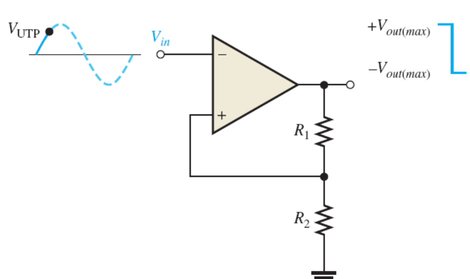
Reducing Noise Effects with Hysteresis

- **Hysteresis** is incorporated by adding regenerative (positive) feedback, which creates two switching points: the upper trigger point (UTP) and the lower trgger point (LTP). After one trigger point is crossed, it becomes inactive and the other one becomes active.

When V_{out} is $+V_{out(max)}$ → UTP is set by

$$V_{\text{UTP}} = \frac{R_2}{R_1 + R_2}(+V_{out(max)})$$

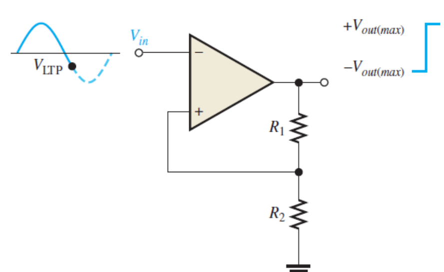
→ When V_{in} exceeds UTP, the output switches to the $-V_{out(max)}$



When V_{out} is $-V_{out(max)}$ → LTP is set by

$$V_{\text{LTP}} = \frac{R_2}{R_1 + R_2}(-V_{out(max)})$$

→ When V_{in} goes below LTP, the output switches to the $+V_{out(max)}$



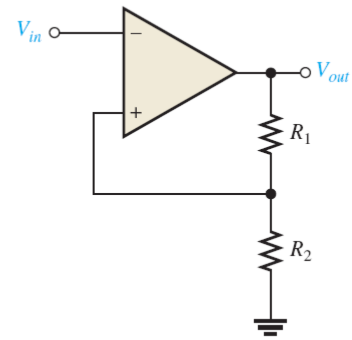
13.1: Comparators

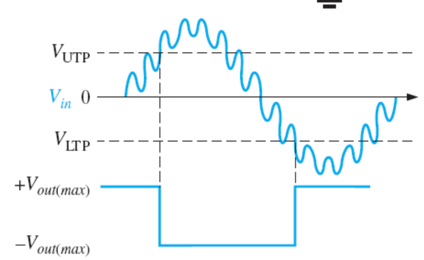
Reducing Noise Effects with Hysteresis

- Hence, the device triggers only once when UTP or LTP is reached as shown; thus, there is immunity to noise that is riding on the input signal.
- The amount of hysteresis is defined by the difference of the two trigger levels.

$$V_{HYS} = V_{UTP} - V_{LTP}$$

- A comparator with built-in hysteresis is sometimes known as a **Schmitt trigger**.

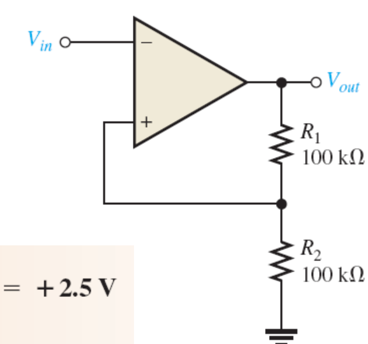




13.1: Comparators

Reducing Noise Effects with Hysteresis: Example

Determine the upper and lower trigger points for the comparator circuit in figure. Assume that $+V_{out(max)} = +5$ V and - $V_{out(max)} = -5$V.



$$V_{UTP} = \frac{R_2}{R_1 + R_2}(+V_{out(max)}) = 0.5(5\text{ V}) = \mathbf{+2.5\ V}$$

$$V_{LTP} = \frac{R_2}{R_1 + R_2}(-V_{out(max)}) = 0.5(-5\text{ V}) = \mathbf{-2.5\ V}$$

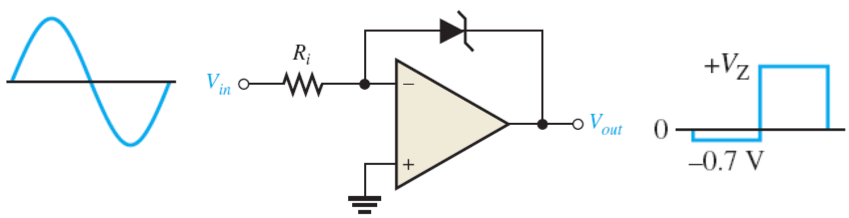
13.1: Comparators
Output Bounding

- In some applications, it is necessary to limit the output voltage levels of a comparator to a value less than that provided by the saturated op-amp.
- A process of limiting the output called **bounding** can be used by adding a single zener diode to limit the output voltage to the zener voltage in one direction and to the forward diode voltage drop in the other direction.

- If zener anode is connected to inverting input (virtual ground, V = 0) → when V_{out} is +ve, zener is reverse → V_{out} = +V_Z

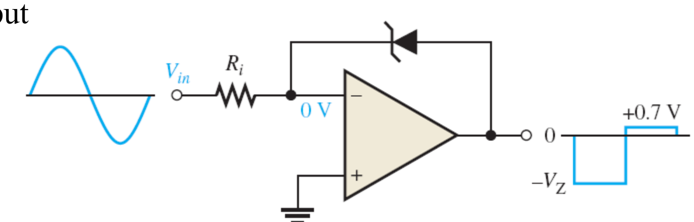
→When V_{out} is –ve, zener is forward→ V_{out} = -0.7V

→ positive bounded output

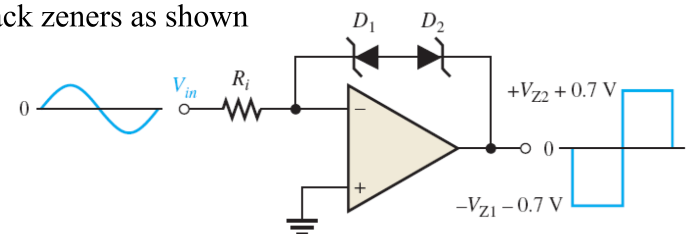


13.1: Comparators
Output Bounding

- If zener is reversed, the result will be the inverse → negative bounded out put

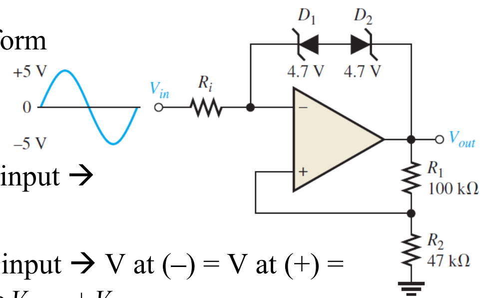


- Positive and negative bounded out put can be obtained by putting two back to back zeners as shown



13.1: Comparators
Output Bounding: Example

Determine the output voltage waveform



We have zener diodes between input and output → Bounded output.
But we have feedback to (+) op-amp input → we have also hysteresis voltages

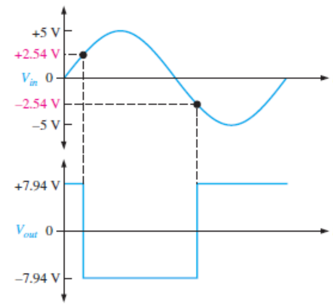
Since input voltage is at inverting (-) input → V at (–) = V at (+) = hysteresis voltage → Hence V_{out} will be $V_{zeners} + V_{hysterisi}$

At + ve V_{out} → $+V_{out} = V_{UPT} + V_{z2} + 0.7 = V_{UPT} + 5.4$

But $V_{UPT} = \frac{R_2}{R_2 + R_1}(+V_{out}) = \frac{47}{147}(+V_{out}) = 0.32(+V_{out})$

$\rightarrow +V_{out} = 0.32(+V_{out}) + 5.4$

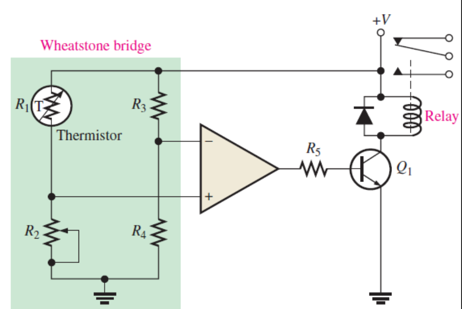
$\rightarrow +V_{out} = 7.94V$



Same can be found when V_{out} is –ve
→ $-V_{out} = -7.94$ V

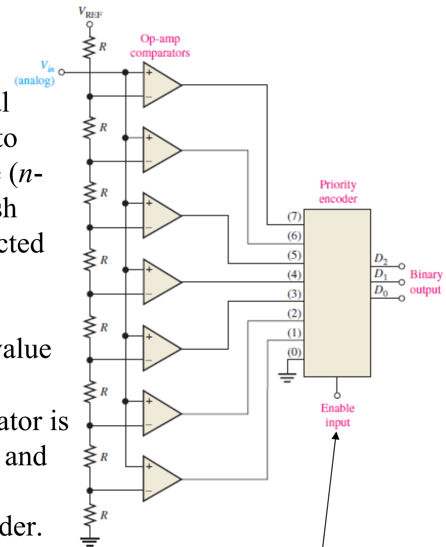
13.1: Comparators
Comparator Applications
Over-Temperature Sensing Circuit

- For the shown bridge, $R_3 = R_4$ and R_1 is high (> R_2) at normal temperatures → V at (+) is lower than V at (-).
- As the temperature increases, the resistance of the thermistor (R_1) decreases → V at (+) input increase. When the temperature reaches the critical value, R_1 becomes equal to R_2, and the bridge becomes balanced (since $R_3 = R_4$) . At this point the op-amp V_{out} switches from low to its high saturated output level, turning Q_1 on. This energizes the relay, which can be used to activate an alarm or initiate an appropriate response to the over-temperature condition.



13.1: Comparators
Comparator Applications
Analog-to-Digital (A/D) Conversion

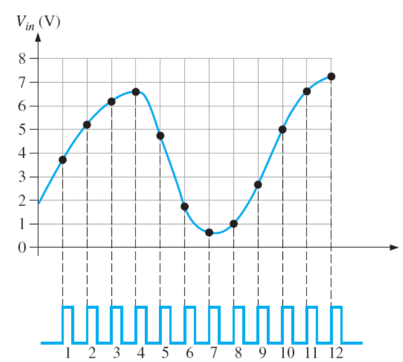
- Simultaneous or flash analog-to-digital converters (ADC) use 2^n-1 comparators to convert an analog input to a digital value (n-digit binary number) for processing. Flash ADCs are a group of comparators connected in parallel, each with a slightly different reference voltage. The priority encoder produces an output equal to the highest value input.
- The reference voltage for each comparator is set by the resistive voltage divider circuit and V_{REF}. The output of each comparator is connected to an input of the priority encoder. The *priority encoder* is a digital device that produces a binary number on its output representing the highest value input



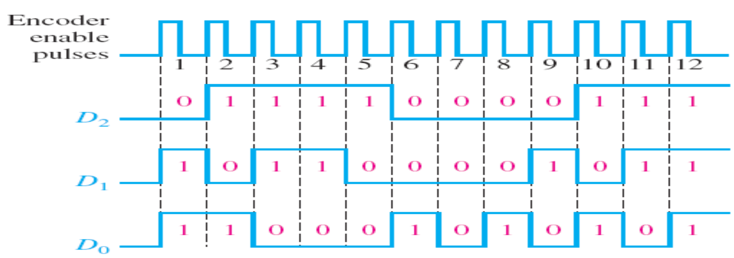
The encoder samples its input when a pulse occurs on the enable line (sampling pulse)

13.1: Comparators

for the input signal in Figure below Determine the binary number sequence of the three-digit simultaneous ADC (Figure shown before). Draw the resulting digital output waveforms. V_{REF} = +8V



Encoder enable pulses (sampling pulses)



Digital numbers: **011, 101, 110, 110, 100, 001, 000, 001, 010, 101, 110, 111**

13.2: Summing Amplifiers

- The summing amplifier is an application of the inverting op-amp covered in Chapter 12. The averaging amplifier and the scaling amplifier are variations of the basic summing amplifier.

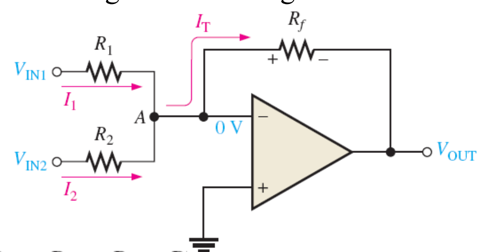
Summing Amplifier with Unity Gain

- A **summing amplifier** has two or more inputs; normally all inputs have unity gain. The output is proportional to the negative of the algebraic sum of the inputs.

$I_T = I_1 + I_2$ Since $V_{OUT} = -I_T R_f$

$$\longrightarrow V_{OUT} = -(I_1 + I_2)R_f$$

$$= -\left(\frac{V_{IN1}}{R_1} + \frac{V_{IN2}}{R_2}\right)R_f$$



For unity gain inverting amplifier $\longrightarrow R_1 = R_2 = R_f = R$

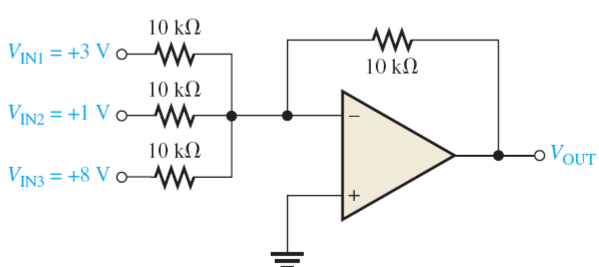
$$V_{OUT} = -\left(\frac{V_{IN1}}{R} + \frac{V_{IN2}}{R}\right)R = -(V_{IN1} + V_{IN2})$$

In general, for n inputs → $\mathbf{V_{OUT} = -(V_{IN1} + V_{IN2} + V_{IN3} + \cdots + V_{INn})}$

13.2: Summing Amplifiers

Summing Amplifier with Unity Gain: Example

Determine the output voltage in Figure



$$V_{OUT} = -(V_{IN1} + V_{IN2} + V_{IN3}) = -(3\text{ V} + 1\text{ V} + 8\text{ V}) = \mathbf{-12\text{ V}}$$

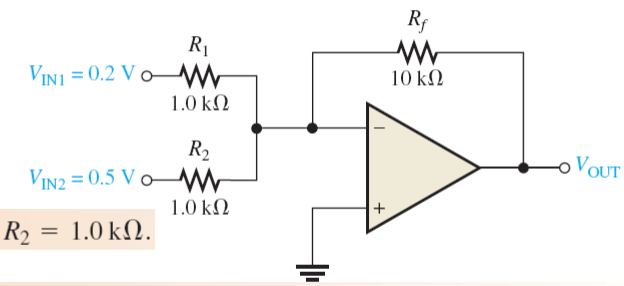
13.2: Summing Amplifiers

Summing Amplifier with Gain Greater Than Unity

- When R_f is larger than the input resistors, the amplifier has a gain of R_f/R, where R is the value of each equal-value input resistor. The general expression for the output is

$$V_{OUT} = -\frac{R_f}{R}(V_{IN1} + V_{IN2} + \cdots + V_{INn})$$

Example: Determine the output voltage for the summing amplifier shown



$R_f = 10\,\text{k}\Omega$ and $R = R_1 = R_2 = 1.0\,\text{k}\Omega$.

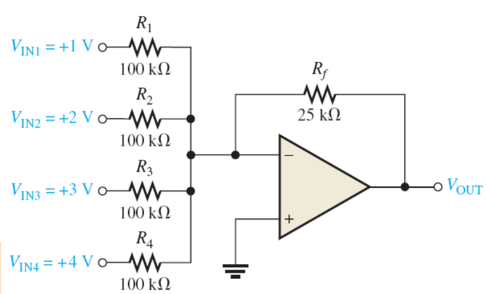
$$V_{OUT} = -\frac{R_f}{R}(V_{IN1} + V_{IN2}) = -\frac{10\,\text{k}\Omega}{1.0\,\text{k}\Omega}(0.2\text{ V} + 0.5\text{ V}) = -10(0.7\text{ V}) = \mathbf{-7\text{ V}}$$

13.2: Summing Amplifiers

Averaging Amplifier

- An **averaging amplifier** is basically a summing amplifier with the gain set to $R_f/R = 1/n$ (n is the number of inputs). The output is the negative average of the inputs.

Example: Show that the amplifier in Figure produces an output whose magnitude is the mathematical average of the input voltages.



$$V_{OUT} = -\frac{R_f}{R}(V_{IN1} + V_{IN2} + V_{IN3} + V_{IN4})$$
$$= -\frac{25\,\text{k}\Omega}{100\,\text{k}\Omega}(1\text{ V} + 2\text{ V} + 3\text{ V} + 4\text{ V}) = -\frac{1}{4}(10\text{ V}) = \mathbf{-2.5\text{ V}}$$

$$V_{IN(avg)} = \frac{1\text{ V} + 2\text{ V} + 3\text{ V} + 4\text{ V}}{4} = \frac{10\text{ V}}{4} = 2.5\text{ V}$$

13.2: Summing Amplifiers

Scaling Adder

■ A **scaling adder** has two or more inputs with each input having a different gain. The output represents the negative *scaled* sum of the inputs. the output voltage can be expressed as

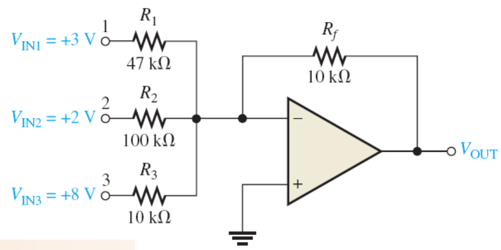
$$V_{OUT} = -\left(\frac{R_f}{R_1}V_{IN1} + \frac{R_f}{R_2}V_{IN2} + \cdots + \frac{R_f}{R_n}V_{INn}\right)$$

Example: Determine the weight of each input voltage for the scaling adder in Figure and find the output voltage.

Weight of input 1: $\frac{R_f}{R_1} = \frac{10\text{ k}\Omega}{47\text{ k}\Omega} = \mathbf{0.213}$

Weight of input 2: $\frac{R_f}{R_2} = \frac{10\text{ k}\Omega}{100\text{ k}\Omega} = \mathbf{0.100}$

Weight of input 3: $\frac{R_f}{R_3} = \frac{10\text{ k}\Omega}{10\text{ k}\Omega} = \mathbf{1.00}$



$$V_{OUT} = -\left(\frac{R_f}{R_1}V_{IN1} + \frac{R_f}{R_2}V_{IN2} + \frac{R_f}{R_3}V_{IN3}\right)$$
$$= -[0.213(3\text{ V}) + 0.100(2\text{ V}) + 1.00(8\text{ V})]$$
$$= -(0.639\text{ V} + 0.2\text{ V} + 8\text{ V}) = \mathbf{-8.84\text{ V}}$$

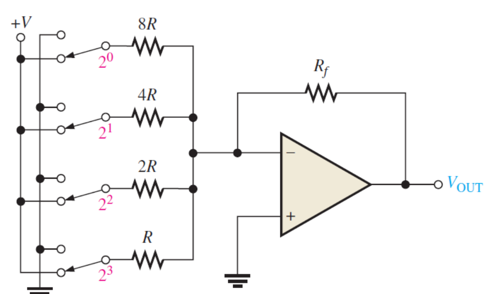
13.2: Summing Amplifiers

Applications: Digital to analogue convertor (DAC)

■ An application of a **scaling adder** is the D/A converter circuit shown here. the method shown here is useful only for small DACs.

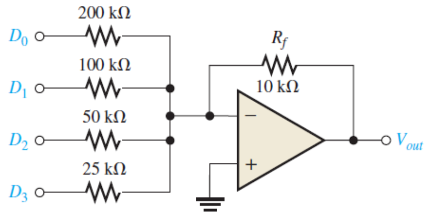
■ The resistors are inversely proportional to the binary column weights (The lowest-value resistor *R* corresponds to the highest weighted binary input (2^3). All of the other resistors are multiples of *R* and correspond to the binary weights 2^2, 2^1, and 2^0.

■ The inverting input is at virtual ground, and so the output voltage is proportional to the current through the feedback resistor R_f (sum of input currents) → $V_{out} = -IR_f$

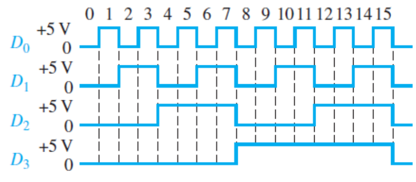


13.2: Summing Amplifiers
Applications: Digital to analogue convertor (DAC): Example

Determine the output voltage of the DAC for the four digit sequence binary codes shown, that are applied to the inputs. A high level is a binary 1, and a low level is a binary 0. The least significant binary digit is D_0.



(a)



(b)

For each input digit, we can calculate the current when it is at high (1) level at +5V

$$I_0 = \frac{5\text{ V}}{200\text{ k}\Omega} = 0.025\text{ mA} \quad I_1 = \frac{5\text{ V}}{100\text{ k}\Omega} = 0.05\text{ mA} \quad I_2 = \frac{5\text{ V}}{50\text{ k}\Omega} = 0.1\text{ mA} \quad I_3 = \frac{5\text{ V}}{25\text{ k}\Omega} = 0.2\text{ mA}$$

For each input digit, we have a corresponding digit output voltage

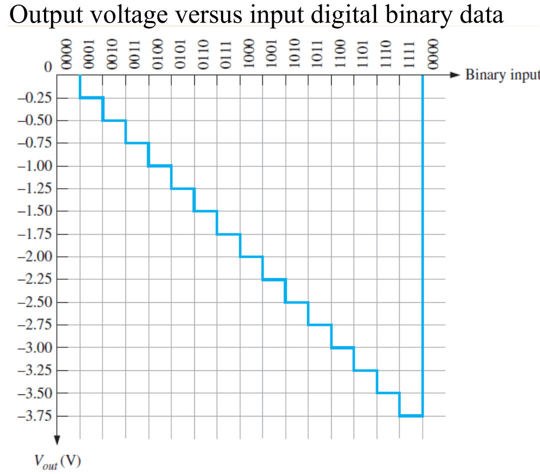
$$V_{OUT(D0)} = -R_f I_0 = -(10\text{ k}\Omega)(0.025\text{ mA}) = \mathbf{-0.25\text{ V}}$$
$$V_{OUT(D1)} = -R_f I_1 = -(10\text{ k}\Omega)(0.05\text{ mA}) = \mathbf{-0.5\text{ V}}$$
$$V_{OUT(D2)} = -R_f I_2 = -(10\text{ k}\Omega)(0.1\text{ mA}) = \mathbf{-1\text{ V}}$$
$$V_{OUT(D3)} = -R_f I_3 = -(10\text{ k}\Omega)(0.2\text{ mA}) = \mathbf{-2\text{ V}}$$

13.2: Summing Amplifiers
Applications: Digital to analogue convertor (DAC): Example – continued from previous

- Hence for any given digital value, the output will be the sum of corresponding digit output voltage:

input	Addition of digit voltages	Total (V_{out})
0000	0-0-0-0	0
0001	0-0-0-0.25	-0.25
0010	0-0-0.5-0	-0.5
0011	0-0-0.5-0.25	-0.75
0100	0-1-0-0	-1
0101	0-1-0-0.25	-1.25
0110	0-1-0.5-0	-1.5
1111	2-1-0.5-0.25	-3.75

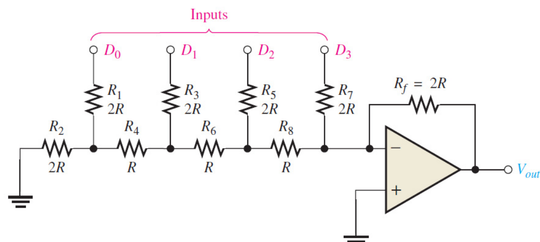
Output voltage versus input digital binary data



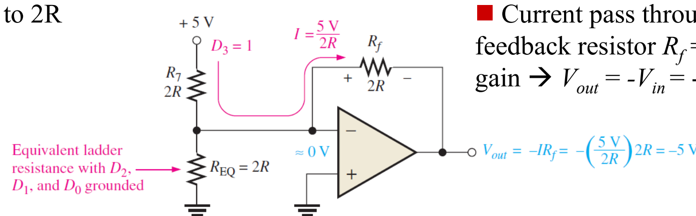
13.2: Summing Amplifiers
Applications: Digital to analogue convertor (DAC):

■ A more widely used method for D/A conversion is the ***R*/2*R* ladder**. The gain for D_3 is –1. Each successive input has a gain that is half of previous one. The output represents a weighted sum of all of the inputs (similar to the scaling adder).

→ the output voltage is proportional to the binary weight of the input bits



With $D_3 = 1$ (+5V) and $D_2 = 0$, $D_1 = 0$, $D_0 = 0$ → For circuit befor *D*3 input (befor R7) → the equivalent resistor can be calculated to be equal to 2R

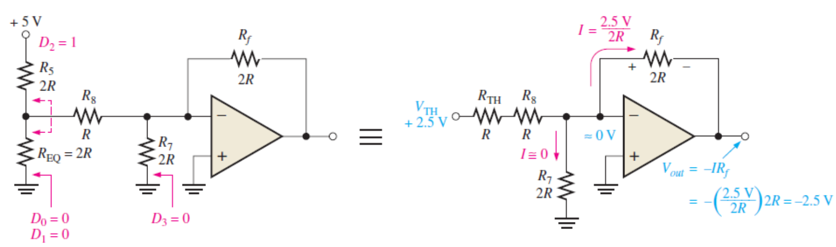


■ Current pass through R_7 = 2R and feedback resistor R_f = 2R → unity gain → $V_{out} = -V_{in} = -5$V

13.2: Summing Amplifiers
Applications: Digital to analogue convertor (DAC):

■ With D_2 = +V → if we thevinize the circuit before R_8 → we will have R_{TH} = R and V_{TH} = +2.5 (= +5/2). Again with unity gain → $V_{out} = -V_{in} = -V_{TH} = -2.5$V → gain for D_2 = ½ gain for D_3

→ With $D_2 = 1$ (+5V) and $D_3 = 0$, $D_1 = 0$, $D_0 = 0$ → $V_{out} = -2.5$



(b) Equivalent circuit for $D_3 = 0$, $D_2 = 1$, $D_1 = 0$, $D_0 = 0$

This process is repeated for other inputs

→ With $D_1 = 1$ (+5V) and $D_3 = 0$, $D_2 = 0$, $D_0 = 0$ → $V_{out} = -1.25$ V

→ With $D_1 = 1$ (+5V) and $D_3 = 0$, $D_2 = 0$, $D_0 = 0$ → $V_{out} = -0.625$ V

■ Hence, for different digital data input → The output represents a weighted sum of all of the inputs (similar to the scaling adder).

13.3: Integrators and differentiators

An op-amp **integrator** simulates mathematical integration, and **differentiator** simulates mathematical differentiation.

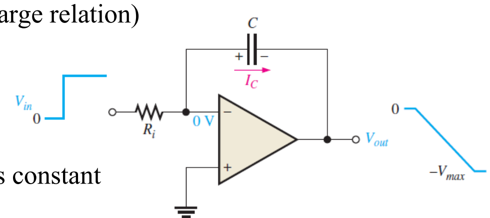
The Op-Amp Integrator: Ideal integrator

■ The **ideal integrator** is an inverting amplifier that has a capacitor in the feedback path. The output voltage is proportional to the negative integral (running sum) of the input voltage.

For capacitor $Q = I_C t$ (current charge relation)

Also charge on capacitor is

$Q = CV_C \longrightarrow V_C = \left(\frac{I_C}{C}\right)t$



Since V_{in} is constant → $I_i = V_{in}/R_i = I_C$ is constant

Hence I_C/C is constant → $V_C = \left(\frac{I_C}{C}\right)t$ is an equation of a straight line with a constant slope I_C/C .

$V_{out} = -V_C$, because (-) input of op-amp is virtual ground $\longrightarrow$ $V_{out} = -\left(\frac{I_C}{C}\right)t$

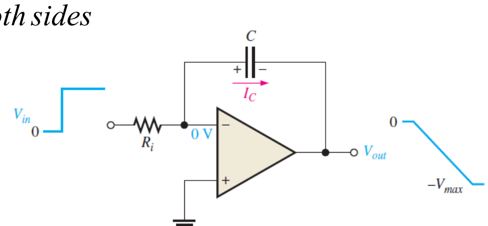
→output change or slope of the integrator $\frac{\Delta V_{out}}{\Delta t} = -\frac{V_{in}}{R_i C}$

13.3: Integrators and differentiators

The Op-Amp Integrator: Ideal integrator

■ As you can see the output voltage is the time integral of input voltage as also shown below

$$dq = Idt,\ But\ also\ dq = CdV$$
$$\rightarrow CdV_C = I_C dt,\ Integrate\ both\ sides$$
$$\rightarrow \int CdV_C = \int I_C dt$$
$$But\ I_C = I_i = V_{in} / R_i$$
$$\int CdV_C = \int \frac{V_{in}}{R_i} dt$$



$$\Rightarrow \Delta V_{out} = -\frac{V_{in}}{R_i C} \Delta t \text{ (}-\text{ve sign is added for inverting output)}$$

13.3: Integrators and differentiators

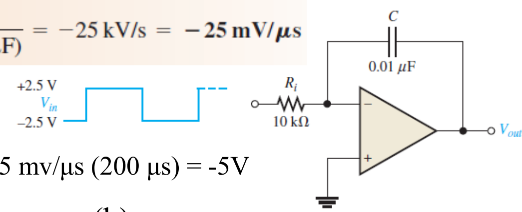
The Op-Amp Integrator: Ideal integrator -Example

(a) Determine the rate of change of the output voltage in response to the input square wave, as shown for the ideal integrator in Figure The output voltage is initially zero. The pulse width is 200μs

(b) Describe the output and draw the waveform.

(a) When (a) in is +ve (+2.5 V)

$$\frac{\Delta V_{out}}{\Delta t} = -\frac{V_{in}}{R_i C} = -\frac{2.5\ \text{V}}{(10\ \text{k}\Omega)(0.01\ \mu\text{F})} = -25\ \text{kV/s} = \mathbf{-25\ mV/\mu s}$$



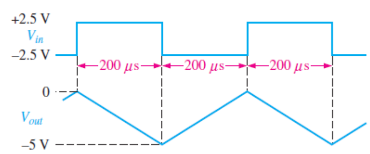
→ For 200 μs width, ΔV_{out} = -25 mv/μs (200 μs) = -5V

When (a) in is -ve (-2.5 V)

$$\frac{\Delta V_{out}}{\Delta t} = +\frac{V_{in}}{R_i C} = \mathbf{+25\ mV/\mu s}$$

ΔV_{out} = -25 mv/μs (200 μs) = 5V

(b)



13.3: Integrators and differentiators

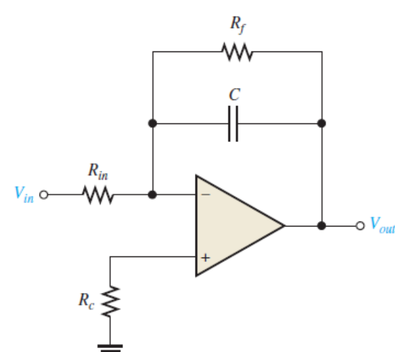
The Op-Amp Integrator: Practical integrator

- Op-amp integrating circuits must have extremely low dc offset and bias currents, because small errors are equivalent to a dc input. The ideal integrator tends t o accumulate these errors, which moves the output toward saturation (high infinite open loop gain because C is open to dc).

- The **practical integrator** overcomes these errors– the simplest method is to add a relatively large feedback resistor R_f→Relatively very small error compared to integrator without R_f.

- Also we may add R_c to (+) input to balance the effect of bias current

- Calculations will be same as for ideal integrators

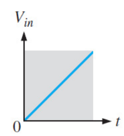


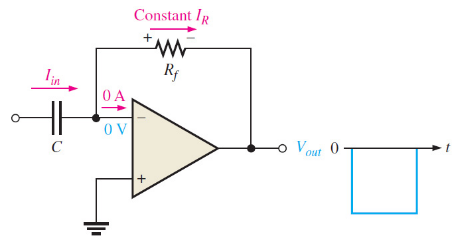
13.3: Integrators and differentiators

The Op-Amp Differentiator

- The **ideal differentiator** is an inverting amplifier that has a capacitor in the input path. The output voltage is proportional to the negative rate of change of the input voltage.

In this case, $V_{in} = V_C$ is linearly increase with time
From basic capacitor relation →





$$V_C = (I_C/C)t \longrightarrow I_C = \left(\frac{V_C}{t}\right)C$$

The output voltage is $V_{out} = -I_R R_f = -I_C R_f$

Because I through the op-amp = 0

$$\longrightarrow V_{out} = -\left(\frac{V_C}{t}\right)R_f C$$

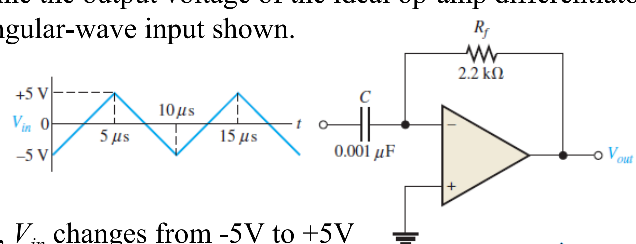
Which is constant (as shown) because the slope = $dV_{in}/dt = V_C/t = V_{in}/C$ is constant

Note that $R_f C$ is the RC circuit time constant

13.3: Integrators and differentiators

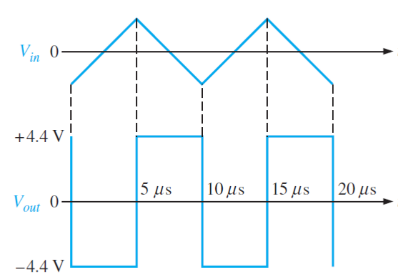
The Op-Amp Differentiator: Ideal differentiator - Example

Determine the output voltage of the ideal op-amp differentiator in Figure for the triangular-wave input shown.



In 5μs, V_{in} changes from -5V to +5V

→ slope $\frac{V_C}{t} = \frac{10\text{ V}}{5\ \mu\text{s}} = 2\text{ V}/\mu\text{s}$



The time constant is

$$R_f C = (2.2\text{ k}\Omega)(0.001\ \mu\text{F}) = 2.2\ \mu\text{s}$$

$$\rightarrow V_{out} = -\left(\frac{V_C}{t}\right)R_f C = -(2\text{ V}/\mu\text{s})2.2\ \mu\text{s} = \mathbf{-4.4\text{ V}}$$

For the –ve slope input voltage → $V_{out} = \mathbf{+4.4\text{ V}}$

13.3: Integrators and differentiators

The Op-Amp Differentiator: Practical differentiator

The very low reactance of C at high frequencies means an ideal differentiator circuit has very high gain for high-frequency noise. To compensate for this, a small series resistor is often added to the input. This **practical differentiator** has reduced high frequency gain and is less prone to noise.

- Also we may add R_c to (+) input to balance the effect of bias current

- Calculations will be same as for ideal differentiator