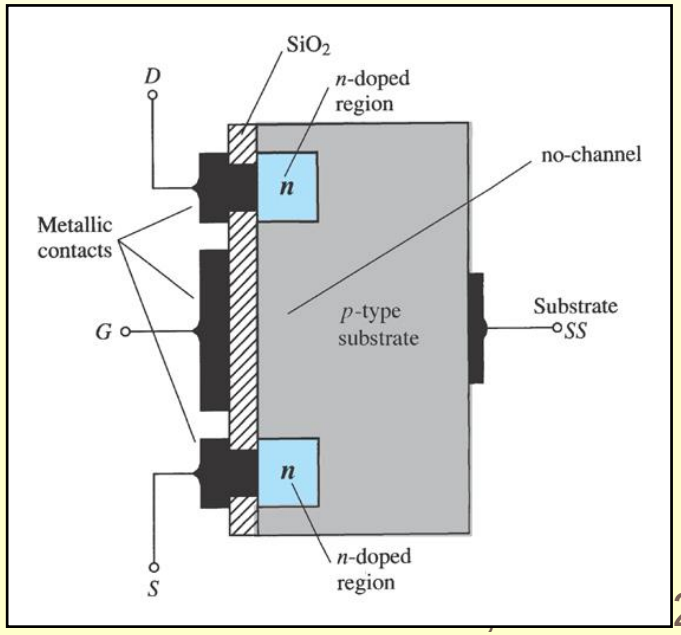
Supplementation

- Field Effect Transistors
- DC Biasing
- FET Amplifiers

Field Effect Transistors

What is FET?

In FET, a weak electrical signal coming through one electrode creates an electric field which controls the current flowing.



FET	BJT
1. FET is an unipolar semiconductor device because its operation depends upon the flow of majority carriers *i.e.*, either holes or electrons as the case may be.	1. BJT is a bipolar semiconductor device because the current constituting elements are both majority carriers as well as minority carriers in this case.
2. The input impedance of FET is much more larger (ranging in Megaohms) than BJT. The reason behind this is that the input terminal *i.e.*, gate to source of FET is reverse biased and reverse bias offers ideally infinite resistance.	2. The input impedance of BJT is very less in comparison to FET.
3. FET is a voltage controlled device.	3. BJT is a current controlled device.
4. FET is less noisy. Because there are no junctions.	4. Much noisy than FET.
5. Higher frequency response.	5. Frequency variation affects the performance.
6. Good thermal stability because of absence of minority carriers.	6. Temperature dependent, thermal runaway may cause.
7. Costlier than BJT.	7. Relatively cheaper.
8. Small sized.	8. Comparatively bigger.
9. In FET, relationship between input and output quantities is nonlinear due to square term in shockley's equations $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$	9. The BJT is an almost linear device or we can say that BJT works linearly in active region as an amplifier.
10. No offset voltage; so it works better as a switch or chopper.	10. There is always an offset voltage before switching.
11. Small gain bandwith product.	11. Greater than FET.

FET are smaller and more temperature stable than BJT and suited for IC applications.

FETs vs. BJTs

Similarities:

Amplifiers
Switching devices
Impedance matching circuits

Differences:

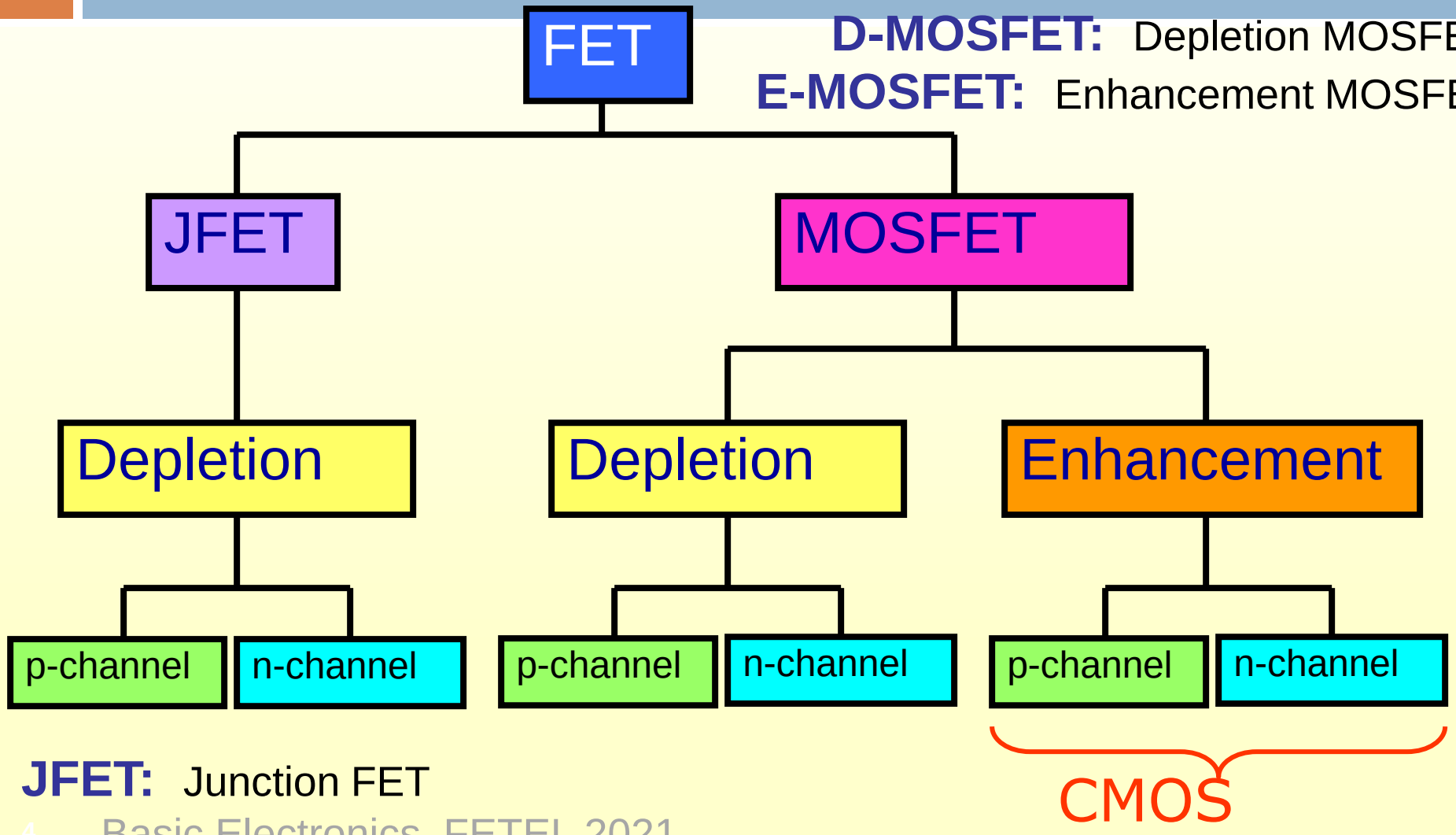
FETs are voltage controlled devices. BJTs are current controlled devices.

FETs have higher input impedance. BJTs have higher gain.

FETs are less sensitive to temperature variations and are better suited for integrated circuits

FETs are generally more static sensitive than BJTs.

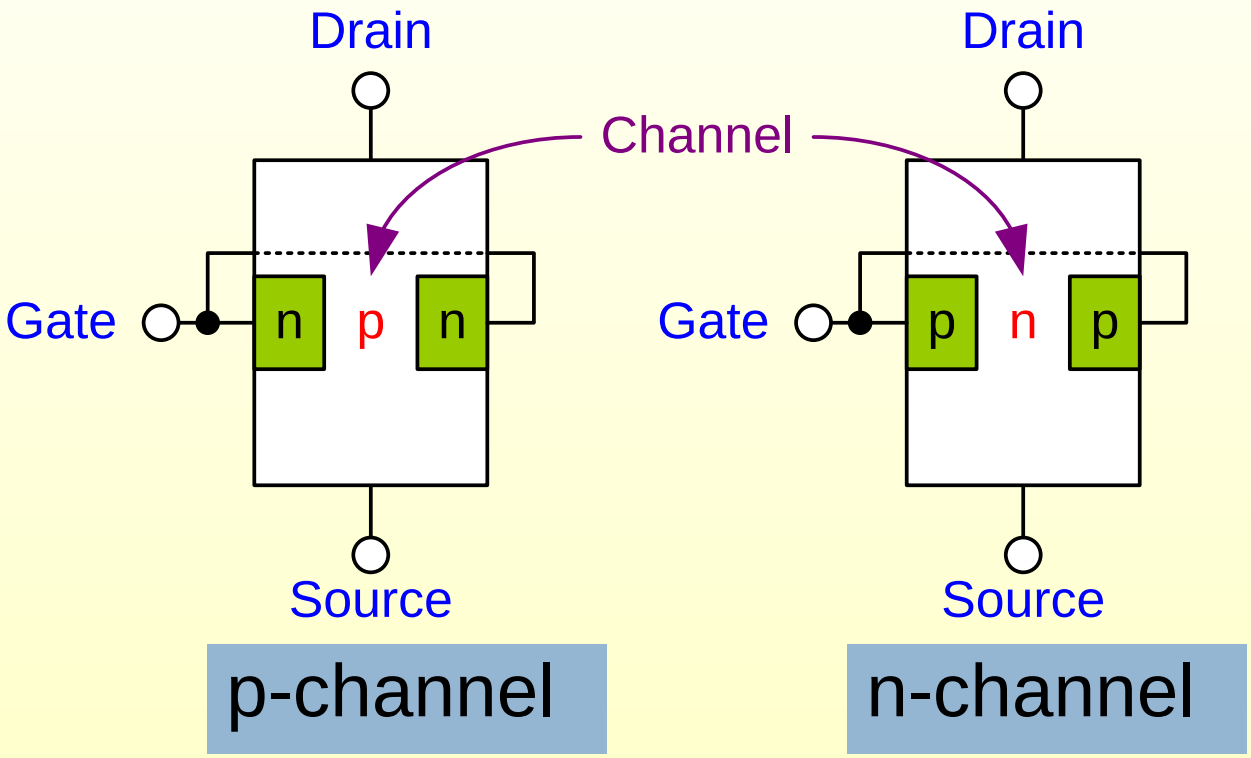
FET Family



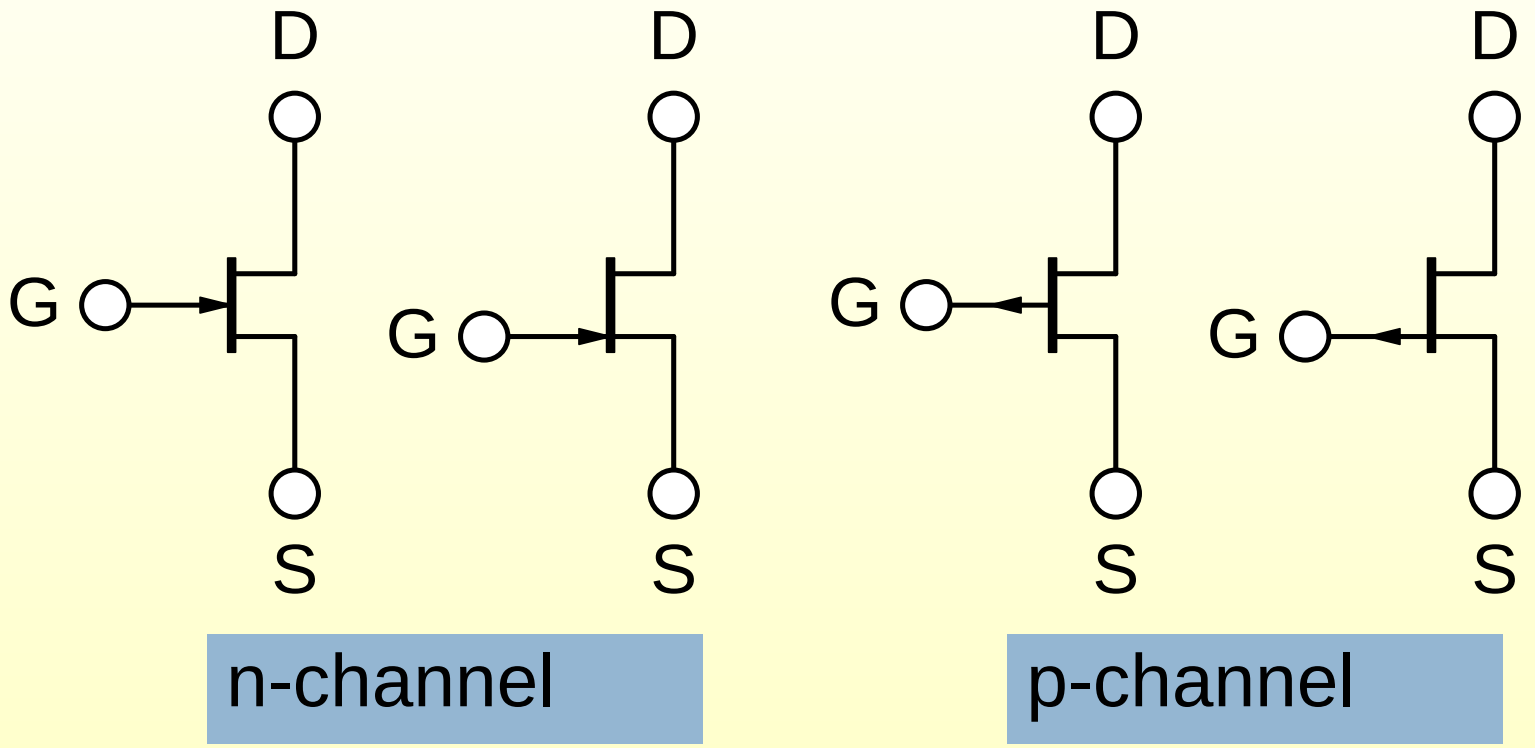
JFET: Junction FET

MOSFET: Metal–Oxide–Semiconductor FET

JFET construction.



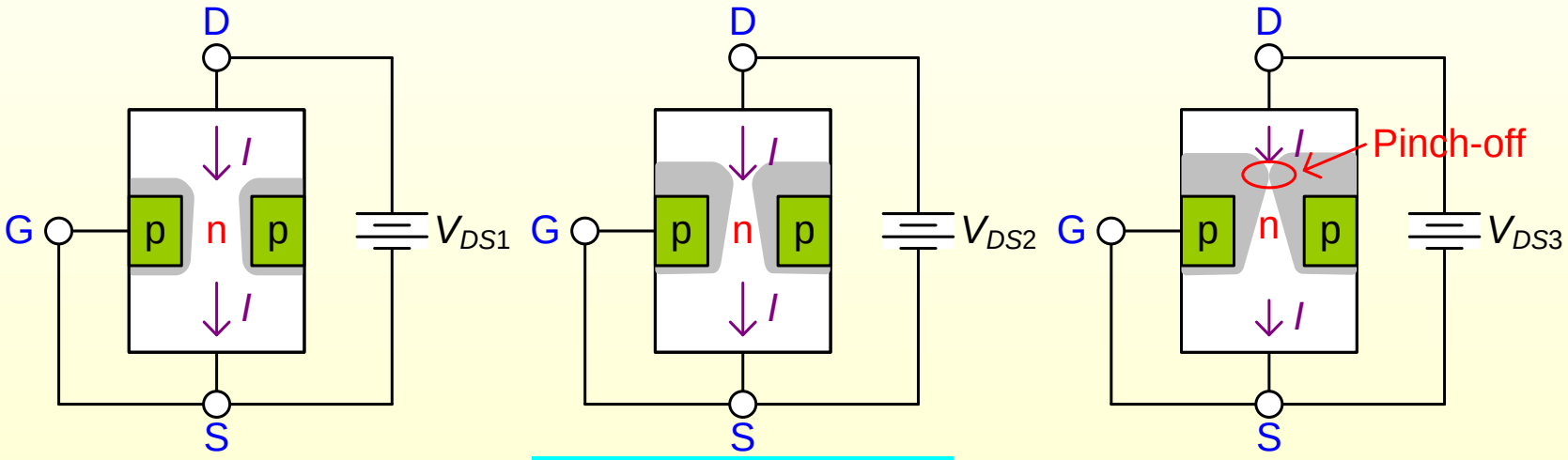
JFET schematic symbols.



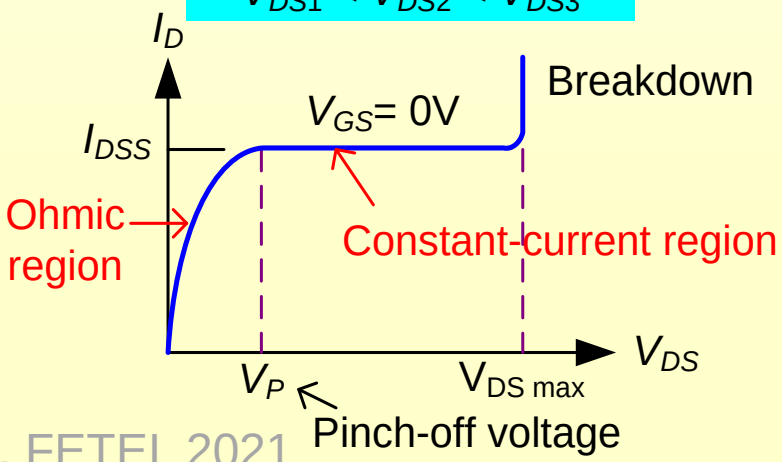
n-channel

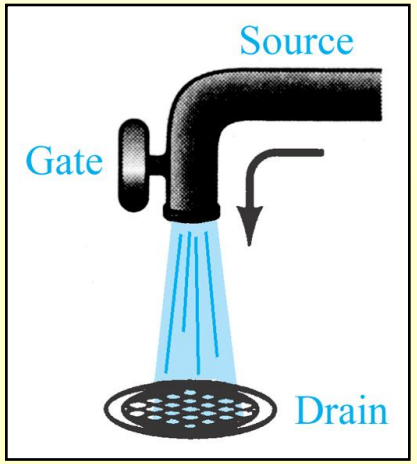
p-channel

Summary: Varying V_{DS} with V_{GS} = 0V

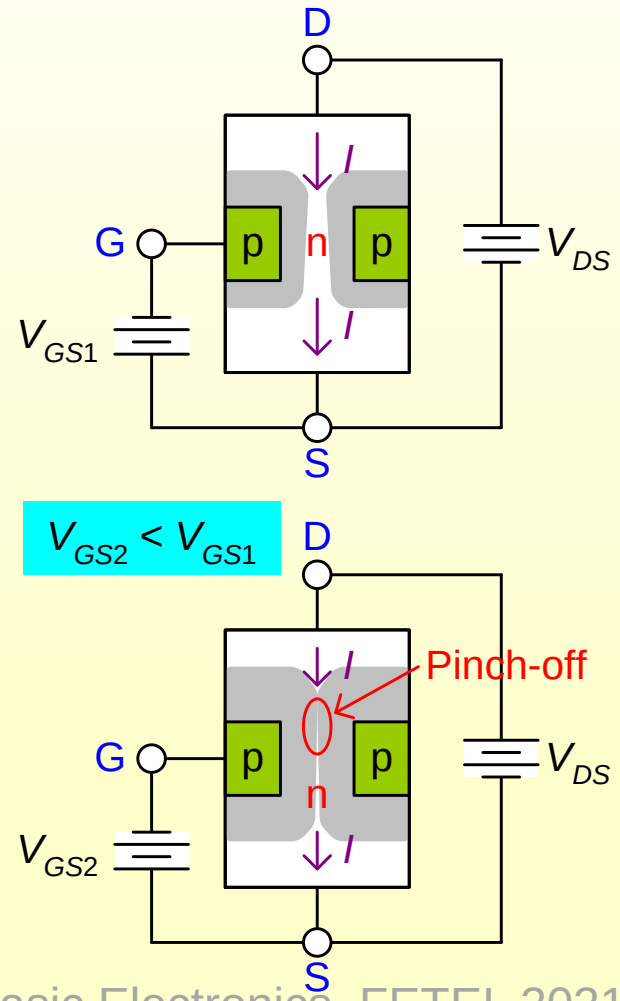


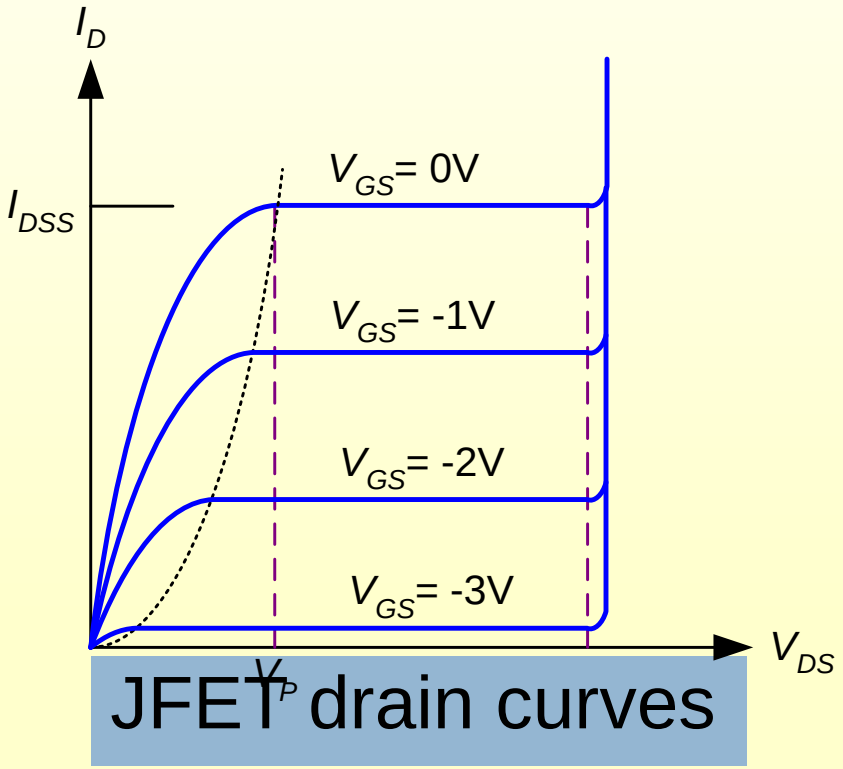
$V_{DS1} < V_{DS2} < V_{DS3}$





Summary: Varying V_{GS}

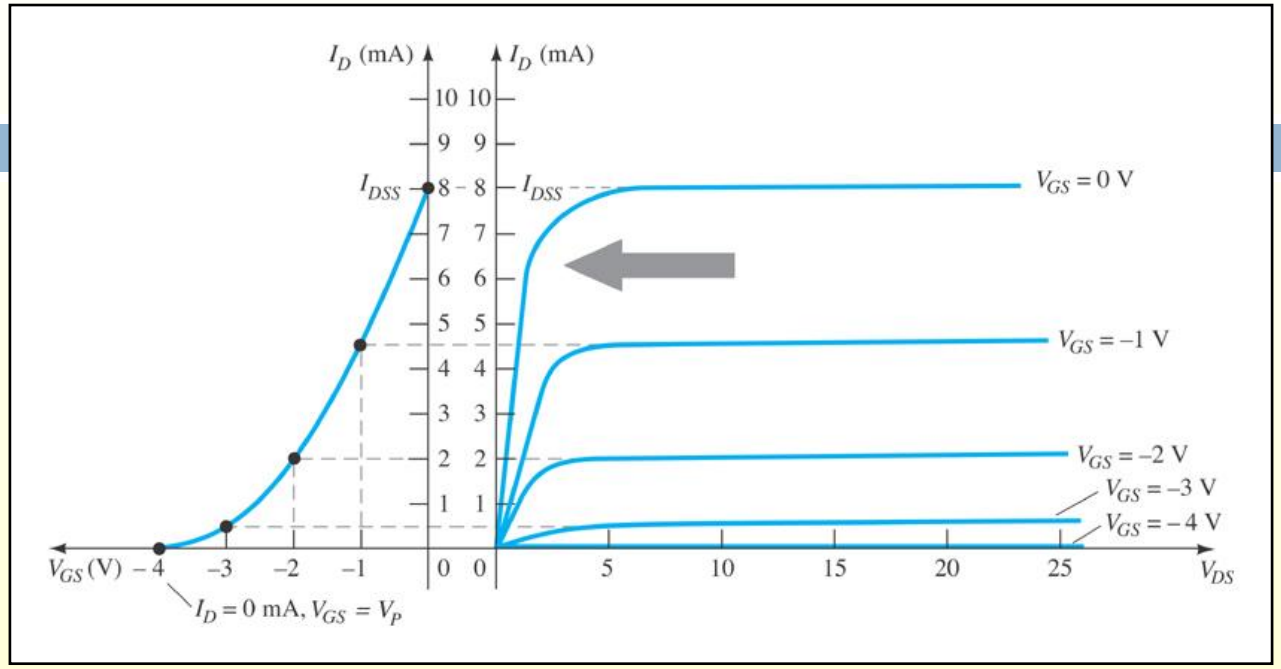




JFET drain curves

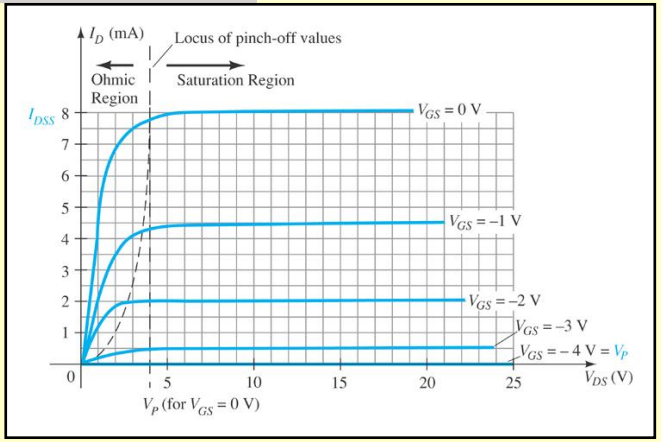
JFET Transfer Curve

This graph shows the value of I_D for a given value of V_{GS}.

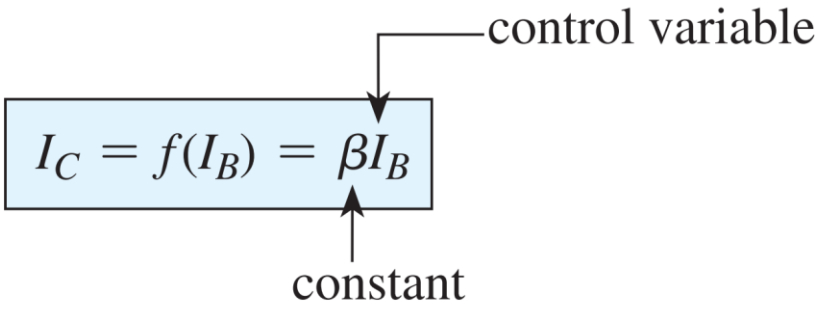


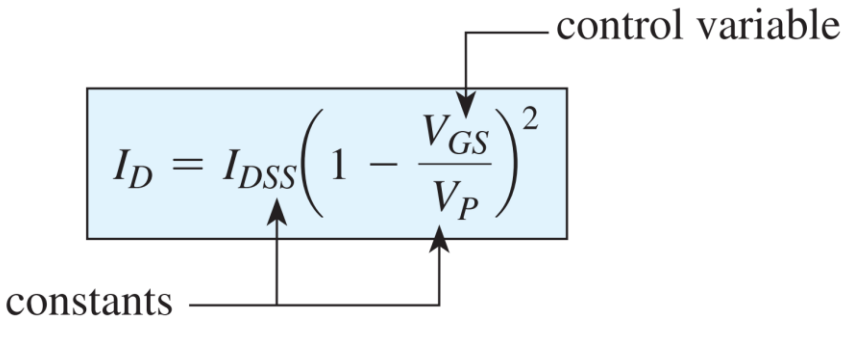
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

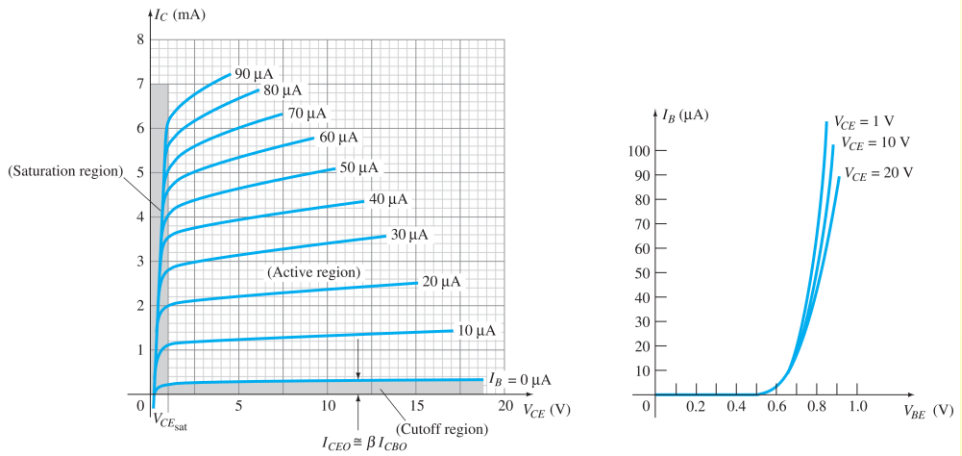
where I_{DSS} = saturation drain current
V_P = pinch-off voltage (or $V_{GS(off)}$)

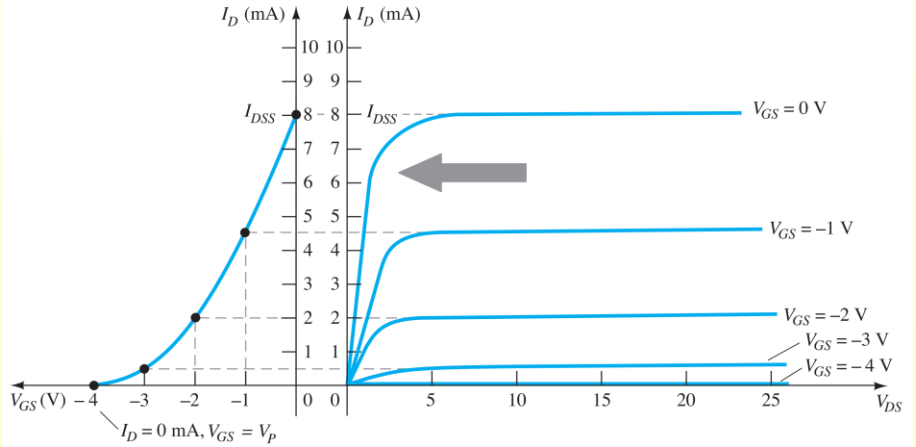


BJT vs. JFET


control variable
$I_C = f(I_B) = \beta I_B$
constant


control variable
$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$
constants


I_C (mA)
90 μA
80 μA
70 μA
60 μA
50 μA
40 μA
30 μA
20 μA
10 μA
$I_B = 0$ μA
(Saturation region)
(Active region)
(Cutoff region)
$V_{CE_{sat}}$
$I_{CEO} \cong \beta I_{CBO}$
V_{CE} (V)
I_B (μA)
$V_{CE} = 1$ V
$V_{CE} = 10$ V
$V_{CE} = 20$ V
V_{BE} (V)

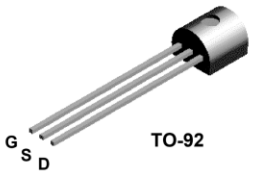

I_D (mA)
I_D (mA)
I_{DSS}
I_{DSS}
$V_{GS} = 0$ V
$V_{GS} = -1$ V
$V_{GS} = -2$ V
$V_{GS} = -3$ V
$V_{GS} = -4$ V
V_{GS} (V)
$I_D = 0$ mA, $V_{GS} = V_P$
V_{DS}

JFET
Specification Sheet

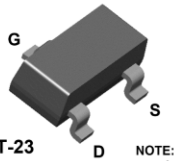
FAIRCHILD
SEMICONDUCTOR™

2N5457
2N5458
2N5459

MMBF5457
MMBF5458
MMBF5459



TO-92



SOT-23
Mark: 6D / 61S / 6L

NOTE: Source & Drain are interchangeable

N-Channel General Purpose Amplifier

This device is a low level audio amplifier and switching transistors, and can be used for analog switching applications. Sourced from Process 55.

Absolute Maximum Ratings*

TA = 25°C unless otherwise noted

Symbol	Parameter	Value	Units
V_{DG}	Drain-Gate Voltage	25	V
V_{GS}	Gate-Source Voltage	- 25	V
I_{GF}	Forward Gate Current	10	mA
T_J, T_{stg}	Operating and Storage Junction Temperature Range	-55 to +150	°C

2N5457 / 5458 / 5459 / MMBF5457 / 5458 / 5459

N-Channel General Purpose Amplifier
(continued)

Electrical Characteristics

TA = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
OFF CHARACTERISTICS							
$V_{(BR)GSS}$	Gate-Source Breakdown Voltage	I_G = 10 µA, V_{DS} = 0		- 25			V
I_{GSS}	Gate Reverse Current	V_{GS} = -15 V, V_{DS} = 0				- 1.0	nA
		V_{GS} = -15 V, V_{DS} = 0, T_A = 100°C				- 200	nA
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 15 V, I_D = 10 nA	**5457**	- 0.5		- 6.0	V
			5458	- 1.0		- 7.0	V
			5459	- 2.0		- 8.0	V
V_{GS}	Gate-Source Voltage	V_{DS} = 15 V, I_D = 100 µA	**5457**		- 2.5		V
		V_{DS} = 15 V, I_D = 200 µA	**5458**		- 3.5		V
		V_{DS} = 15 V, I_D = 400 µA	**5459**		- 4.5		V
ON CHARACTERISTICS							
I_{DSS}	Zero-Gate Voltage Drain Current*	V_{DS} = 15 V, V_{GS} = 0	**5457**	1.0	3.0	5.0	mA
			5458	2.0	6.0	9.0	mA
			5459	4.0	9.0	16	mA
SMALL SIGNAL CHARACTERISTICS							
g_{fs}	Forward Transfer Conductance*	V_{DS} = 15 V, V_{GS} = 0, f = 1.0 kHz					
			5457	1000		5000	µmhos
			5458	1500		5500	µmhos
			5459	2000		6000	µmhos
g_{os}	Output Conductance*	V_{DS} = 15 V, V_{GS} = 0, f = 1.0 kHz			10	50	µmhos
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0, f = 1.0 MHz			4.5	7.0	pF
C_{rss}	Reverse Transfer Capacitance	V_{DS} = 15 V, V_{GS} = 0, f = 1.0 MHz			1.5	3.0	pF
NF	Noise Figure	V_{DS} = 15 V, V_{GS} = 0, f = 1.0 kHz, R_G = 1.0 megohm, BW = 1.0 Hz				3.0	dB

2N5457 / 5458 / 5459 / MMBF5457 / 5458 / 5459

Example

The partial datasheet for a 2N5459 JFET indicates that typically I_{DSS} = 9 mA and $V_{GS(off)}$ = -8 V (maximum). Using these values, determine the drain current for VGS = 0 V, -1 V, and -4 V.

For $V_{GS} = 0$ V,

$$I_D = I_{DSS} = \mathbf{9\,mA}$$

For $V_{GS} = -1$ V,

$$I_D \cong I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 = (9\,\text{mA})\left(1 - \frac{-1\,\text{V}}{-8\,\text{V}}\right)^2$$

$$= (9\,\text{mA})(1 - 0.125)^2 = (9\,\text{mA})(0.766) = \mathbf{6.89\,mA}$$

For $V_{GS} = -4$ V,

$$I_D \cong (9\,\text{mA})\left(1 - \frac{-4\,\text{V}}{-8\,\text{V}}\right)^2 = (9\,\text{mA})(1 - 0.5)^2 = (9\,\text{mA})(0.25) = \mathbf{2.25\,mA}$$

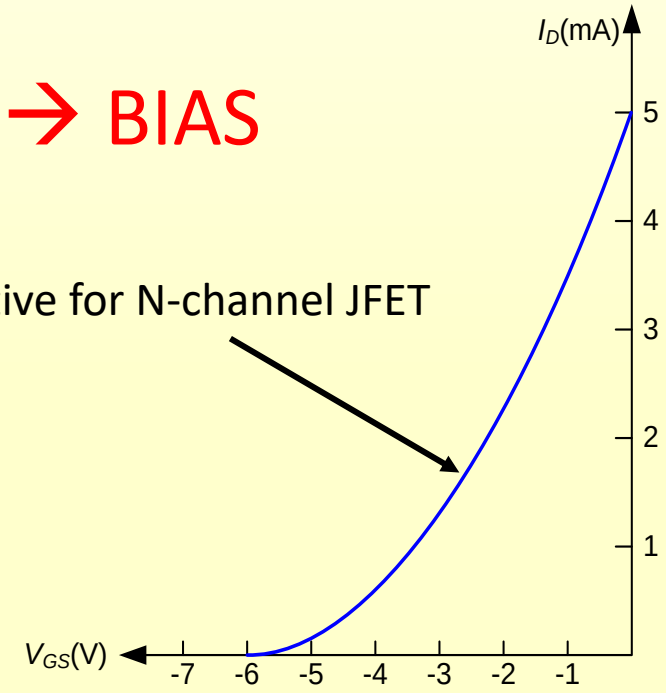
JFET Biasing Circuits

- Gate bias (Fixed bias) circuit
- Self bias circuit
- Voltage-divider bias circuit

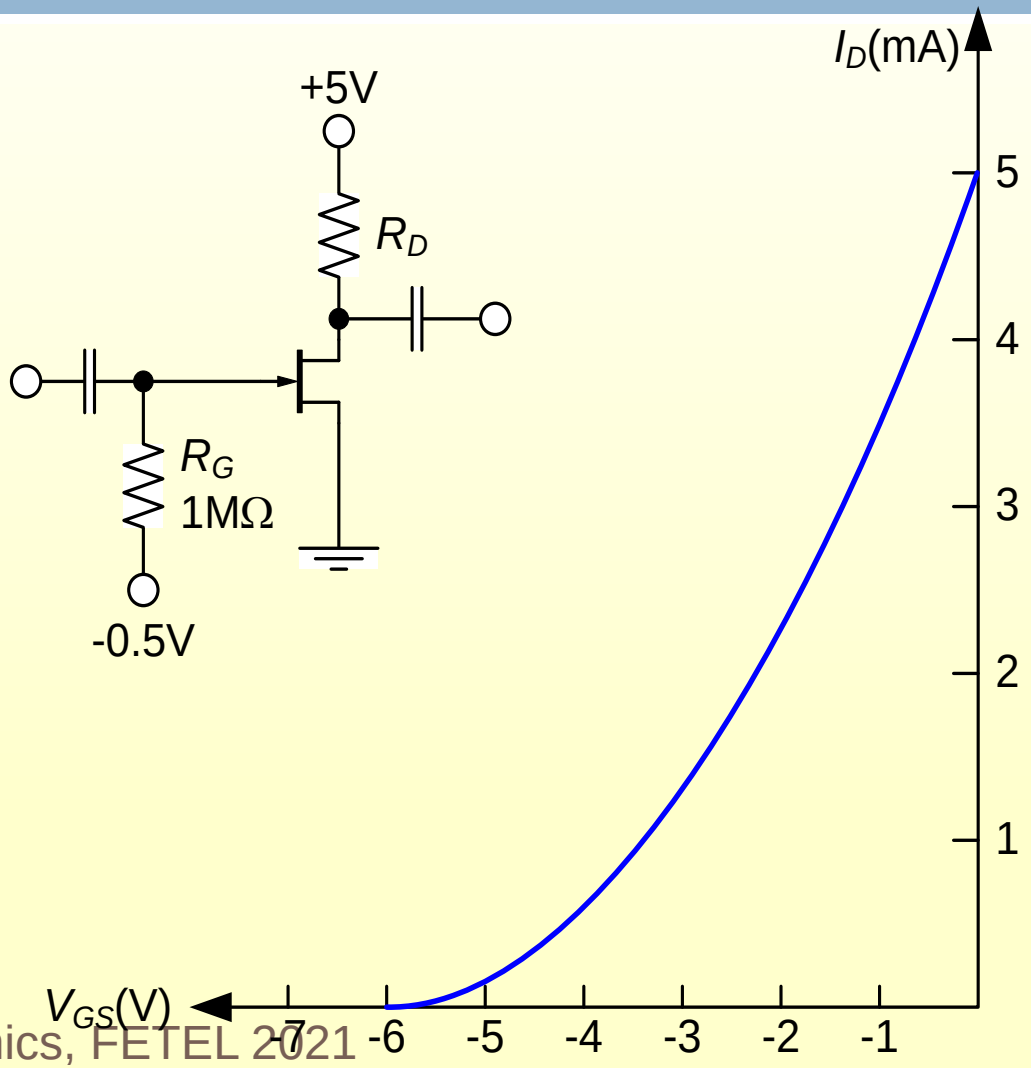
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

V_{GS} =???? → BIAS

V_{GS} must be negative for N-channel JFET

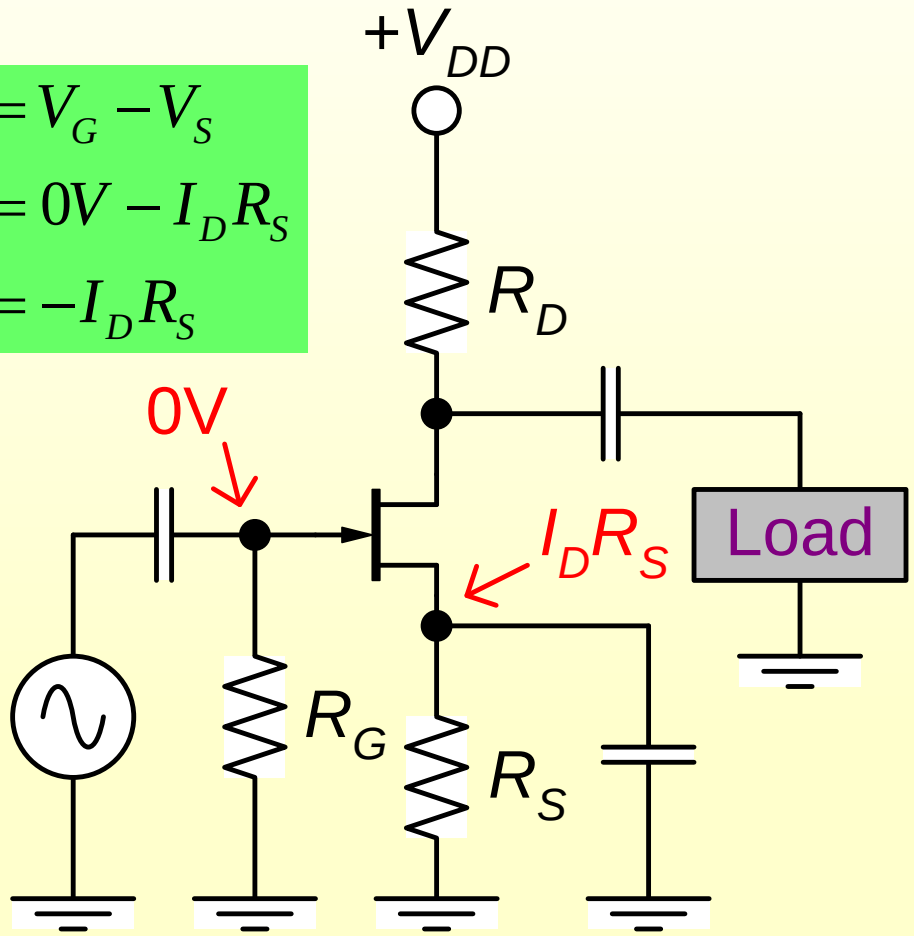


Gate Bias (Fixed bias)

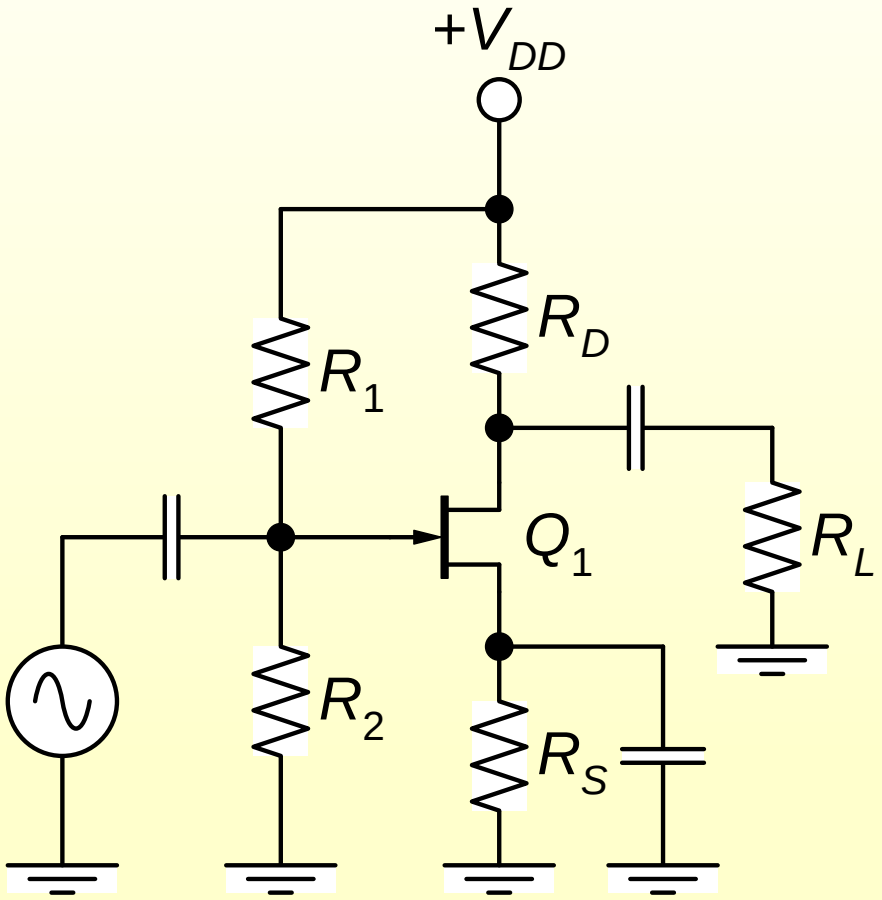


Self bias circuit.

$$V_{GS} = V_G - V_S$$
$$= 0V - I_D R_S$$
$$= -I_D R_S$$



Voltage-divider bias.



$$V_G = V_{DD}\frac{R_2}{R_1 + R_2}$$

$$I_D = \frac{V_S}{R_S} = \frac{V_G - V_{GS}}{R_S}$$

$$\therefore I_D\big|_{V_{GS}=0} = \frac{V_G}{R_S}$$

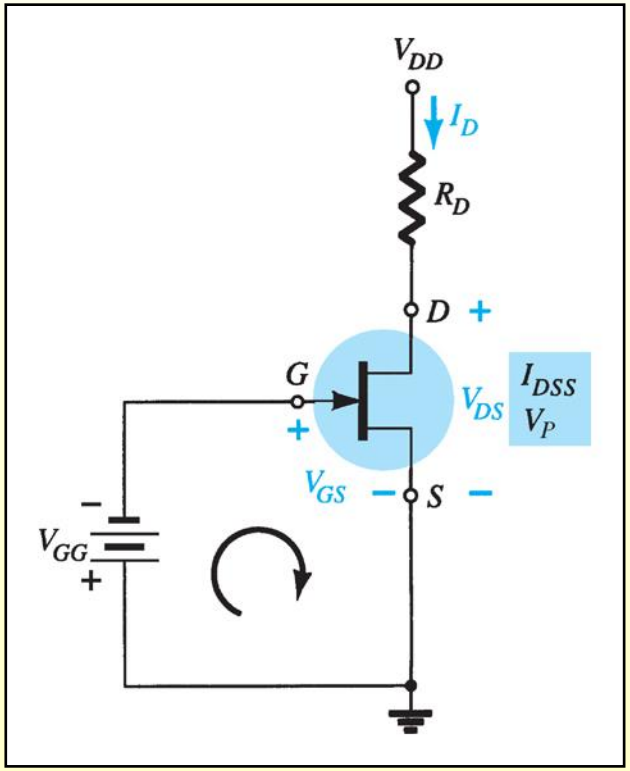
$$\therefore V_{GS}\big|_{I_D=0} = V_G$$

JFET Biasing:

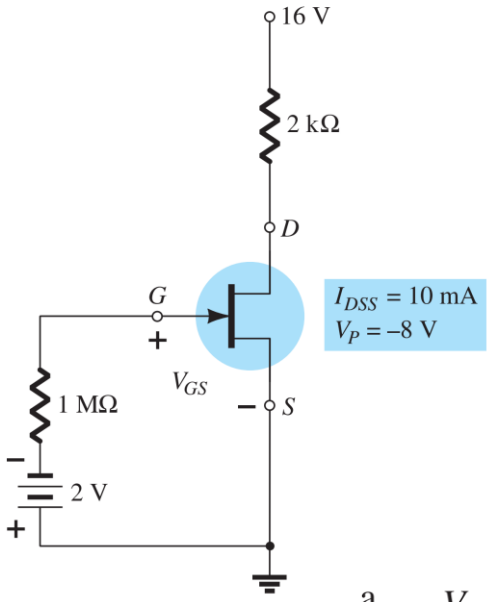
Gate bias/Fixed Bias Configuration

$$V_{DS} = V_{DD} - I_D R_D$$
$$V_S = 0\,\text{V}$$
$$V_C = V_{DS}$$
$$V = V_{GS}$$
$$V_{GS} = -V_{GG}$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$



Example



a. V_{GS_Q}.
b. I_{D_Q}.
c. V_{DS}.
d. V_D.
e. V_G.
f. V_S.

Mathematical Approach

a. $V_{GS_Q} = -V_{GG} = \mathbf{-2\ V}$

b. $I_{D_Q} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 10\text{ mA}\left(1 - \frac{-2\text{ V}}{-8\text{ V}}\right)^2$
$= 10\text{ mA}(1 - 0.25)^2 = 10\text{ mA}(0.75)^2 = 10\text{ mA}(0.5625)$
$= \mathbf{5.625\ mA}$

c. $V_{DS} = V_{DD} - I_D R_D = 16\text{ V} - (5.625\text{ mA})(2\text{ k}\Omega)$
$= 16\text{ V} - 11.25\text{ V} = \mathbf{4.75\ V}$

d. $V_D = V_{DS} = \mathbf{4.75\ V}$

e. $V_G = V_{GS} = \mathbf{-2\ V}$

f. $V_S = \mathbf{0\ V}$

Graphical Approach

a. $V_{GS_Q} = -V_{GG} = \mathbf{-2\ V}$

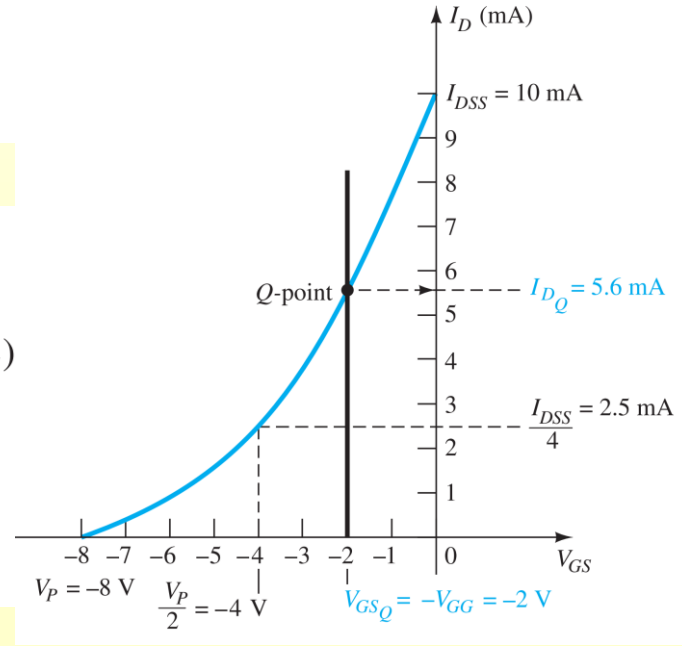
b. $I_{D_Q} = \mathbf{5.6\ mA}$

c. $V_{DS} = V_{DD} - I_D R_D = 16\text{ V} - (5.6\text{ mA})(2\text{ k}\Omega)$
$= 16\text{ V} - 11.2\text{ V} = \mathbf{4.8\ V}$

d. $V_D = V_{DS} = \mathbf{4.8\ V}$

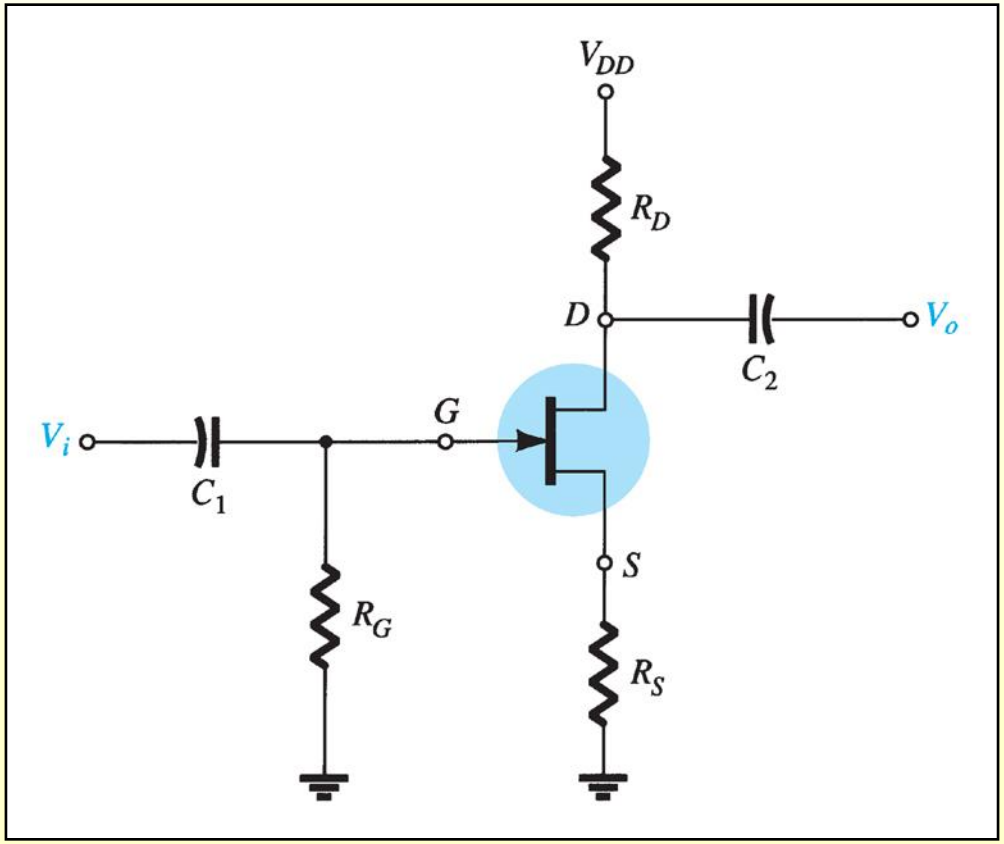
e. $V_G = V_{GS} = \mathbf{-2\ V}$

f. $V_S = \mathbf{0\ V}$



JFET Biasing:

Self-Bias Configuration



JFET Biasing:

Self-Bias Calculations

Graphical calculations

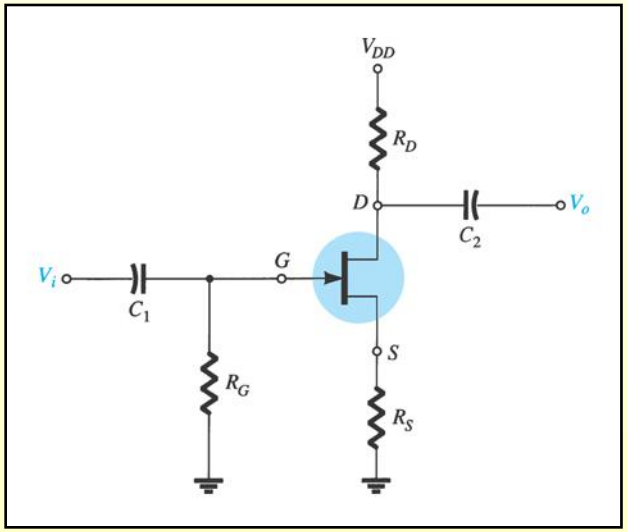
$$V_{GS} = -I_D R_S$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

1. Select a value of $I_D < I_{DSS}$ and use the component value of R_S to calculate V_{GS}. Plot the point identified by I_D and V_{GS} and draw a line from the origin of the axis to this point.

2. Plot the transfer curve using I_{DSS} and V_P ($V_P = |V_{GSoff}|$ on spec sheets) and a few points such as $V_{GS} = V_P / 4$ and $V_{GS} = V_P / 2$ etc.

The Q-point is located where the first line intersects the transfer curve. Using the value of I_D at the Q-point (I_{DQ}):



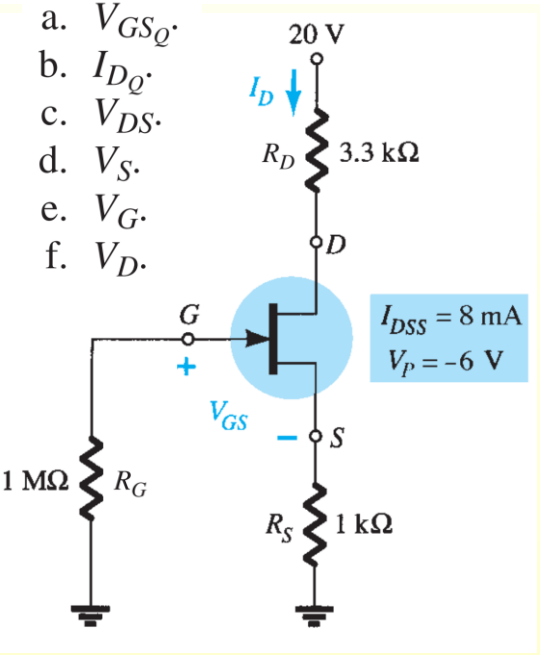
$$V_{DS} = V_{DD} - I_D(R_S + R_D)$$

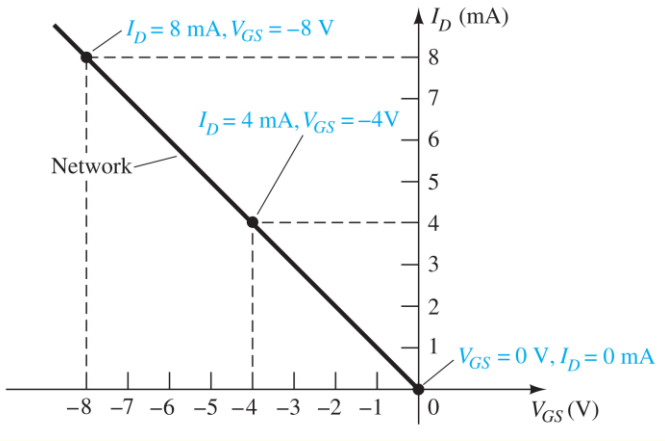
$$V_S = I_D R_S$$

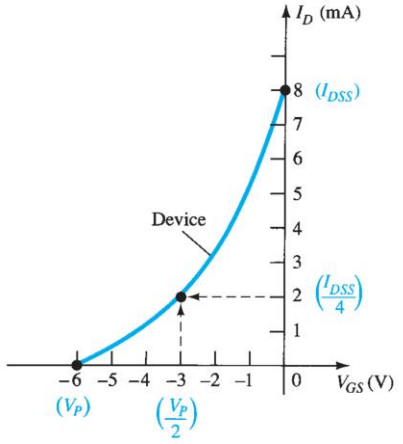
$$V_D = V_{DS} + V_S = V_{DD} - V_{RD}$$

Example

a. V_{GS_Q}.
b. I_{D_Q}.
c. V_{DS}.
d. V_S.
e. V_G.
f. V_D.







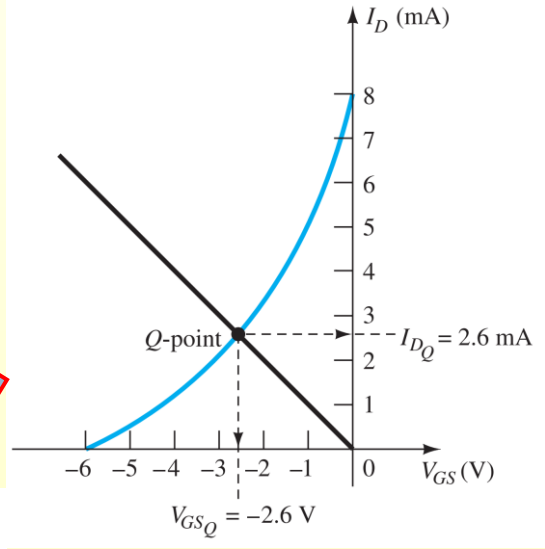
$$V_{GS} = -I_D R_S$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= I_{DSS}\left(1 - \frac{-I_D R_S}{V_P}\right)^2$$

$$I_D = I_{DSS}\left(1 + \frac{I_D R_S}{V_P}\right)^2$$

$$V_{GS_Q} = -2.6\ \text{V}$$



b. At the quiescent point

$$I_{D_Q} = \mathbf{2.6\ mA}$$

c. $$V_{DS} = V_{DD} - I_D(R_S + R_D)$$
$$= 20\ \text{V} - (2.6\ \text{mA})(1\ \text{k}\Omega + 3.3\ \text{k}\Omega)$$
$$= 20\ \text{V} - 11.18\ \text{V}$$
$$= \mathbf{8.82\ V}$$

d. $V_S = I_D R_S$
$= (2.6\ \text{mA})(1\ \text{k}\Omega)$
$= \mathbf{2.6\ V}$

e. $V_G = \mathbf{0\ V}$

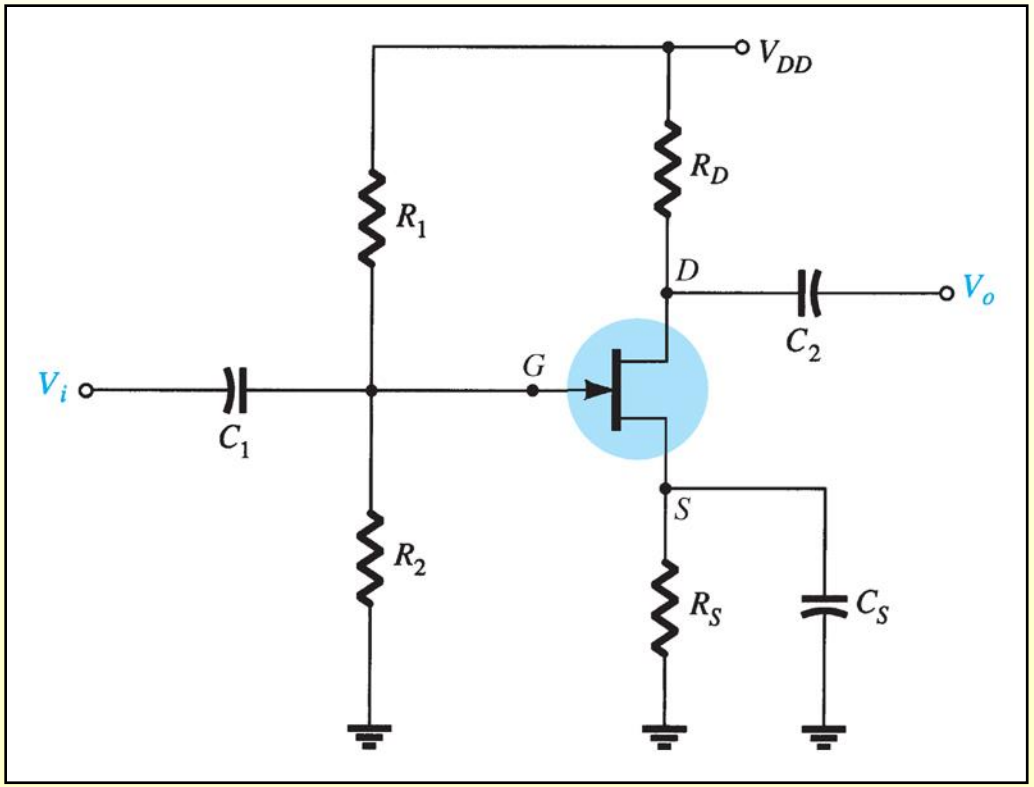
f. $V_D = V_{DS} + V_S = 8.82\ \text{V} + 2.6\ \text{V} = \mathbf{11.42\ V}$
$V_D = V_{DD} - I_D R_D = 20\ \text{V} - (2.6\ \text{mA})(3.3\ \text{k}\Omega) = \mathbf{11.42\ V}$

JFET Biasing:

Voltage-Divider Bias

$I_G = 0$ A

I_D responds to changes in V_{GS}.



JFET Biasing:

Voltage-Divider Bias Calculations

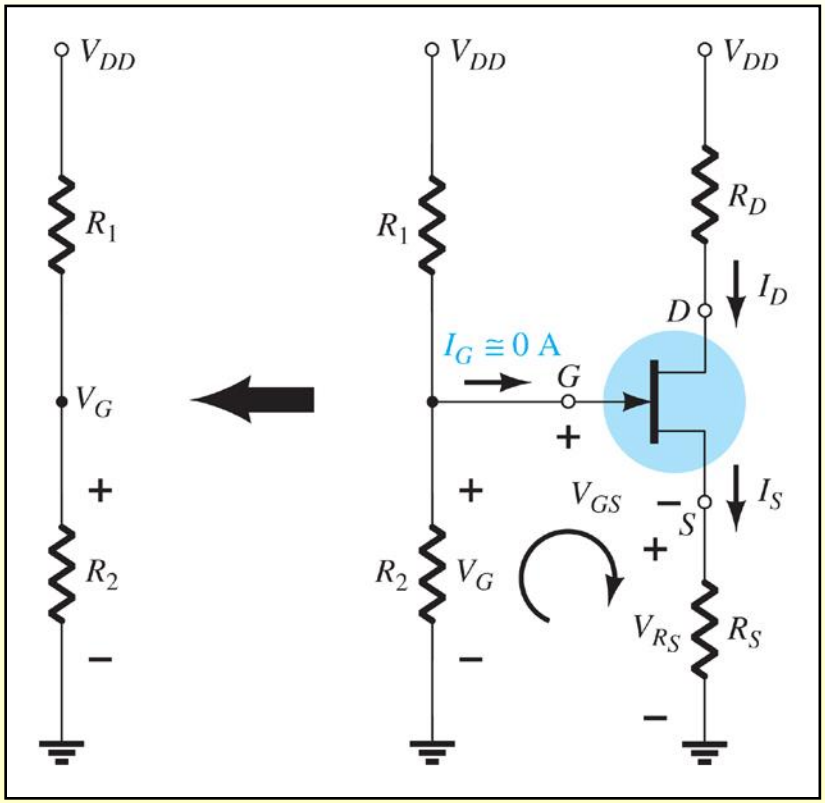
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

V_G is equal to the voltage across divider resistor R_2:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

Using Kirchhoff's Law:

$$V_{GS} = V_G - I_D R_S$$



The Q-point is established by plotting a line that intersects the transfer curve.

JFET Biasing:

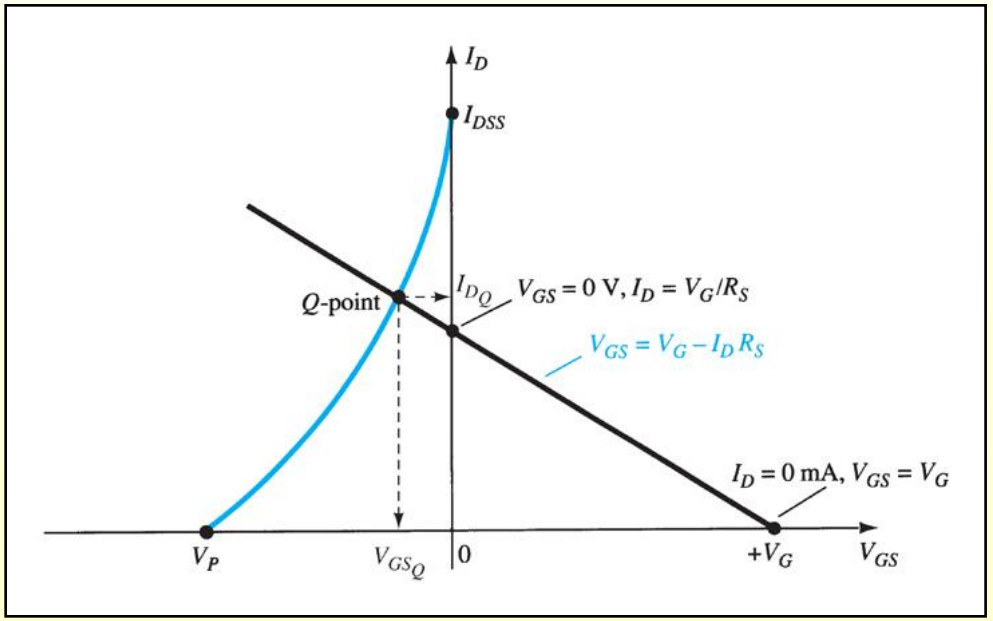
Voltage-Divider Q-Point

Plot the line that is defined by these two points:

$V_{GS} = V_G$, $I_D = 0$ A

$V_{GS} = 0$ V, $I_D = V_G / R_S$

Plot the transfer curve by plotting I_{DSS}, V_P and the calculated values of I_D



The Q-point is located where the line intersects the transfer curve

JFET Biasing:

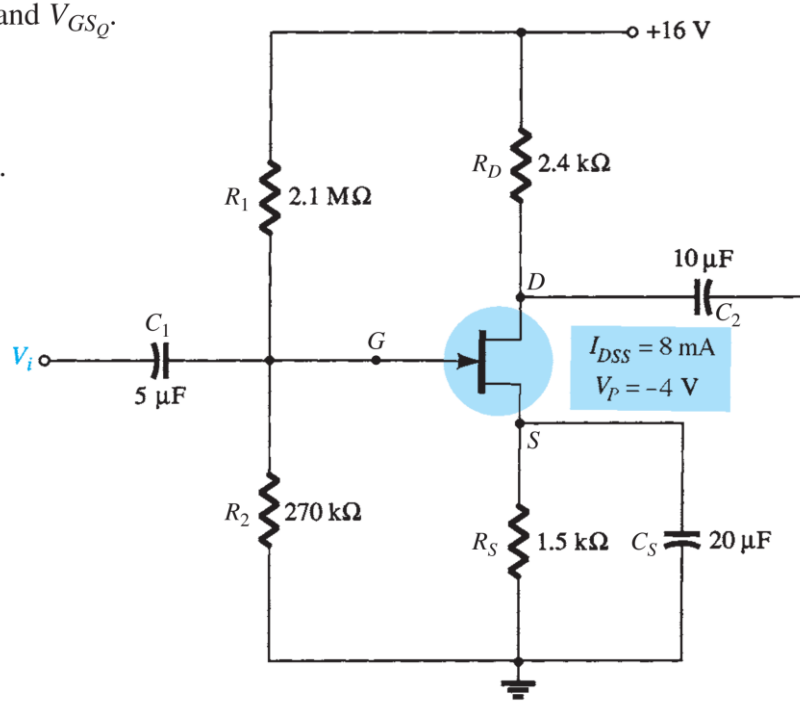
Voltage-Divider Bias Calculations

Using the value of I_D at the Q-point, solve for the other values in the voltage-divider bias circuit:

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$
$$V_D = V_{DD} - I_D R_D$$
$$V_S = I_D R_S$$

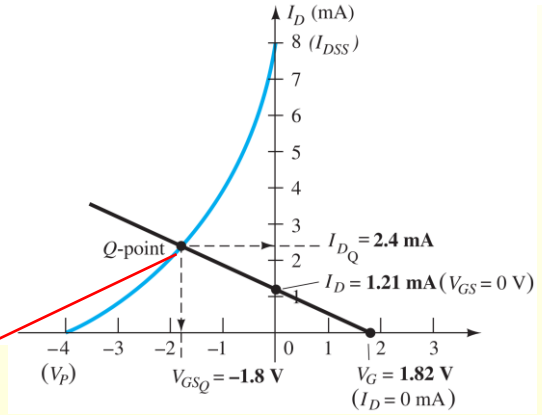
Example

a. I_{D_Q} and V_{GS_Q}.
b. V_D.
c. V_S.
d. V_{DS}.
e. V_{DG}.



$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} = \frac{(270\,\text{k}\Omega)(16\,\text{V})}{2.1\,\text{M}\Omega + 0.27\,\text{M}\Omega} = 1.82\,\text{V}$$

$$V_{GS} = V_G - I_D R_S = 1.82\,\text{V} - I_D(1.5\,\text{k}\Omega)$$



Determining the Q-point

$$I_{D_Q} = \mathbf{2.4\,mA}$$
$$V_{GS_Q} = \mathbf{-1.8\,V}$$

b. $V_D = V_{DD} - I_D R_D = 16\,\text{V} - (2.4\,\text{mA})(2.4\,\text{k}\Omega) = \mathbf{10.24\,V}$

c. $V_S = I_D R_S = (2.4\,\text{mA})(1.5\,\text{k}\Omega) = \mathbf{3.6\,V}$

d. $V_{DS} = V_{DD} - I_D(R_D + R_S) = 16\,\text{V} - (2.4\,\text{mA})(2.4\,\text{k}\Omega + 1.5\,\text{k}\Omega) = \mathbf{6.64\,V}$

or $V_{DS} = V_D - V_S = 10.24\,\text{V} - 3.6\,\text{V} = \mathbf{6.64\,V}$

$V_{DG} = V_D - V_G = 10.24\,\text{V} - 1.82\,\text{V} = \mathbf{8.42\,V}$

JFET Amplifiers

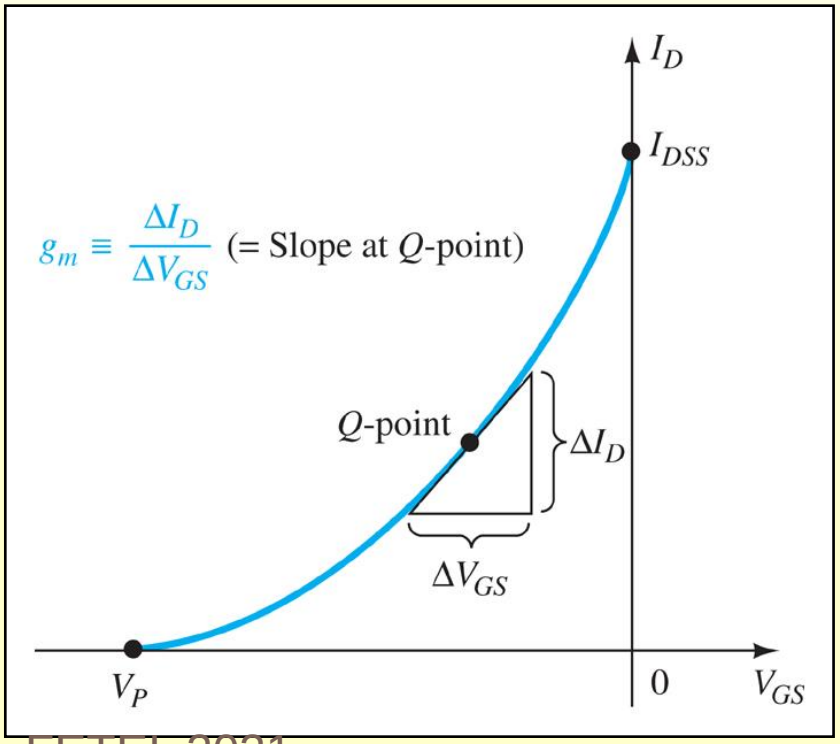
JFET amplifier:

FET Small-Signal Model

Transconductance: The ratio of a change in I_D to the corresponding change in V_{GS}

- Transconductance is denoted g_m and given by:

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$



JFET amplifier:

Mathematical Definitions of g_m

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

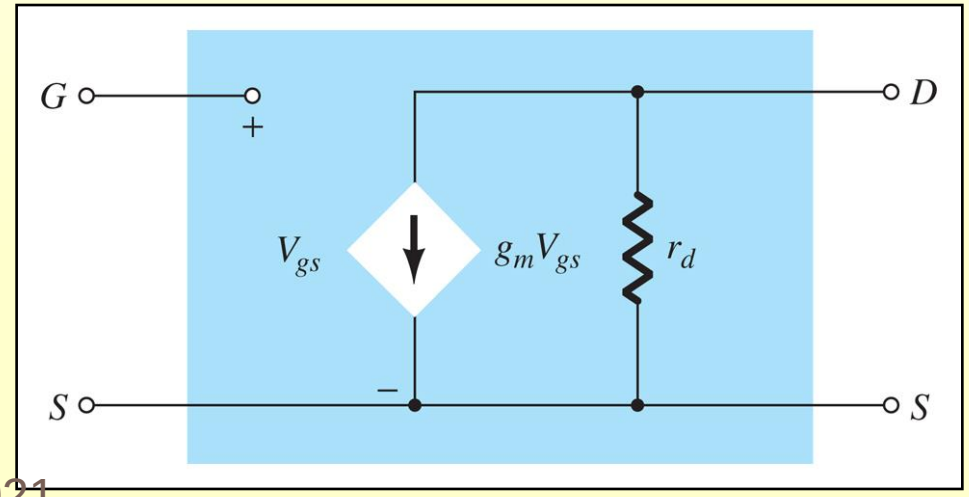
$$g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{V_{GS}}{V_P}\right]$$

For V_{GS} = 0 V

$$g_{m0} = \frac{2I_{DSS}}{|V_P|}$$

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right] = g_{m0}\sqrt{\frac{I_D}{I_{DSS}}}$$

FET AC Equivalent Circuit



JFET amplifier:

FET Impedance

Input impedance:

$$Z_i = \infty\,\Omega$$

Output Impedance:

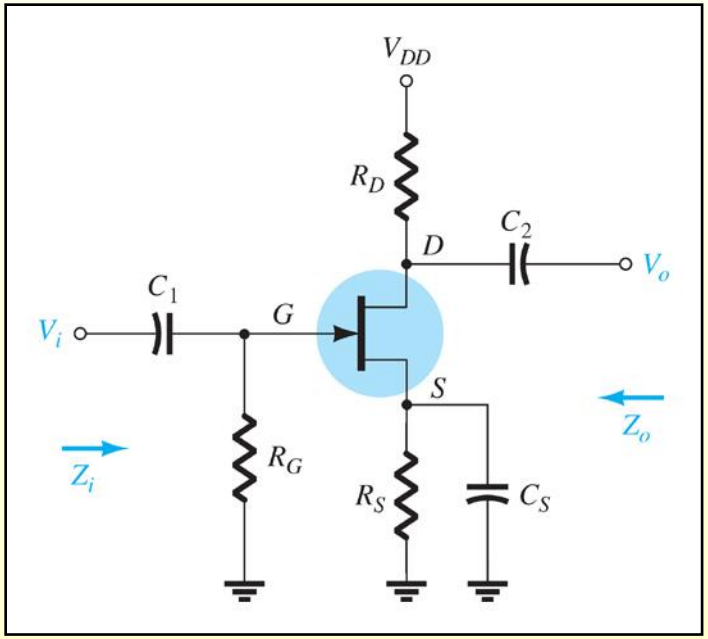
$$Z_o = r_d = \frac{1}{y_{os}} \qquad \text{where} \qquad r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}\,=\,\text{constant}}$$

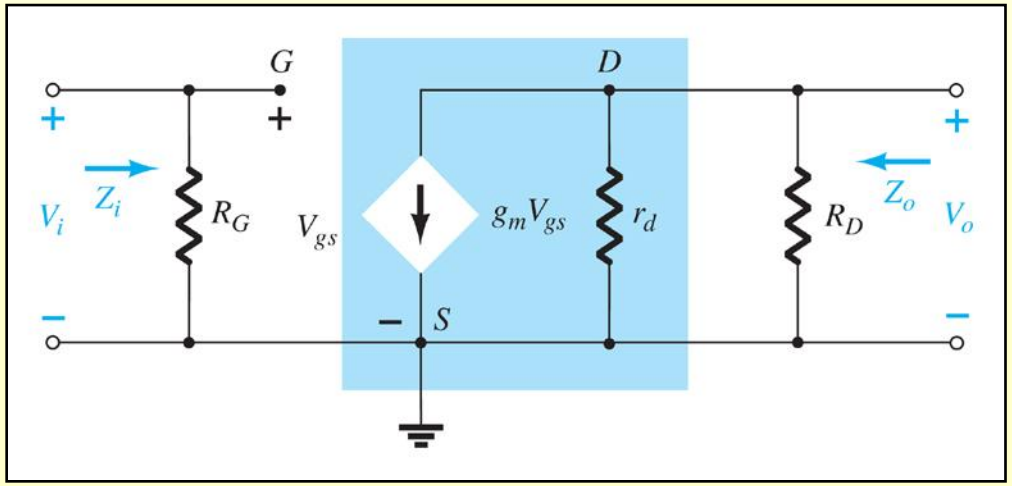
y_{os}= admittance parameter listed on FET spec sheets

JFET amplifier:

Common-Source (CS) Self-Bias

This is a common-source amplifier configuration, so the input is applied to the gate and the output is taken from the drain.





There is a 180° phase shift between input and output.

JFET amplifier:

Common-Source (CS) Self-Bias Calculation

Input impedance:

$$Z_i = R_G$$

Output impedance:

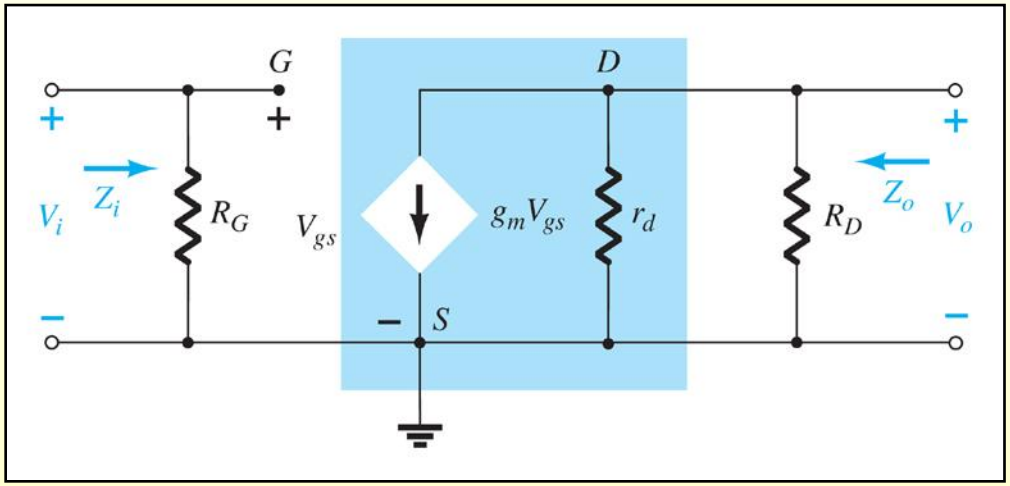
$$Z_o = r_d \| R_D$$

$$Z_o \cong R_D \Big|_{r_d \geq 10R_D}$$

Voltage gain:

$$A_v = -g_m(r_d \| R_D)$$

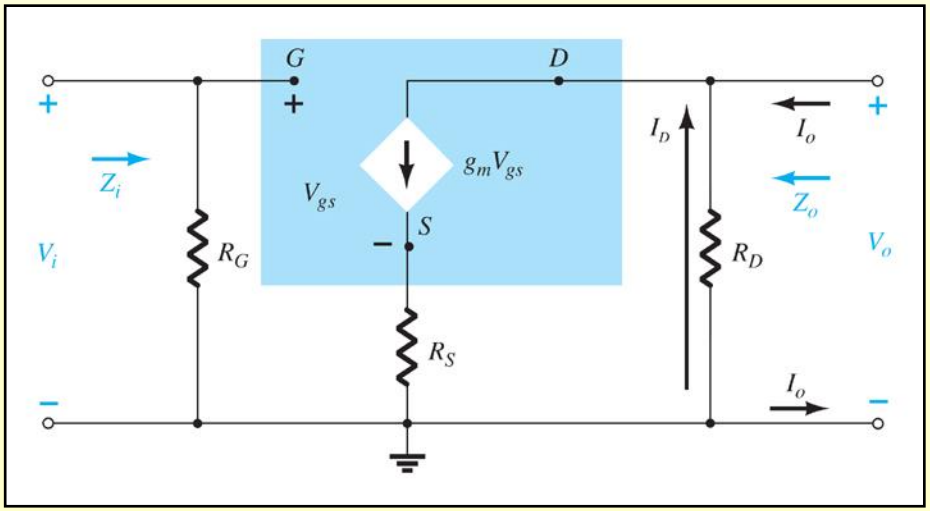
$$A_v = -g_m R_D \Big|_{r_d \geq 10R_D}$$

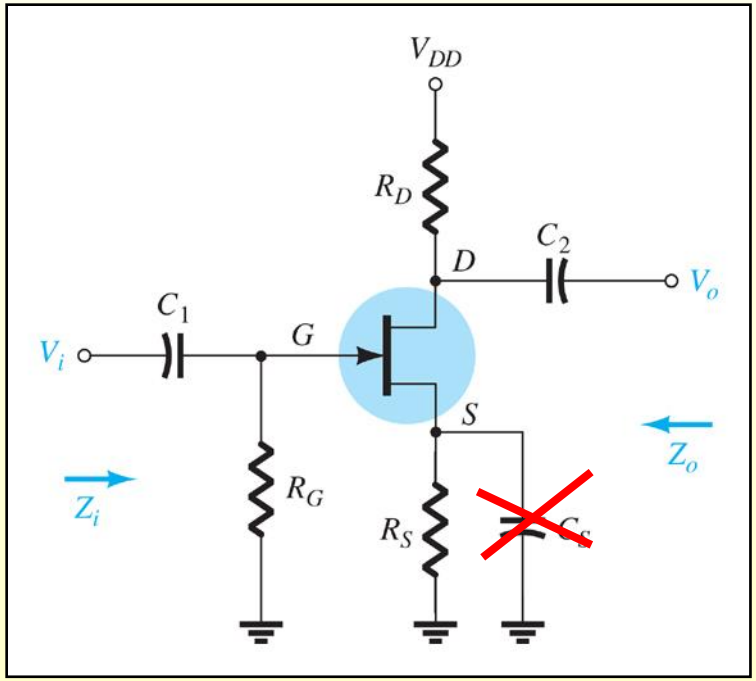


JFET amplifier:

Common-Source (CS) Self-Bias Calculation, without C_S

Removing C_s affects the gain of the circuit.





JFET amplifier:

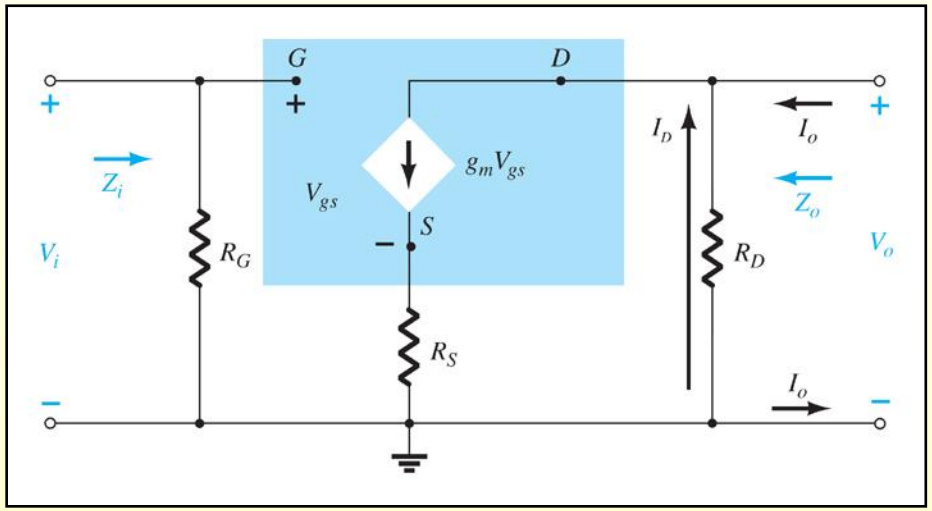
Common-Source (CS) Self-Bias Calculation, without C_S

Input impedance:

$$Z_i = R_G$$

Output impedance:

$$Z_o \cong R_D \Big|_{r_d \geq 10R_D}$$



Voltage gain:

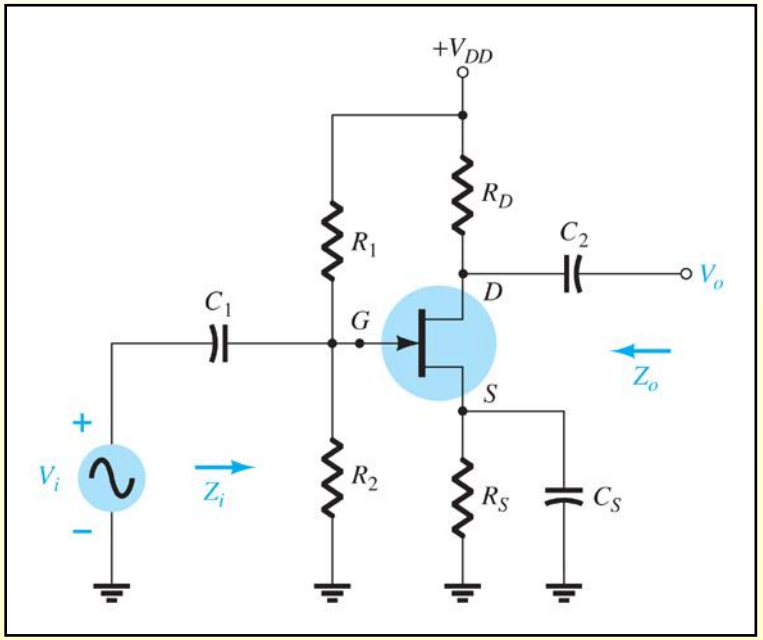
$$A_v = \frac{V_o}{V_i} = -\frac{g_m R_D}{1 + g_m R_S + \dfrac{R_D + R_S}{r_d}}$$

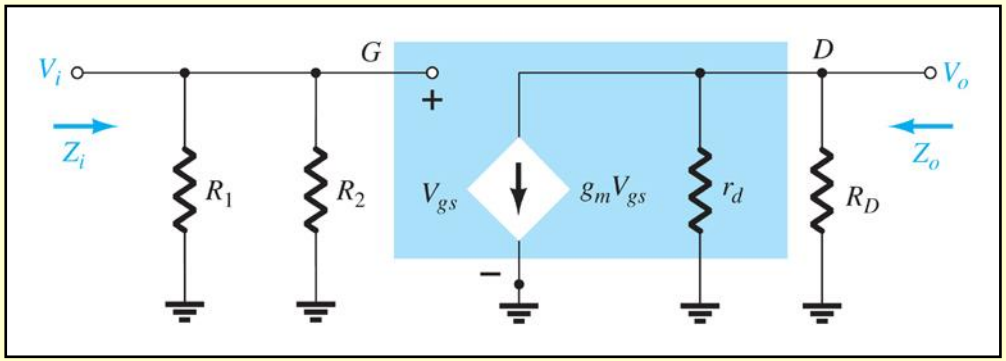
$$A_v = \frac{V_o}{V_i} = -\frac{g_m R_D}{1 + g_m R_S}\Bigg|_{r_d \geq 10(R_D + R_S)}$$

JFET amplifier:

Common-Source (CS) Voltage-Divider Bias

This is a common-source amplifier configuration, so the input is applied to the gate and the output is taken from the drain.





JFET amplifier:

Common-Source (CS) Voltage-Divider Bias

Impedances

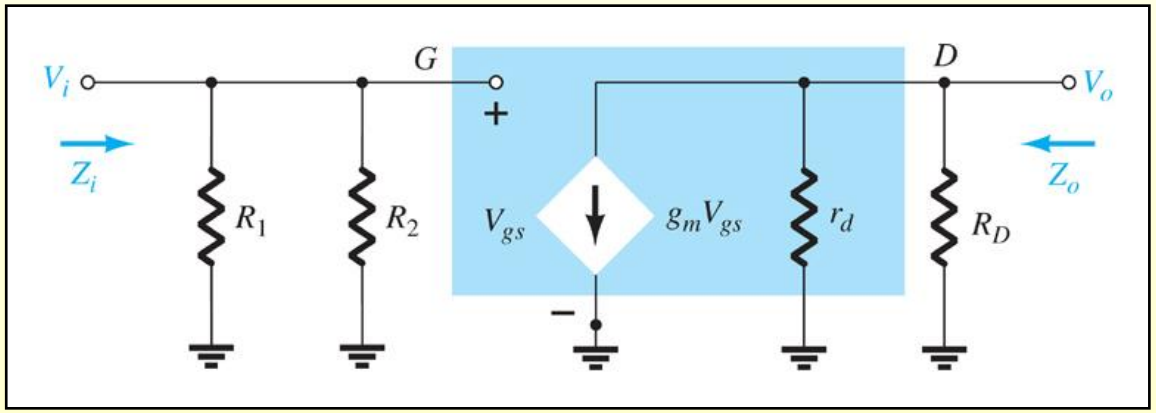
Input impedance:

$$Z_i = R_1 \| R_2$$

Output impedance:

$$Z_o = r_d \| R_D$$

$$Z_o \cong R_D \Big|_{r_d \geq 10 R_D}$$

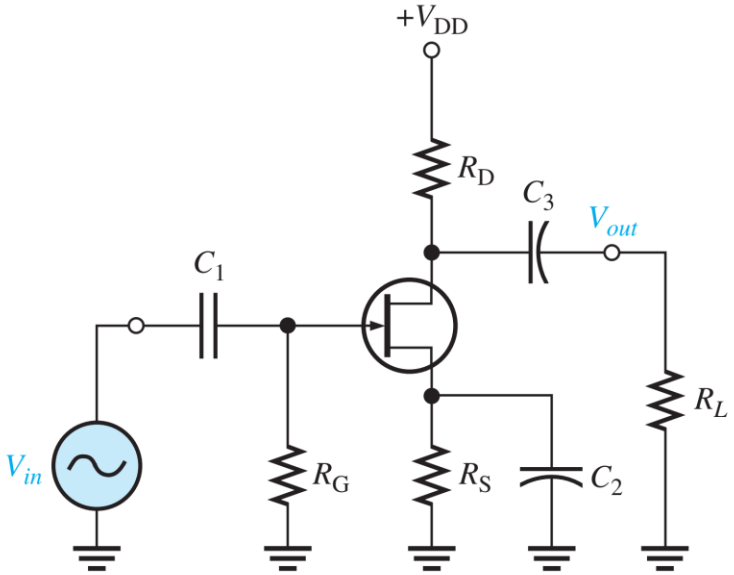


Voltage gain:

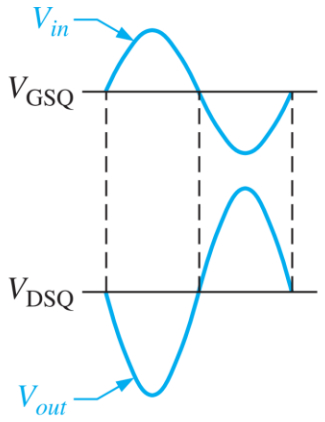
$$A_v = -g_m (r_d \| R_D)$$

$$A_v = -g_m R_D \Big|_{r_d \geq 10 R_D}$$

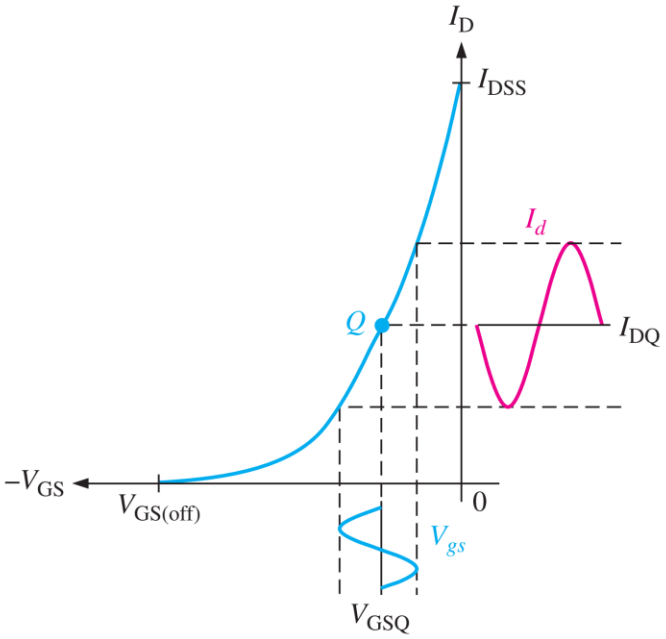
JFET amplifier

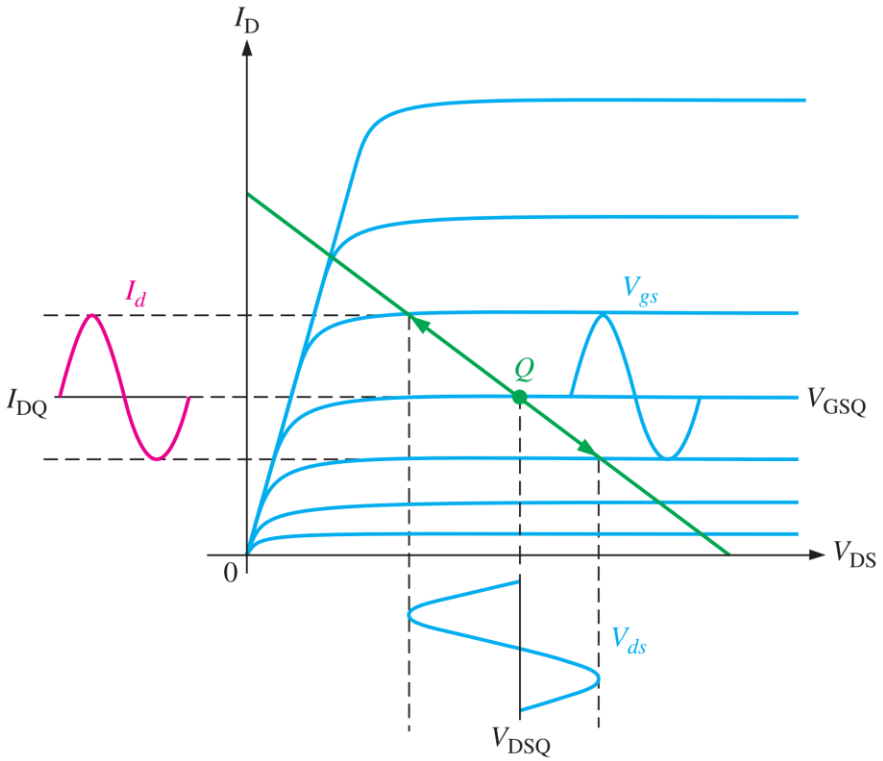


(a) Schematic



(b) Voltage waveform relationship





EXAMPLE 8.8 The self-bias configuration of Example 7.2 has an operating point defined by $V_{GS_Q} = -2.6$ V and $I_{D_Q} = 2.6$ mA, with $I_{DSS} = 8$ mA and $V_P = -6$ V. The network is redrawn as Fig. 8.20 with an applied signal V_i. The value of g_{os} is given as 20 μS.

a. Determine g_m.
b. Find r_d.
c. Find Z_i.
d. Calculate Z_o with and without the effects of r_d. Compare the results.
e. Calculate A_v with and without the effects of r_d. Compare the results.

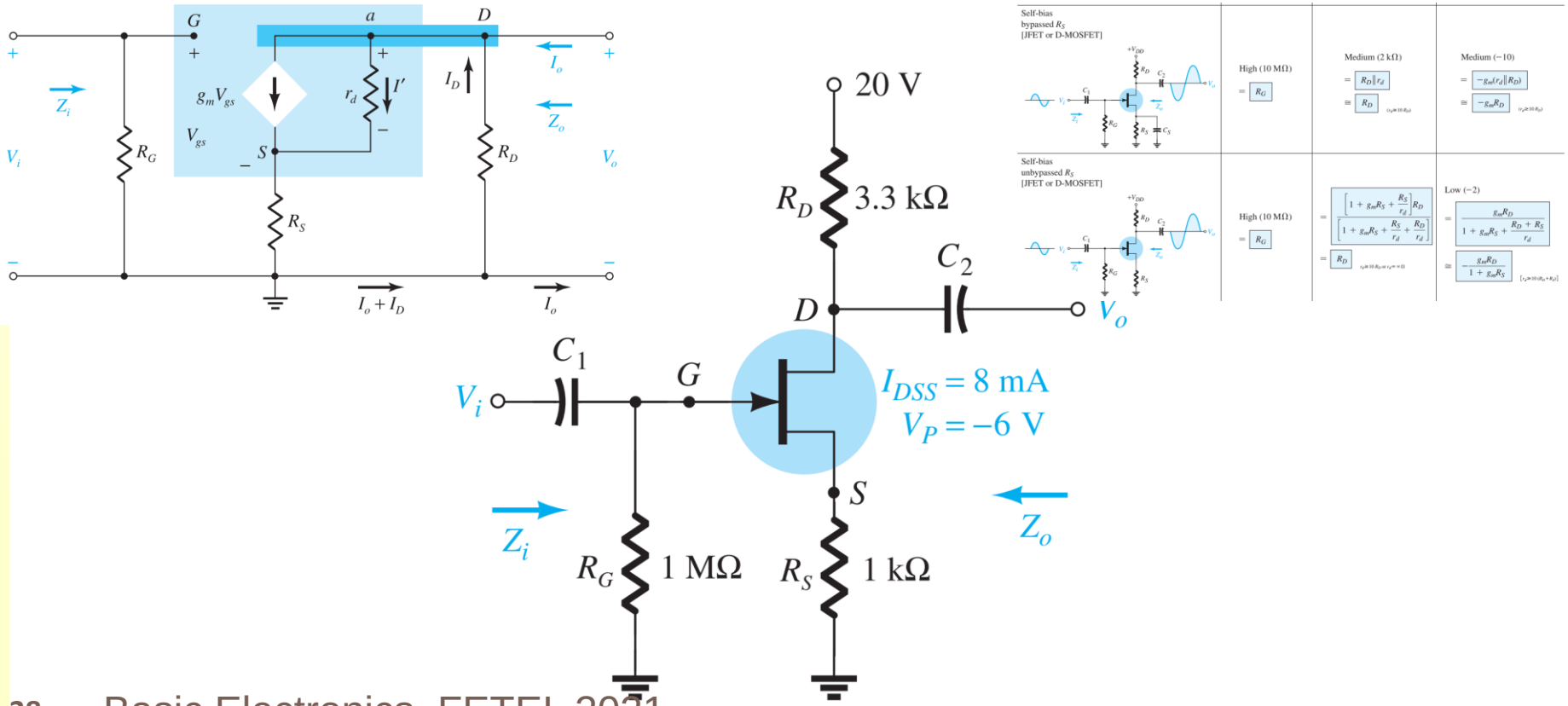


FIG. 8.20

Solution:

a. $$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(8\text{ mA})}{6\text{ V}} = 2.67\text{ mS}$$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 2.67\text{ mS}\left(1 - \frac{(-2.6\text{ V})}{(-6\text{ V})}\right) = \mathbf{1.51\text{ mS}}$$

b. $$r_d = \frac{1}{y_{os}} = \frac{1}{20\ \mu\text{S}} = \mathbf{50\ k\Omega}$$

c. $Z_i = R_G = \mathbf{1\ M\Omega}$

d. With r_d,

$$r_d = 50\text{ k}\Omega > 10R_D = 33\text{ k}\Omega$$

Therefore,

$$Z_o = R_D = \mathbf{3.3\ k\Omega}$$

If $r_d = \infty\,\Omega$,

$$Z_o = R_D = \mathbf{3.3\ k\Omega}$$

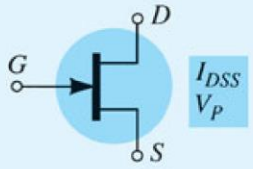
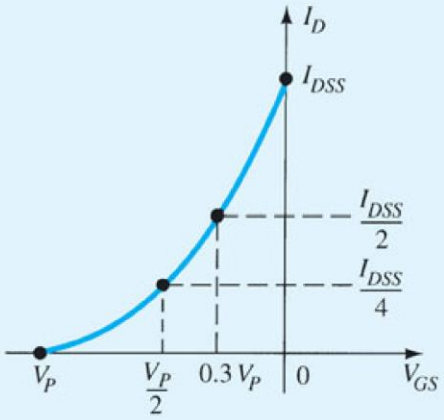
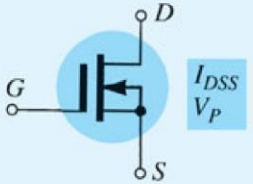
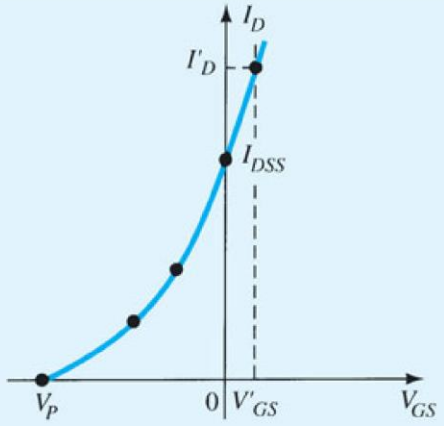
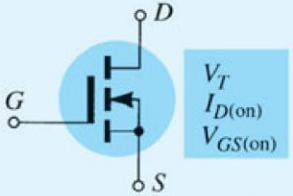
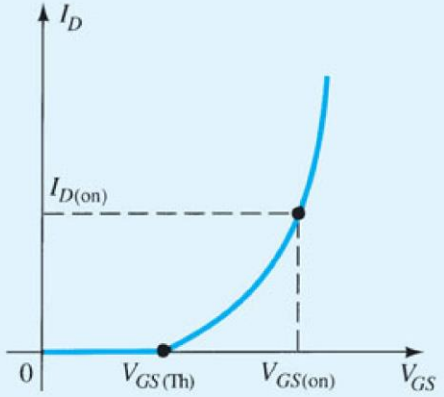
e. With r_d,

$$A_v = \frac{-g_m R_D}{1 + g_m R_S + \dfrac{R_D + R_S}{r_d}} = \frac{-(1.51\text{ mS})(3.3\text{ k}\Omega)}{1 + (1.51\text{ mS})(1\text{ k}\Omega) + \dfrac{3.3\text{ k}\Omega + 1\text{ k}\Omega}{50\text{ k}\Omega}}$$

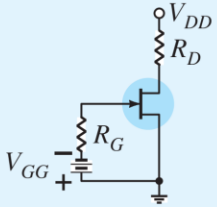
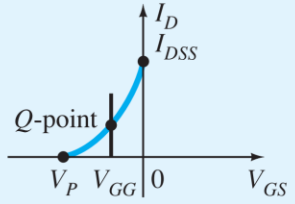
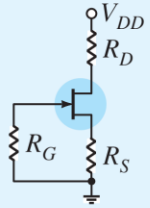
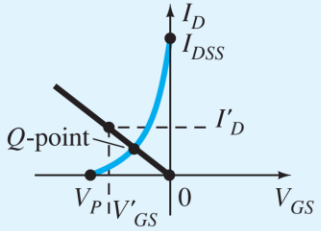
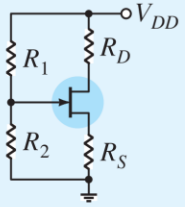
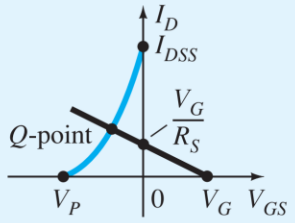
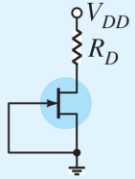
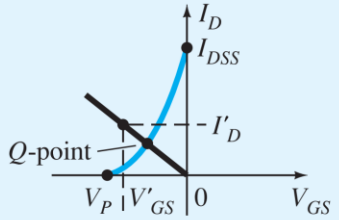
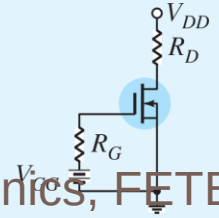
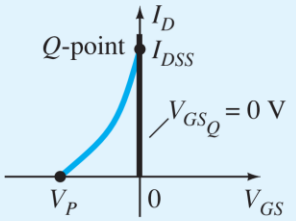
$$= \mathbf{-1.92}$$

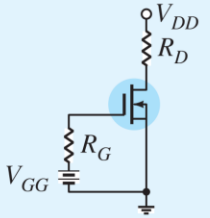
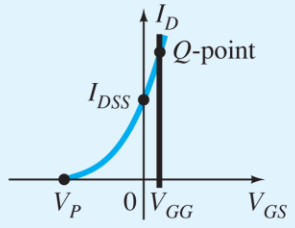
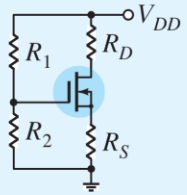
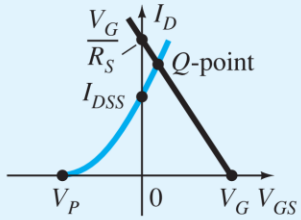
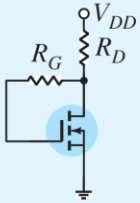
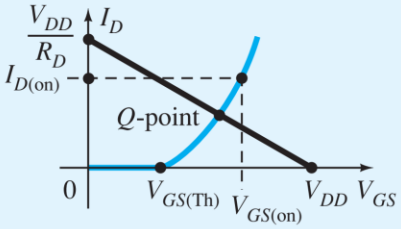
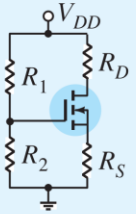
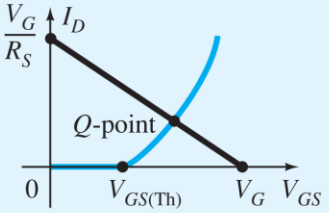
With $r_d = \infty\,\Omega$ (open-circuit equivalence),

$$A_v = \frac{-g_m R_D}{1 + g_m R_S} = \frac{-(1.51\text{ mS})(3.3\text{ k}\Omega)}{1 + (1.51\text{ mS})(1\text{ k}\Omega)} = \mathbf{-1.98}$$

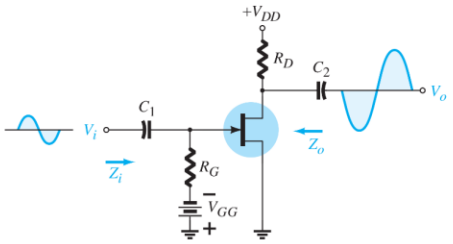
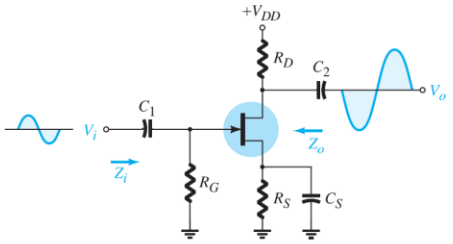
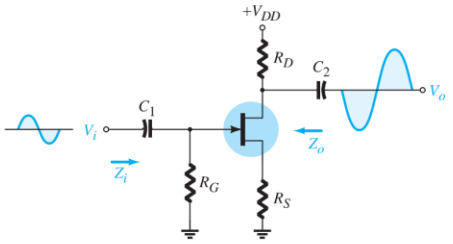
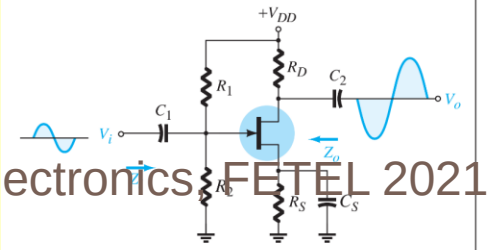
Type	Symbol and Basic Relationships	Transfer Curve	Input Resistance and Capacitance
JFET (*n*-channel)	$I_G = 0\ \text{A}, I_D = I_S$  $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$		$R_i > 100\ \text{M}\Omega$ C_i: (1 – 10) pF
MOSFET depletion type (*n*-channel)	$I_G = 0\ \text{A}, I_D = I_S$  $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$		$R_i > 10^{10}\ \Omega$ C_i: (1 – 10) pF
MOSFET enhancement type (*n*-channel)	$I_G = 0\ \text{A}, I_D = I_S$  $I_D = k\,(V_{GS} - V_{GS\,(\text{Th})})^2$ $k = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS\,(\text{Th})})^2}$		$R_i > 10^{10}\ \Omega$ C_i: (1 – 10) pF

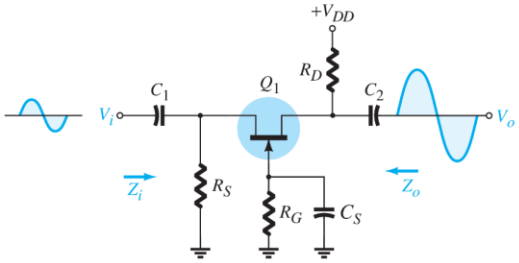
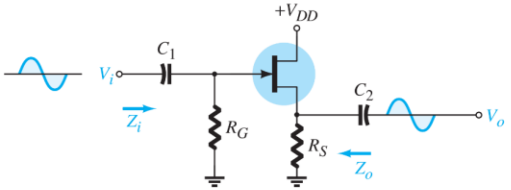
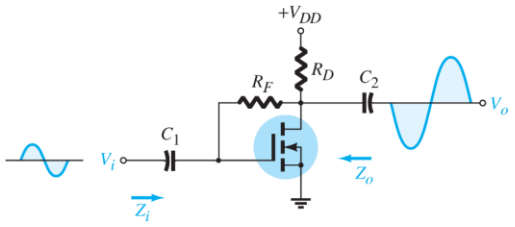
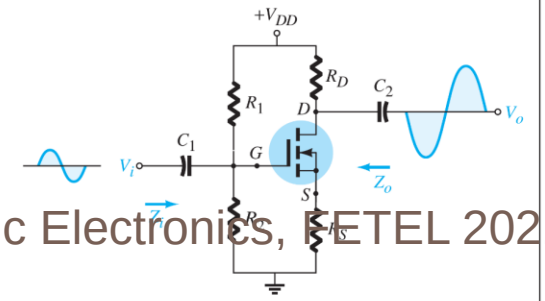
FET Bias Configurations

Type	Configuration	Pertinent Equations	Graphical Solution
JFET Fixed-bias		$V_{GS_Q} = -V_{GG}$ $V_{DS} = V_{DD} - I_D R_S$	
JFET Self-bias		$V_{GS} = -I_D R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	
JFET Voltage-divider bias		$V_G = \dfrac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_D R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	
JFET ($R_D = 0\ \Omega$)		$V_{GS} = -I_D R_S$ $V_D = V_{DD}$ $V_S = I_D R_S$ $V_{DS} = V_{DD} - I_S R_S$	
JFET Special case ($V_{GS_Q} = 0$ V)		$V_{GS_Q} = 0$ V $I_{D_Q} = I_{DSS}$	

Depletion-type MOSFET Fixed-bias (and MESFETs)		$V_{GS_Q} = +V_{GG}$ $V_{DS} = V_{DD} - I_D R_S$	
Depletion-type MOSFET Voltage-divider bias (and MESFETs)		$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_S R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	
Enhancement type MOSFET Feedback configuration (and MESFETs)		$V_{GS} = V_{DS}$ $V_{GS} = V_{DD} - I_D R_D$	
Enhancement type MOSFET Voltage-divider bias (and MESFETs)		$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_D R_S$	

Z_i, Z_o, and A_v for various FET configurations

Configuration	Z_i	Z_o	$A_v = \frac{V_o}{V_i}$
Fixed-bias [JFET or D-MOSFET] 	High (10 MΩ) $= R_G$	Medium (2 kΩ) $= R_D \| r_d$ $\cong R_D$ $(r_d \geq 10\,R_D)$	Medium (−10) $= -g_m(r_d \| R_D)$ $\cong -g_m R_D$ $(r_d \geq 10\,R_D)$
Self-bias bypassed R_S [JFET or D-MOSFET] 	High (10 MΩ) $= R_G$	Medium (2 kΩ) $= R_D \| r_d$ $\cong R_D$ $(r_d \geq 10\,R_D)$	Medium (−10) $= -g_m(r_d \| R_D)$ $\cong -g_m R_D$ $(r_d \geq 10\,R_D)$
Self-bias unbypassed R_S [JFET or D-MOSFET] 	High (10 MΩ) $= R_G$	$= \dfrac{\left[1 + g_m R_S + \frac{R_S}{r_d}\right] R_D}{\left[1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d}\right]}$ $= R_D$ $r_d \geq 10\,R_D$ or $r_d = \infty\,\Omega$	Low (−2) $= \dfrac{g_m R_D}{1 + g_m R_S + \frac{R_D + R_S}{r_d}}$ $\cong -\dfrac{g_m R_D}{1 + g_m R_S}$ $[r_d \geq 10\,(R_D + R_S)]$
Voltage-divider bias [JFET or D-MOSFET] 	High (10 MΩ) $= R_1 \| R_2$	Medium (2 kΩ) $= R_D \| r_d$ $\cong R_D$ $(r_d \geq 10\,R_D)$	Medium (−10) $= -g_m(r_d \| R_D)$ $\cong -g_m R_D$ $(r_d \geq 10\,R_D)$

Configuration	Z_i	Z_o	$A_v = \frac{V_o}{V_i}$
Common-gate [JFET or D-MOSFET] 	Low (1 kΩ) $= R_S \Vert \left[\frac{r_d + R_D}{1 + g_m r_d} \right]$ $\cong R_S \Vert \frac{1}{g_m}$ $(r_d \geq 10\, R_D)$	Medium (2 kΩ) $= R_D \Vert r_d$ $\cong R_D$ $(R_d \geq 10\, R_D)$	Medium (+10) $= \frac{g_m R_D + \frac{R_D}{r_d}}{1 + \frac{R_D}{r_d}}$ $\cong g_m R_D$ $(r_d \geq 10\, RD)$
Source-follower [JFET or D-MOSFET] 	High (10 MΩ) $= R_G$	Low (100 kΩ) $= r_d \Vert R_S \Vert 1/g_m$ $\cong R_S \Vert 1/g_m$ $(r_d \geq 10\, R_S)$	Low (<1) $= \frac{g_m (r_d \Vert R_S)}{1 + g_m (r_d \Vert R_S)}$ $\cong \frac{g_m R_S}{1 + g_m R_S}$ $(r_d \geq 10\, R_S)$
Drain-feedback bias E-MOSFET 	Medium (1 MΩ) $= \frac{R_F + r_d \Vert R_D}{1 + g_m (r_d \Vert R_D)}$ $\cong \frac{R_F}{1 + g_m R_D}$ $(r_d \geq 10\, R_D)$	Medium (2 kΩ) $= R_F \Vert r_d \Vert R_D$ $\cong R_D$ $(R_F,\, r_d \geq 10 R_D)$	Medium (−10) $= -g_m (R_F \Vert r_d \Vert R_D)$ $\cong -g_m R_D$ $(R_F,\, r_d \geq 10 R_D)$
Voltage-divider bias E-MOSFET 	Medium (1 MΩ) $= R_1 \Vert R_2$	Medium (2 kΩ) $= R_D \Vert r_d$ $\cong R_D$ $(r_d \geq 10\, R_D)$	Medium (−10) $= -g_m (r_d \Vert R_D)$ $\cong -g_m R_D$ $(r_d \geq 10\, R_D)$

Admittance is defined as

$$Y \equiv \frac{1}{Z}$$

where

Y is the admittance, measured in siemens, Dẫn nạp

Z is the impedance, measured in ohms

$$Y = G + jB$$

here

Y is the admittance, measured in siemens.

G is the conductance, measured in siemens. Độ dẫn

B is the susceptance, measured in siemens. Điện nạp