8-FET DC Biasing

The general relationships that can be applied to the dc analysis of all FET amplifiers

$$I_G \cong 0\ \text{A} \qquad [8\text{-}1]$$

$$I_D = I_S \qquad [8\text{-}2]$$

JFET & D-MOSFET, Shockley's equation is applied to relate the input & output quantities:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \qquad [8\text{-}3]$$

For enhancement-type MOSFETs, the following equation is applicable:

$$I_D = k(V_{GS} - V_T)^2 \qquad [8\text{-}4]$$

Fixed-Bias Configuration

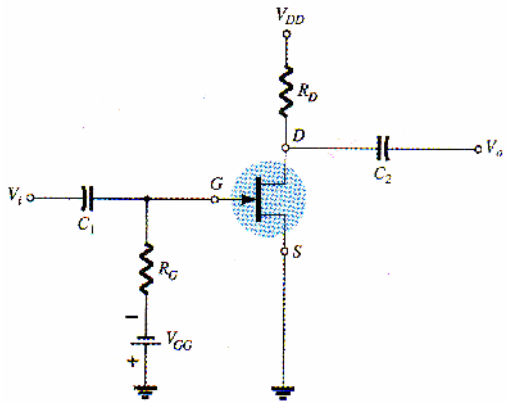


Fig8-1 Fixed-Bias Configuration

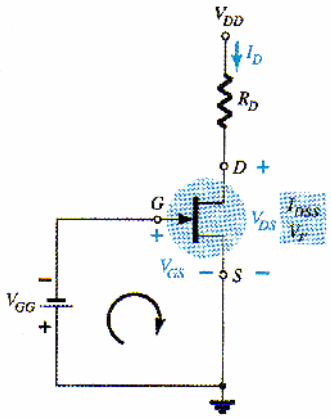


Fig8-2 Network for DC analysis

$$I_G \cong 0\ \text{A}$$

$$V_{R_G} = I_G R_G = (0\ \text{A})R_G = 0\ \text{V}$$

Replacing R_G by a short-circuit equivalent, as in fig8-2, Applying KVL will result:

$$-V_{GG} - V_{GS} = 0$$

$$V_{GS} = -V_{GG} \qquad [8\text{-}5]$$

Since V_{GG} is a fixed dc supply, V_{GS} is fixed in magnitude

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

*The fixed level of V_{GS} has been superimposed as a vertical line at **V_{GS} = - V_{GG}**. **I_D** determined at any point on the vertical line (**V_{GS}** is **- V_{GG}**).*

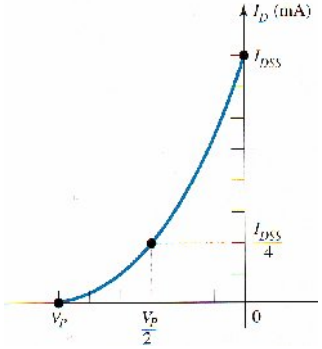


Fig8-3 plotting Shockely's equation

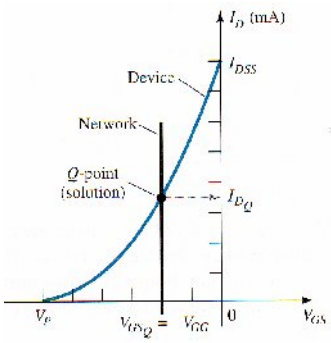
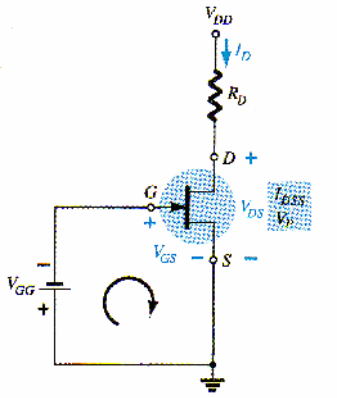


Fig8-4solution for the fixed bias configuration



$$+V_{DS} + I_D R_D - V_{DD} = 0$$

$$V_{DS} = V_{DD} - I_D R_D \qquad [8\text{-}6]$$

$$V_S = 0\ \text{V} \qquad [8\text{-}7]$$

$$V_{DS} = V_D - V_S$$

$$V_D = V_{DS} + V_S = V_{DS} + 0\ \text{V}$$

$$V_D = V_{DS} \qquad [8\text{-}8]$$

In addition, $V_{GS} = V_G - V_S$

or $V_G = V_{GS} + V_S = V_{GS} + 0\ \text{V}$

and $V_G = V_{GS} \qquad [8\text{-}9]$

Example1: *Determine the following for the network of fig8-5, (a) V_{GSQ} (b) I_{DQ} (c) V_{DS} (d) V_D (e) V_G (f) V_S*

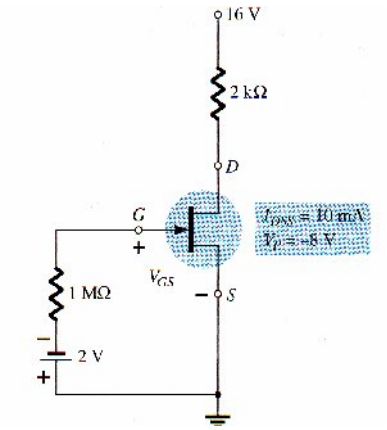


Fig8-5 Example 1:

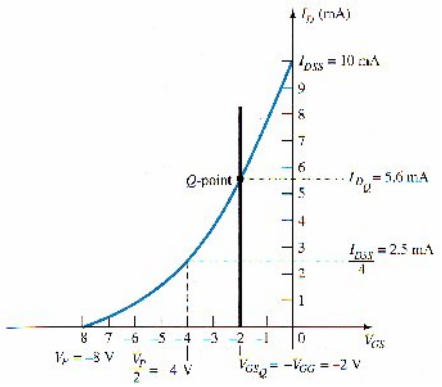


Fig8-6 Graphical solution for Ex:1

Solution:

From the graph of fig8 -6 , 5.6mA is quite acceptable. Therefore, for part (a)

$$V_{GS_Q} = -V_{GG} = \mathbf{-2\ V}$$

(b) $I_{D_Q} = \mathbf{5.6\ mA}$

(c) $V_{DS} = V_{DD} - I_D R_D = 16\ \text{V} - (5.6\ \text{mA})(2\ \text{k}\Omega)$

$= 16\ \text{V} - 11.2\ \text{V} = \mathbf{4.8\ V}$

(d) $V_D = V_{DS} = \mathbf{4.8\ V}$

(e) $V_G = V_{GS} = \mathbf{-2\ V}$

(f) $V_S = \mathbf{0\ V}$

Self-Bias Configuration

The controlling gate-to-source voltage is now determined by the voltage across a resistor $\boldsymbol{R_S}$ *introduced in the source leg of the configuration in fig 8-7*

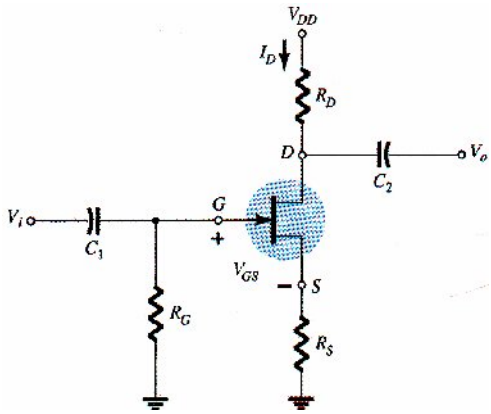


Fig8-7 JFET self-bias configuration

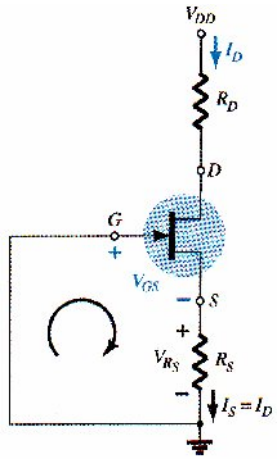


Fig8-8 DC analysis of the self configuration

*The current through R_S is the source current **I_S** but **$I_S = I_D$** and*

$$V_{R_S} = I_D R_S$$

For the indicated closed loop of fig 8-8 we find that

$$-V_{GS} - V_{R_S} = 0$$

and $$V_{GS} = -V_{R_S}$$

or $$V_{GS} = -I_D R_S \qquad [8\text{-}10]$$

Substituting this equation into Shockley"s equation as below:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= I_{DSS}\left(1 - \frac{-I_D R_S}{V_P}\right)^2$$

$$I_D = I_{DSS}\left(1 + \frac{I_D R_S}{V_P}\right)^2$$

*so we must identify two point , **the first** point as defines shown in fig8-9, **The second** point identifies by using this approximating:*

$$I_D = \frac{I_{DSS}}{2} \qquad \textit{Then} \qquad V_{GS} = -I_D R_S = -\frac{I_{DSS} R_S}{2}$$

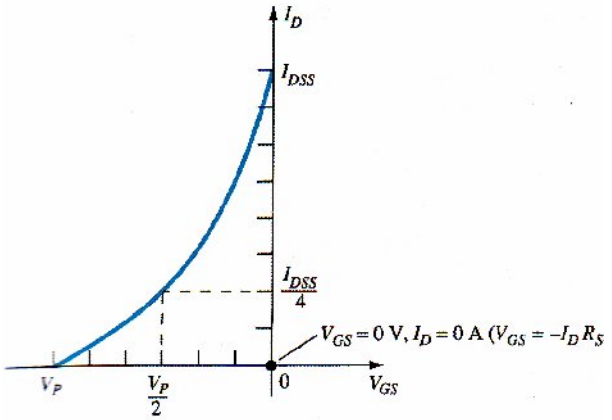


Fig8-9defining a point on the self-bias line

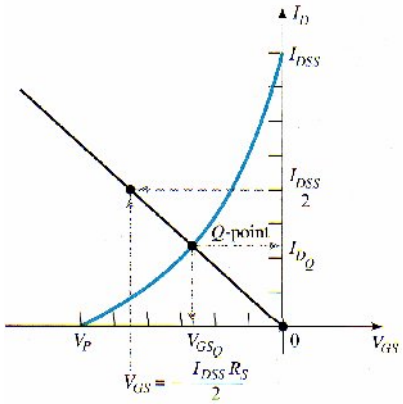


Fig8-10 sketching the self-bias line

Applying KVL to the output circuit to determine the V_{DS}

$$V_{R_S} + V_{DS} + V_{R_D} - V_{DD} = 0$$

and $$V_{DS} = V_{DD} - V_{R_S} - V_{R_D} = V_{DD} - I_S R_S - I_D R_D$$

but $I_D = I_S$

and $V_{DS} = V_{DD} - I_D(R_S + R_D)$ [8-11]

$V_S = I_D R_S$ [8-12]

$V_G = 0\ \text{V}$ [8-13]

and $V_D = V_{DS} + V_S = V_{DD} - V_{R_D}$ [8-14]

Example 2: *Determine the following for the network of fig8-11,(a) V_{GSQ} (b) I_{DQ} (c) V_{DS} (d) V_S (e) V_G (f) V_D*

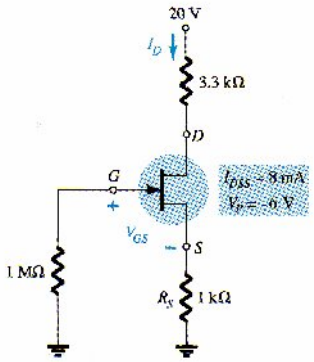


Fig8-11 Example2:

Solution:

$$V_{GS} = -I_D R_S$$

Choosing ***I_D = 4mA****, we obtain*

$$V_{GS} = -(4\ \text{mA})(1\ \text{k}\Omega) = -4\ \text{V}$$

The result is the plot of fig8-12 as defined by the network, If choose $V_{GS} = V_P / 2 = -3V$, we find $I_D = I_{DSS} /4 = 8mA / 4 = 2mA$, as shown in fig 8-13

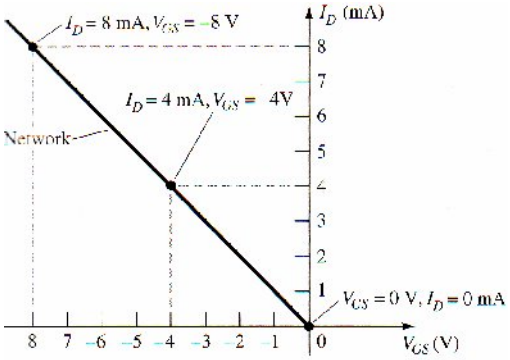


Fig8-12 self bias line for Ex2:

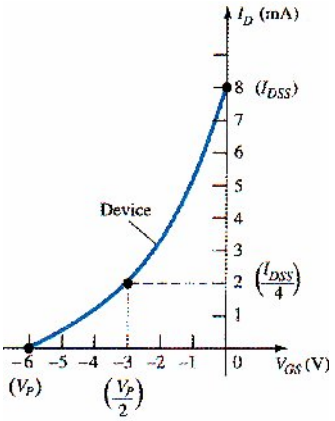
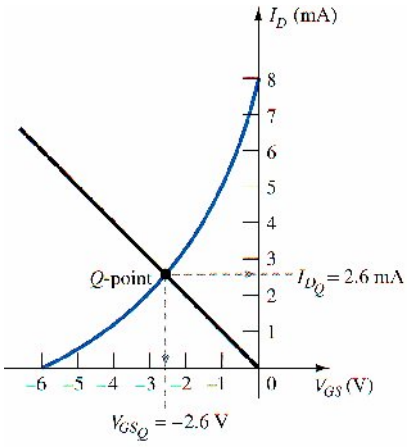


Fig8-13 JFET of Ex2



Fg8-14 Q-point for the network

$$V_{GS_Q} = -2.6\ \text{V}$$

(b) At the quiescent point:

$$I_{D_Q} = 2.6\ \text{mA}$$

(c) Eq[8-11]:

$$V_{DS} = V_{DD} - I_D(R_S + R_D)$$
$$= 20\text{ V} - (2.6\text{ mA})(1\text{ k}\Omega + 3.3\text{ k}\Omega)$$
$$= 20\text{ V} - 11.18\text{ V}$$
$$= \mathbf{8.82\text{ V}}$$

(d) Eq.[8-12]:

$$= (2.6\text{ mA})(1\text{ k}\Omega)$$
$$= \mathbf{2.6\text{ V}}$$

(e) Eq. [8-13]:

$$V_G = \mathbf{0\text{ V}}$$

(f) Eq.[8-14]:

$$V_D = V_{DS} + V_S = 8.82\text{ V} + 2.6\text{ V} = \mathbf{11.42\text{ V}}$$
$$V_D = V_{DD} - I_D R_D = 20\text{ V} - (2.6\text{ mA})(3.3\text{ k}\Omega) = \mathbf{11.42\text{ V}}$$

Example3: *Find the quiescent point for the network of fig8-11 if(a) RS=100Ω, (b) RS=10kΩ*

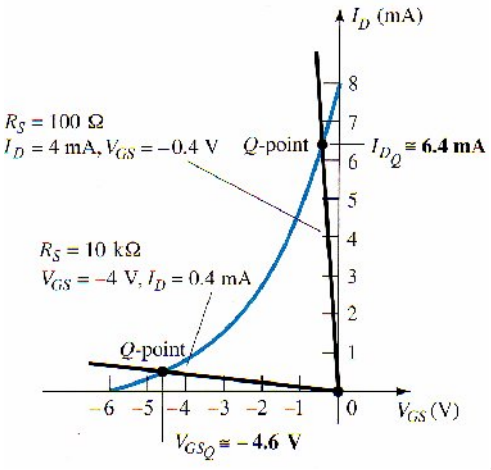


Fig8-15 Example 3:

(a)I_D scale

$$I_{D_Q} \cong \mathbf{6.4\text{ mA}}$$

From Eq.[9-10]

$$V_{GS_Q} \cong \mathbf{-0.64\text{ V}}$$

V_{GS} scale,

$$V_{GS_Q} \cong \mathbf{-4.6\text{ V}}$$

From Eq.[9-10]

$$I_{D_Q} \cong \mathbf{0.46\text{ mA}}$$

Example4: *Determine the following for the common-gate configuration of fig8-16(a)V_{GSQ} (b) I_D (c) V_D (d)V_G (e)V_S (f)V_{DS}*

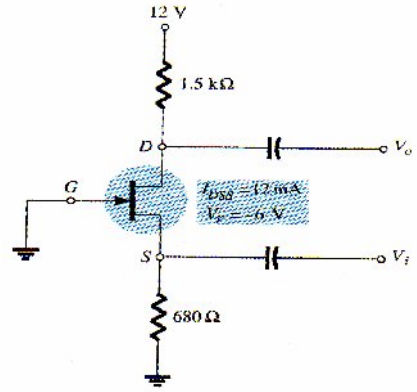
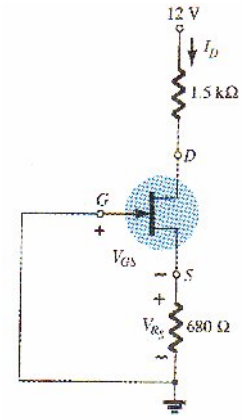


Fig8-16 Example 4:



8-17 the dc resulting

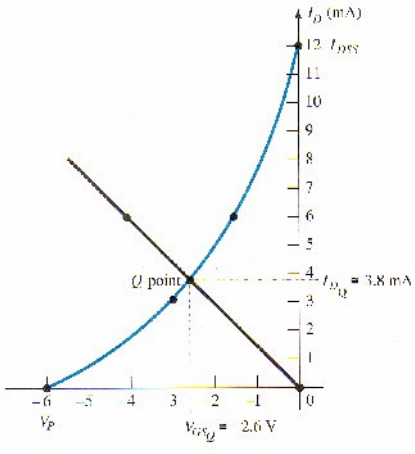


Fig 8-18 Q-point for the network

Solution:

a) The transfer characteristic and load line appear in fig8-18. ***The second*** *point for the sketch of the load line was determined by choosing (arbitrarily)* I_D**=6mA,** *solving for* V_{GS}

$$V_{GS} = -I_D R_S = -(6\text{ mA})(680\ \Omega) = -4.08\text{ V}$$

As shown in fig8-18. The device transfer curve was sketched using

$$I_D = \frac{I_{DSS}}{4} = \frac{12\text{ mA}}{4} = 3\text{ mA}$$

$$V_{GS} = \frac{V_P}{2} = -\frac{6\text{ V}}{2} = -3\text{ V}$$

The resulting quiescent point of fig8-18 is:

$$V_{GS_Q} \cong -2.6\text{ V}$$

(b) from fig8-18

$$I_{D_Q} \cong 3.8\text{ mA}$$

(c) $V_D = V_{DD} - I_D R_D$

$= 12\text{ V} - (3.8\text{ mA})(1.5\text{ k}\Omega) = 12\text{ V} - 5.7\text{ V}$

$= 6.3\text{ V}$

(d) $V_G = 0\text{ V}$

(e) $V_S = I_D R_S = (3.8\text{ mA})(680\ \Omega)$

$= 2.58\text{ V}$

(f) $V_{DS} = V_D - V_S$

$= 6.3\text{ V} - 2.58\text{ V}$

$= 3.72\text{ V}$

Voltage-Divider Biasing

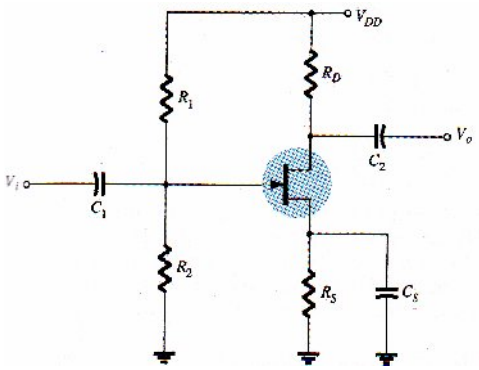


Fig8-19 voltage-divider bias arrangement

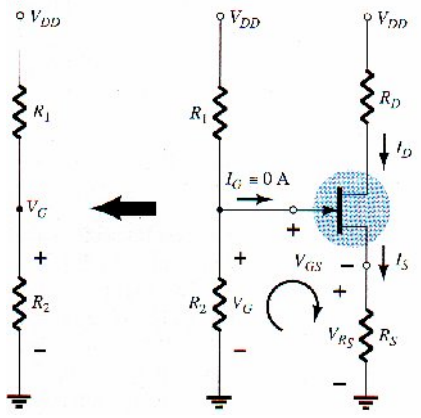


Fig8-20 redrawn network for dc analysis

I_G **= 0 A**, *KCL requires that* I_{R1} **=** I_{R2}, V_G *found using Voltage Divider Rule as:*

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} \qquad [8\text{-}15]$$

Applying KVL in the clockwise direction to the indicated loop of fig 8-20

$$V_G - V_{GS} - V_{R_S} = 0$$

$$V_{GS} = V_G - V_{R_S}$$

$V_{R_S} = I_S R_S = I_D R_S$, we have

$$V_{GS} = V_G - I_D R_S \qquad [8\text{-}16]$$

Set I_D *= 0mA resulting:*

$$V_{GS} = V_G - I_D R_S$$
$$= V_G - (0\text{ mA})R_S$$

$$V_{GS} = V_G|_{I_D = 0\text{ mA}}$$ [8-17]

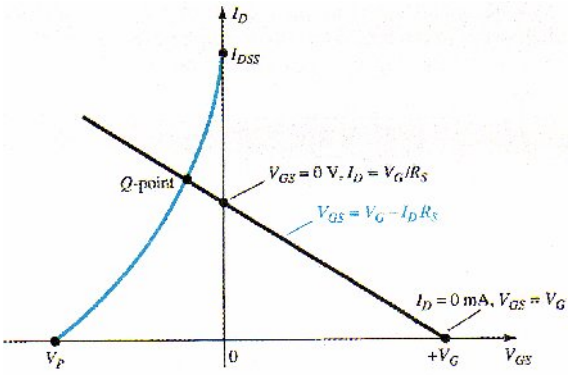


Fig8-21 the network equation

For the other point, let us now employ the fact that:

$$V_{GS} = V_G - I_D R_S$$
$$0\text{ V} = V_G - I_D R_S$$

$$I_D = \frac{V_G}{R_S}\Big|_{V_{GS} = 0\text{ V}}$$ [8-18]

Increasing values of R_S result in lower quiescent values of I_D and more negative values of V_{GS}

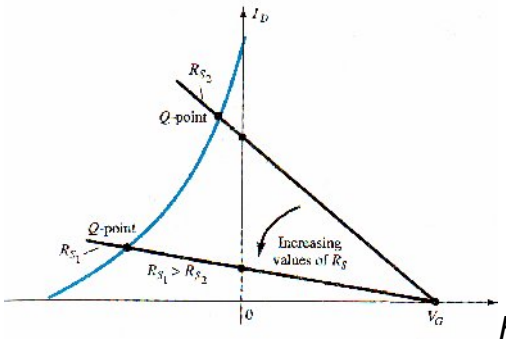


Fig8-22 effect of R_S on the resulting Q-point

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$ [8-19]

$$V_D = V_{DD} - I_D R_D$$ [8-20]

$$V_S = I_D R_S$$ [8-21]

$$I_{R_1} = I_{R_2} = \frac{V_{DD}}{R_1 + R_2}$$ [8-22]

Example 5: *Determine the following for the network of fig8-23,(a) I_{DQ} & V_{GSQ} (b) V_D (c) V_S (d) V_{DS} (e) V_{DG}*

Solution*: a) For the transfer char-, if $I_D = I_{DSS}/4 = 8mA/4 = 2mA$, then $V_{GS} = V_P/2 = -4V/2 = -2V$*
The resulting curve in fig8-24; the network equation is defined by:

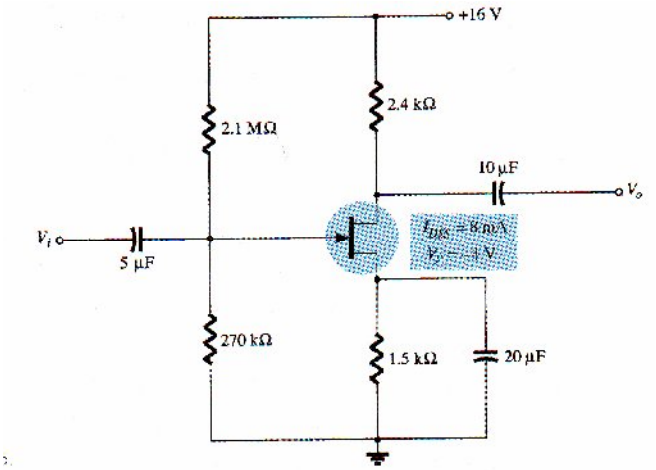


Fig8-23 Example 5:

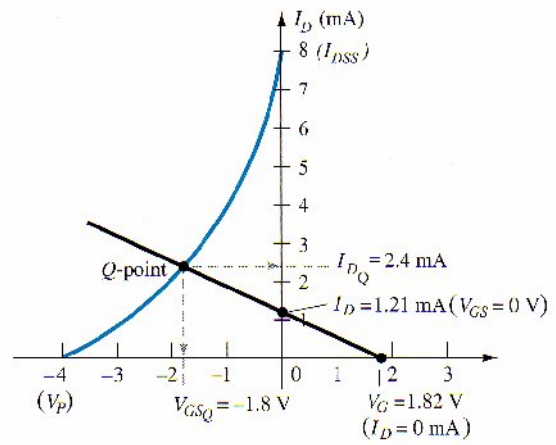


Fig8-24 the **Q**-point for the network

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

$$= \frac{(270\ \text{k}\Omega)(16\ \text{V})}{2.1\ \text{M}\Omega + 0.27\ \text{M}\Omega}$$

$$= 1.82\ \text{V}$$

$$V_{GS} = V_G - I_D R_S$$

$$= 1.82\ \text{V} - I_D(1.5\ \text{k}\Omega)$$

When $I_D = 0$ mA:

$$V_{GS} = +1.82\ \text{V}$$

When $V_{GS} = 0$ V:

$$I_D = \frac{1.82\ \text{V}}{1.5\ \text{k}\Omega} = 1.21\ \text{mA}$$

The resulting bias line appears on fig 8-24 with quiescent values of

$$I_{D_Q} = \mathbf{2.4\ mA}$$

and

$$V_{GS_Q} = \mathbf{-1.8\ V}$$

(b) $V_D = V_{DD} - I_D R_D$

$= 16\ \text{V} - (2.4\ \text{mA})(2.4\ \text{k}\Omega)$

$= \mathbf{10.24\ V}$

(c) $V_S = I_D R_S = (2.4\ \text{mA})(1.5\ \text{k}\Omega)$

$= \mathbf{3.6\ V}$

(d) $V_{DS} = V_{DD} - I_D(R_D + R_S)$

$= 16\ \text{V} - (2.4\ \text{mA})(2.4\ \text{k}\Omega + 1.5\ \text{k}\Omega)$

$= \mathbf{6.64\ V}$

or $V_{DS} = V_D - V_S = 10.24\ \text{V} - 3.6\ \text{V}$

$= \mathbf{6.64\ V}$

$V_{DG} = V_D - V_G$

$= 10.24\ \text{V} - 1.82\ \text{V}$

$= \mathbf{8.42\ V}$

Example6: *Determine the following for the network of fig8-25, ,(a) I_{DQ} & V_{GSQ} (b) V_{DS} (c) V_D (d) V_S*

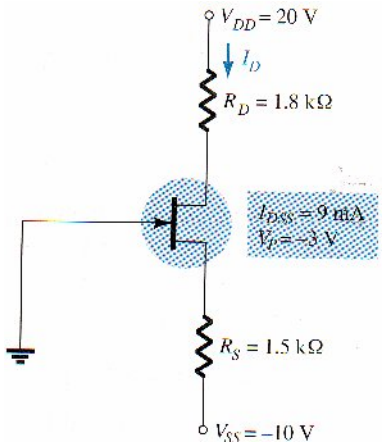


Fig8-25 Ex6

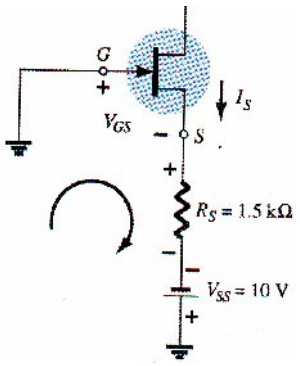


Fig8-26 the network

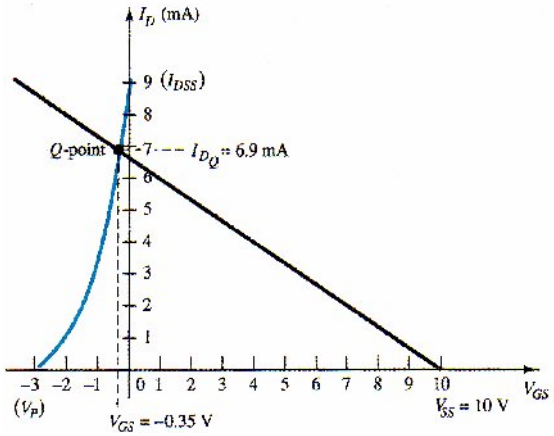


Fig8-27 Q-point

Solution:

a) Applying KVL to the input section of the network redrawn in fig 8-26

$$-V_{GS} - I_S R_S + V_{SS} = 0$$

or $$V_{GS} = V_{SS} - I_S R_S$$

but $$I_S = I_D$$

and $$\boxed{V_{GS} = V_{SS} - I_D R_S} \qquad [8\text{-}23]$$

$$V_{GS} = 10\text{ V} - I_D(1.5\text{ k}\Omega)$$

For $I_D = 0$ mA,

$$V_{GS} = V_{SS} = 10\text{ V}$$

For $V_{GS} = 0$ V,

$$0 = 10\text{ V} - I_D(1.5\text{ k}\Omega)$$

and $$I_D = \frac{10\text{ V}}{1.5\text{ k}\Omega} = 6.67\text{ mA}$$

For the transfer char-, $V_{GS}=V_P/2=-3V/2 =-1.5V$ and $I_D=I_{DSS}/4 =9mA/4=2.25mA$

$$I_{D_Q} = \mathbf{6.9\text{ mA}}$$

$$V_{GS_Q} = \mathbf{-0.35\text{ V}}$$

b) Applying KVL to the output side of fig8-26 will result

$$-V_{SS} + I_S R_S + V_{DS} + I_D R_D - V_{DD} = 0$$

Substituting $I_S = I_D$ and rearranging gives

$$\boxed{V_{DS} = V_{DD} + V_{SS} - I_D(R_D + R_S)} \qquad [8\text{-}24]$$

$$V_{DS} = 20\text{ V} + 10\text{ V} - (6.9\text{ mA})(1.8\text{ k}\Omega + 1.5\text{ k}\Omega)$$
$$= 30\text{ V} - 22.77\text{ V}$$
$$= \mathbf{7.23\text{ V}}$$

(c) $$V_D = V_{DD} - I_D R_D$$
$$= 20\text{ V} - (6.9\text{ mA})(1.8\text{ k}\Omega) = 20\text{ V} - 12.42\text{ V}$$
$$= \mathbf{7.58\text{ V}}$$

(d) $$V_{DS} = V_D - V_S$$

or $$V_S = V_D - V_{DS}$$
$$= 7.58\text{ V} - 7.23\text{ V}$$
$$= \mathbf{0.35\text{ V}}$$

Depletion –Type MOSFETS

Example 7: *For the n-channel depletion-type of fig8-28, determine: I_{DQ} & V_{GSQ} & V_{DS}*

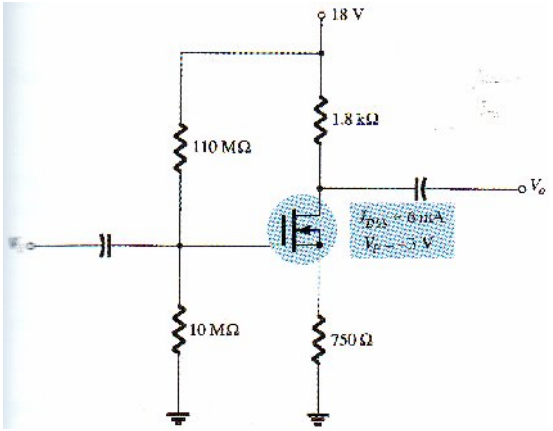


Fig8-28 n-DMOSFET Example 7:

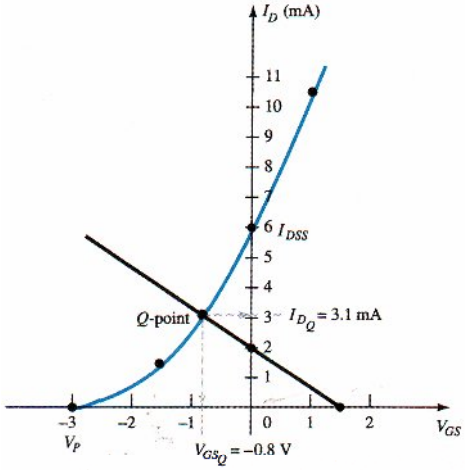


Fig8-29Q-point for the network of Ex7n-DMOSFET

Setting $I_D = 0$ mA results in

$$V_{GS} = V_G = 1.5 \text{ V}$$

Setting $V_{GS} = 0$ V yields

$$I_D = \frac{V_G}{R_S} = \frac{1.5 \text{ V}}{750\ \Omega} = 2 \text{ mA}$$

Solution: *For the transfer char-, $V_{GS}=V_P/2=-3V/2$ =-1.5V and $I_D=I_{DSS}/4$ =6mA/4=1.5mA, consider the level of V_P and the fact that Skockley's equation defines a curve that rises more positive. A plot point will defined at V_{GS} =+1V.*

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= 6 \text{ mA}\left(1 - \frac{+1 \text{ V}}{-3 \text{ V}}\right)^2 = 6 \text{ mA}\left(1 + \frac{1}{3}\right)^2 = 6 \text{ mA}(1.778)$$

$$= 10.67 \text{ mA}$$

Eq[8-15]

$$V_G = \frac{10 \text{ M}\Omega(18 \text{ V})}{10 \text{ M}\Omega + 110 \text{ M}\Omega} = 1.5 \text{ V}$$

Eq[8-16]

$$V_{GS} = V_G - I_D R_S = 1.5 \text{ V} - I_D(750\ \Omega)$$

The plot point and resulting bias line appear in fig8-29 the resulting operating point:

$$I_{D_Q} = \mathbf{3.1 \text{ mA}}$$

$$V_{GS_Q} = \mathbf{-0.8 \text{ V}}$$

b)Eq[8-19]

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

$$= 18 \text{ V} - (3.1 \text{ mA})(1.8 \text{ k}\Omega + 750\ \Omega)$$

$$\cong \mathbf{10.1 \text{ V}}$$

Example 8: *Repeat Example 7: with R_S = 150Ω*

Solution: *(a) The plot points are the same for the transfer curve as shown in fig8-30,*

$$V_{GS} = V_G - I_D R_S = 1.5 \text{ V} - I_D(150\ \Omega)$$

Setting $I_D = 0$ mA results in

$$V_{GS} = 1.5 \text{ V}$$

Setting $V_{GS} = 0$ V yields

$$I_D = \frac{V_G}{R_S} = \frac{1.5 \text{ V}}{150\ \Omega} = 10 \text{ mA}$$

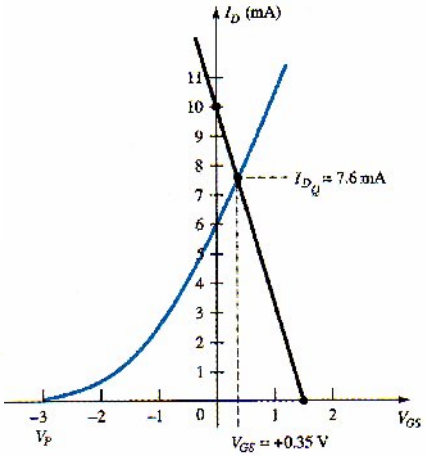


Fig8-30 Ex 8:

$$I_{D_Q} = \mathbf{7.6\ mA}$$
$$V_{GS_Q} = \mathbf{+0.35\ V}$$

b)Eq[8-19]

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$
$$= 18 \text{ V} - (7.6 \text{ mA})(1.8 \text{ k}\Omega + 150\ \Omega)$$

Example 9: *Determine the following for the network of fig8-31, I_{DQ} & V_{GSQ} & V_D*

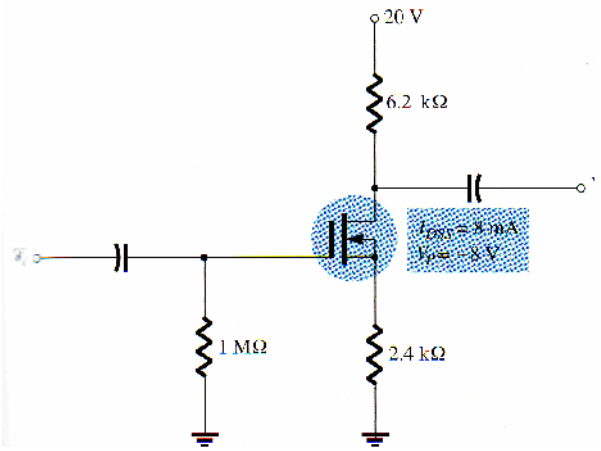


Fig8-31 Example 9:

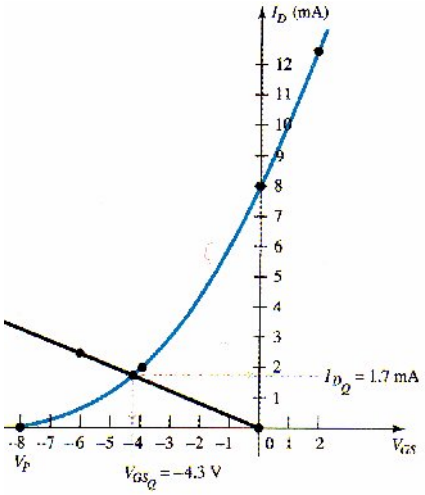


Fig8-32 the Q-point for the network of Ex9:

Solution:

$$V_{GS} = -I_D R_S$$

For JFET V_{GS} must be less than zero volts. Therefore no requirement to plot the transfer curves for positive values of V_{GS}

$$I_D = \frac{I_{DSS}}{4} = \frac{8 \text{ mA}}{4} = 2 \text{ mA}$$

and

$$V_{GS} = \frac{V_P}{2} = \frac{-8 \text{ V}}{2} = -4 \text{ V}$$

and for $V_{GS} > 0$ V, since $V_P = -8$ V, we will choose

$$V_{GS} = +2 \text{ V}$$

and

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 8 \text{ mA}\left(1 - \frac{+2 \text{ V}}{-8 \text{ V}}\right)^2$$
$$= 12.5 \text{ mA}$$

In fig 8-32. For the network bias line, at V_{GS}=0V, I_D=0mA. Choosing V_{GS} = -6V

$$I_D = -\frac{V_{GS}}{R_S} = -\frac{-6\text{ V}}{2.4\text{ k}\Omega} = 2.5\text{ mA}$$

The resulting Q-point:

$$I_{D_Q} = \mathbf{1.7\text{ mA}}$$
$$V_{GS_Q} = \mathbf{-4.3\text{ V}}$$

(b) $V_D = V_{DD} - I_D R_D$
$= 20\text{ V} - (1.7\text{ mA})(6.2\text{ k}\Omega)$
$= \mathbf{9.46\text{ V}}$

Example 10: *Determine V_{DS} for the network of fig8-33*

Solution:

$$V_{GS} = 0\text{ V}$$

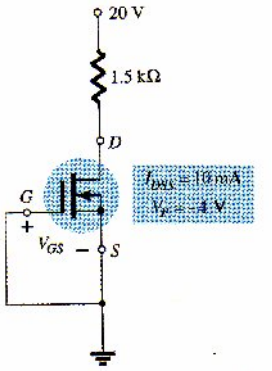


Fig8-33 Example10:

$$V_{GS_Q} = \mathbf{0\text{ V}}$$
$$I_{D_Q} = \mathbf{10\text{ mA}}$$

$V_D = V_{DD} - I_D R_D = 20\text{ V} - (10\text{ mA})(1.5\text{ k}\Omega)$
$= 20\text{ V} - 15\text{ V}$

Enhancement-Type MOSFETs

$$I_D = k(V_{GS} - V_{GS(\text{Th})})^2 \qquad [8\text{-}25]$$

$$I_D = k(V_{GS} - V_{GS(\text{Th})})^2$$

$$I_{D(\text{on})} = k(V_{GS(\text{on})} - V_{GS(\text{Th})})^2$$

$$k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS(\text{Th})})^2} \qquad [8\text{-}26]$$

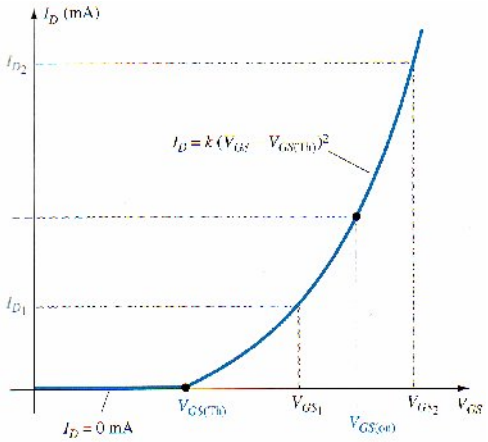


Fig8-34 Transfer char- of n-EMOSFET

Feedback Biasing Arrangement

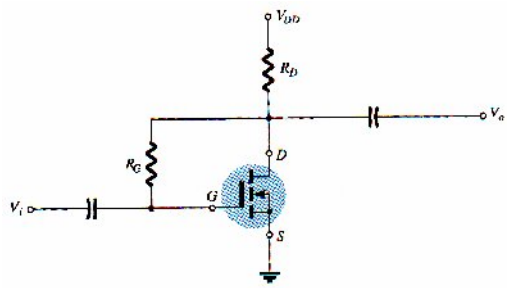


Fig8-35Feedback biasing arrangement

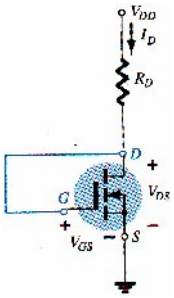


Fig8-36Dc equivalent of the network

A direct connection now exists between drain and gate, resulting in

$$V_D = V_G$$

and

$$V_{DS} = V_{GS} \qquad [8\text{-}27]$$

For the output circuit,

$$V_{DS} = V_{DD} - I_D R_D$$

Which becomes the following after substituting Eq[8-27]

$$V_{GS} = V_{DD} - I_D R_D \qquad [8\text{-}28]$$

Substituting I_D = 0mA into Eq[8-28] gives:

$$V_{GS} = V_{DD}\big|_{I_D = 0\,\text{mA}} \qquad [8\text{-}29]$$

Substituting V_{GS} = 0mA into Eq[8-28], gives:

$$I_D = \frac{V_{DD}}{R_D}\bigg|_{V_{GS} = 0\,\text{V}} \qquad [8\text{-}30]$$

A plot defined by Eq[8-25] and [8-28] in fig 8-37 with the resulting operation point

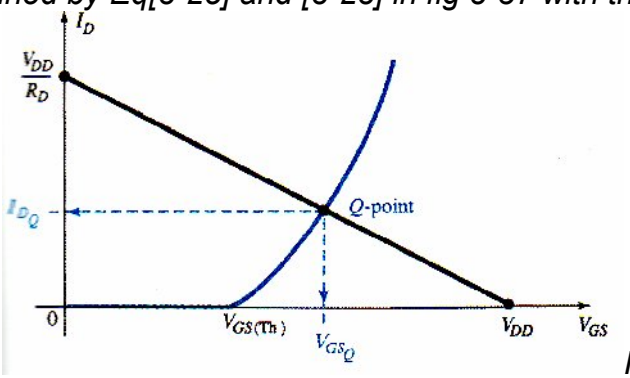


Fig8-37 Q-point for the network

Example 11: *Determine I_{DQ} and V_{DSQ} for the enhancement-type MOSFET of fig 8-38*

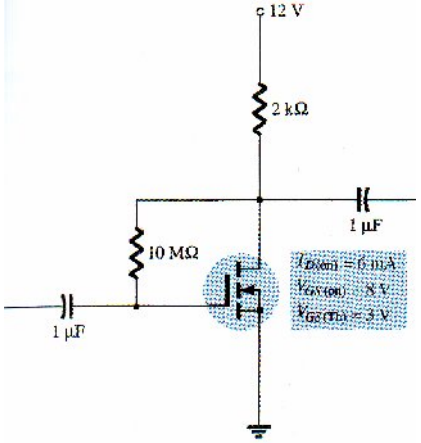


Fig8-38 Example 11:

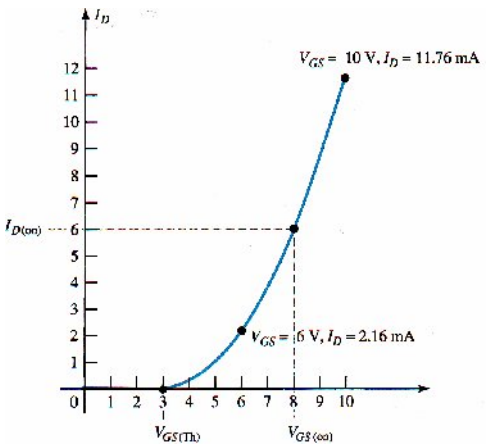


Fig8-39 transfer curve for the MOSFET of Ex 11:

Solution: *Two points are defined immediately as shown in fig8-39. Solving for k, Eq[8-26]:*

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(Th)})^2}$$

$$= \frac{6\text{ mA}}{(8\text{ V} - 3\text{ V})^2} = \frac{6 \times 10^{-3}}{25}\text{ A/V}^2$$

$$= \mathbf{0.24 \times 10^{-3}\ A/V^2}$$

For $V_{GS} = 6$ V (between 3 and 8 V):

$$I_D = 0.24 \times 10^{-3}(6\text{ V} - 3\text{ V})^2 = 0.24 \times 10^{-3}(9)$$

$$= 2.16\text{ mA}$$

For $V_{GS} = 10$ V (slightly greater than $V_{GS(Th)}$):

$$I_D = 0.24 \times 10^{-3}(10\text{ V} - 3\text{ V})^2 = 0.24 \times 10^{-3}(49)$$

$$= 11.76\text{ mA}$$

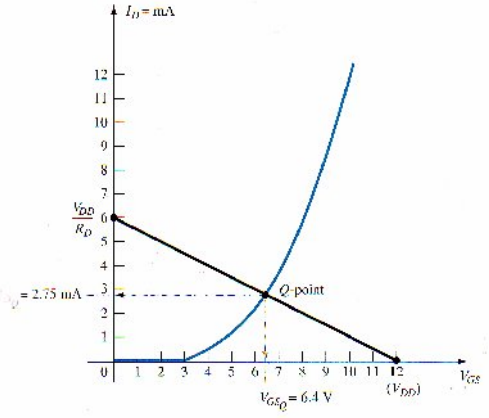
For the Network Bias Line:

$$V_{GS} = V_{DD} - I_D R_D$$

$$= 12\text{ V} - I_D(2\text{ k}\Omega)$$

$$V_{GS} = V_{DD} = 12\text{ V}|_{I_D = 0\text{ mA}}$$

$$I_D = \frac{V_{DD}}{R_D} = \frac{12\text{ V}}{2\text{ k}\Omega} = 6\text{ mA}|_{V_{GS} = 0\text{ V}}$$



$I_{D_Q} = \mathbf{2.75\ mA}$

$V_{GS_Q} = 6.4$ V

$V_{DS_Q} = V_{GS_Q} = \mathbf{6.4\ V}$

Fig8-40Q-point for the network

Voltage-Divider Biasing Arrangement

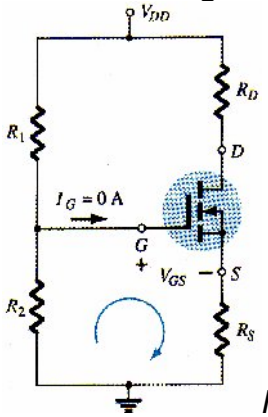


Fig8-41 Voltage-divider biasing for n- EMOSFET

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} \qquad [8\text{-}31]$$

Applying KVL around the indicated loop of fig8-41 will result

$$+V_G - V_{GS} - V_{R_S} = 0$$

$$V_{GS} = V_G - V_{R_S}$$

$$V_{GS} = V_G - I_D R_S \qquad [8\text{-}32]$$

For the output section:

$$V_{R_S} + V_{DS} + V_{R_D} - V_{DD} = 0$$

$$V_{DS} = V_{DD} - V_{R_S} - V_{R_D}$$

$$V_{DS} = V_{DD} - I_D(R_S + R_D) \qquad [8\text{-}33]$$

Example 12: *Determine I_{DQ} , V_{GSQ} , and V_{DS} for the network of fig8-42*

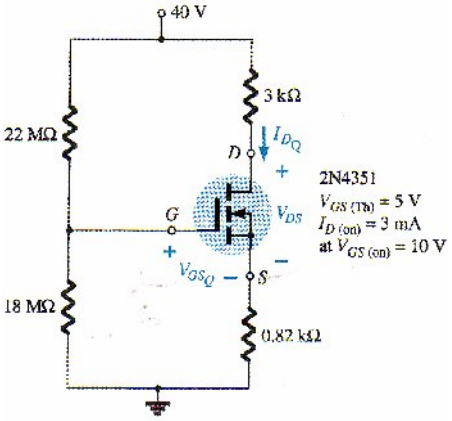


Fig8-42 Example 12:

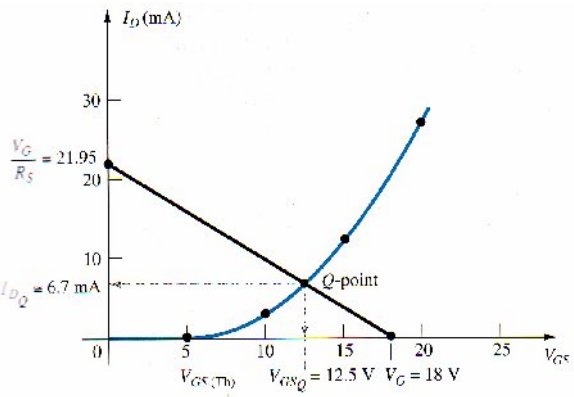


Fig8-43 Q-point for network of Ex 12:

Solution: Network:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} = \frac{(18\ \text{M}\Omega)(40\ \text{V})}{22\ \text{M}\Omega + 18\ \text{M}\Omega} = 18\ \text{V}$$

$$V_{GS} = V_G - I_D R_S = 18\ \text{V} - I_D(0.82\ \text{k}\Omega)$$

When I_D = 0mA

$$V_{GS} = 18\ \text{V} - (0\ \text{mA})(0.82\ \text{k}\Omega) = 18\ \text{V}$$

As appearing on fig 8-43, when V_{GS} = 0 V

$$V_{GS} = 18\ \text{V} - I_D(0.82\ \text{k}\Omega)$$

$$0 = 18\ \text{V} - I_D(0.82\ \text{k}\Omega)$$

$$I_D = \frac{18\ \text{V}}{0.82\ \text{k}\Omega} = 21.95\ \text{mA}$$

Device: $V_{GS(\text{Th})} = 5\ \text{V}, \quad I_{D(\text{on})} = 3\ \text{mA with } V_{GS(\text{on})} = 10\ \text{V}$

$$k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS(\text{Th})})^2}$$

$$= \frac{3\ \text{mA}}{(10\ \text{V} - 5\ \text{V})^2} = 0.12 \times 10^{-3}\ \text{A/V}^2$$

$$I_D = k(V_{GS} - V_{GS(\text{Th})})^2$$

$$= 0.12 \times 10^{-3}(V_{GS} - 5)^2$$

$$I_{D_Q} \cong \mathbf{6.7\ mA}$$

$$V_{GS_Q} = \mathbf{12.5\ V}$$

$$V_{DS} = V_{DD} - I_D(R_S + R_D)$$

$$= 40\ \text{V} - (6.7\ \text{mA})(0.82\ \text{k}\Omega + 3.0\ \text{k}\Omega)$$

$$= 40\ \text{V} - 25.6\ \text{V}$$

$$= \mathbf{14.4\ V}$$

SUMMARY

1- A fixed-bias configuration has, a fixed dc voltage applied from gate to source to establish the operating point.

2- The nonlinear relationship between the gate-to-source voltage and the drain current of a JFET requires that a graphical or mathematical solution be used to determine the quiescent point of operation.

3- All voltages with a single subscript define a voltage from a specified point to ground.

4- The self-bias configuration is determined by an equation for V_{GS} that will always pass through the origin. Any other point determined by the biasing equation will establish a straight line to represent the biasing network.

5- For the voltage-divider biasing configuration, one can always assume that the gate current is 0A to permit isolation or the voltage-divider network from the output section. The resulting gate-to-ground voltage will always be positive for an n-channel JFET and negative for a p-channel JFET. Increasing values of R_s result in lower quiescent values of I_D and more negative values of V_{GS} for an n-channel JFET

6- The method of analysis applied to depletion-type MOSFETs is the same as applied to JFETs, with the only difference being a possible operating point with an I_D level above the I_{DSS} value.

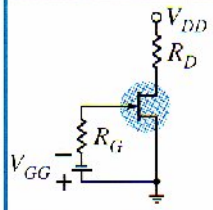
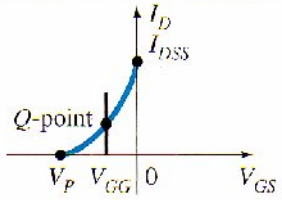
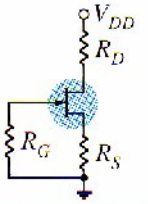
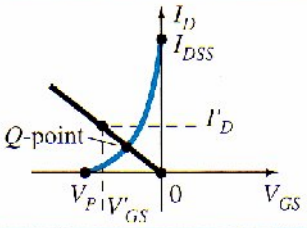
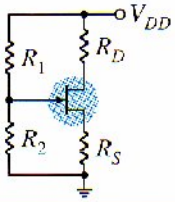
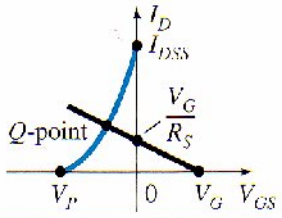
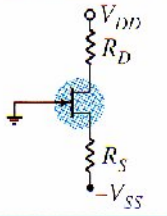
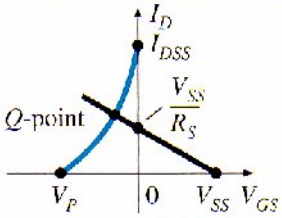
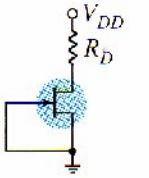
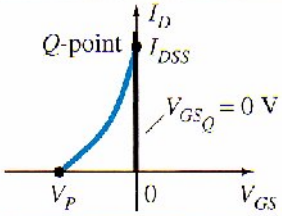
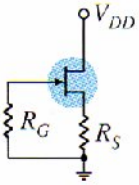
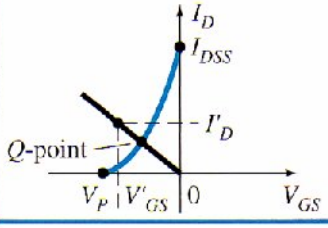
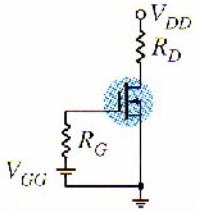
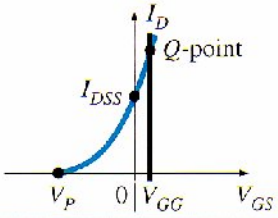
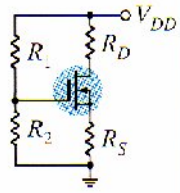
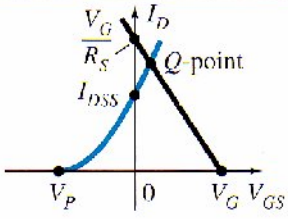
7- The characteristics and method of analysis applied to enhancement-type MOSFETs are entirely different from those of JFETs and depletion-type MOSFETs. For values of V_{GS} less than the threshold value, the drain current I_D is 0A.

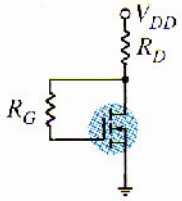
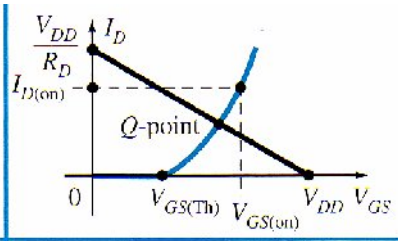
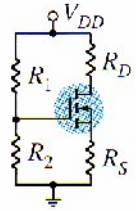
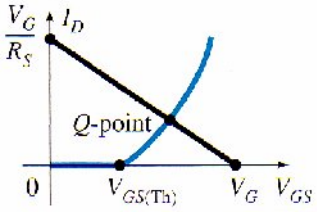
8- When analyzing networks with a variety of devices. First work with the region of the network that will provide a voltage or current level using the basic relationships associated with those devices. Then use that level and the appropriate equations to find other voltage or current levels of the net work in the surrounding region of the system.

9- The design process often requires finding a resistance level to establish the desired voltage or current level. With this in mind remember that a resistance level is defined by the voltage across the resistor divided by the current through the resistor. In the design process, both of these quantities are often available for a particular resistive element.

10- The analysis of p-channel FETs is the same as that applied to n-channel FETs except for the fact that all the voltages will have the opposite polarity and the currents the opposite direction

SUMMARY TABLE

Type	Configuration	Pertinent Equations	Graphical Solution
JFET Fixed-bias		$V_{GS_Q} = -V_{GG}$ $V_{DS} = V_{DD} - I_D R_S$	
JFET Self-bias		$V_{GS} = -I_D R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	
JFET Voltage-divider bias		$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_D R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	
JFET Common-gate		$V_{GS} = V_{SS} - I_D R_S$ $V_{DS} = V_{DD} + V_{SS} - I_D(R_D + R_S)$	
JFET ($V_{GS_Q} = 0$ V)		$V_{GS_Q} = 0$ V $I_{D_Q} = I_{DSS}$	
JFET ($R_D = 0\ \Omega$)		$V_{GS} = -I_D R_S$ $V_D = V_{DD}$ $V_S = I_D R_S$ $V_{DS} = V_{DD} - I_S R_S$	
Depletion-type MOSFET Fixed-bias		$V_{GS_Q} = +V_{GG}$ $V_{DS} = V_{DD} - I_D R_S$	
Depletion-type MOSFET Voltage-divider bias		$V_G = \frac{R_2 V_{DD}}{R_1 - R_2}$ $V_{GS} = V_G - I_S R_S$ $V_{DS} = V_{DD} - I_D(R_D - R_S)$	

Enhancement type MOSFET Feedback configuration		$V_{GS} = V_{DS}$ $V_{GS} = V_{DD} - I_D R_D$	
Enhancement type MOSFET Voltage-divider bias		$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_D R_S$	

Equations:

JFETs/depletion-type MOSFETs:

Fixed-bias configuration: $V_{GS} = -V_{GG} = V_G$

Self-bias configuration: $V_{GS} = -I_D R_S$

Voltage-divider biasing: $V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$

$V_{GS} = V_G - I_D R_S$

Enhancement-type MOSFETs:

Feedback biasing: $V_{DS} = V_{GS}$

$V_{GS} = V_{DD} - I_D R_D$

Voltage-divider biasing: $V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$

$V_{GS} = V_G - I_D R_S$

9-FET Small signal analysis

The gate-to-source ac voltage controls the drain-to-source (channel) current of an FET, Skockley's equation controlled the level of dc drain current through a relationship

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

g_m *is a trans-conductance factor using to determined The change in Drain current that will result from a change in gate-to-source voltage in the following:*

$$\Delta I_D = g_m \, \Delta V_{GS} \qquad [9\text{-}1]$$

Conductance of resistor g = 1/R = I/V

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \qquad [9\text{-}2]$$

Graphical Determination of g_m

$$g_m = m = \frac{\Delta y}{\Delta x} = \frac{\Delta I_D}{\Delta V_{GS}} \qquad [9\text{-}3]$$

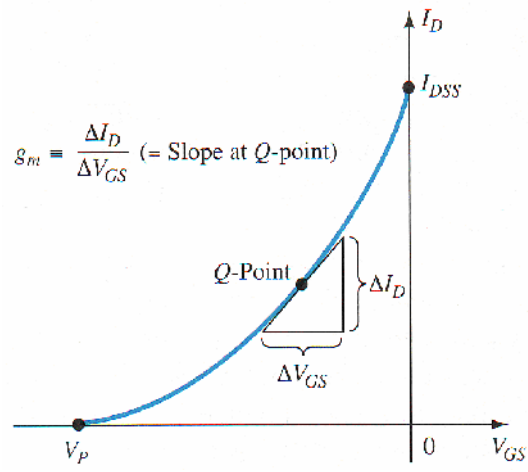


Fig9-1Definition of g_m using transfer chara-

Example1: *Determine* **g_m** *for the JFET with I_{DSS} = 8mA & V_P = -4 at the following dc bias point: (a) V_{GS} = -0.5V,(b) V_{GS} = -1.5V,(c) V_{GS} = -2.5V*

Solution:

$$\text{(a)}g_m = \frac{\Delta I_D}{\Delta V_{GS}} \simeq \frac{2.1\text{ mA}}{0.6\text{ V}} = 3.5\text{ mS}$$

$$\text{(b)}g_m = \frac{\Delta I_D}{\Delta V_{GS}} \cong \frac{1.8\text{ mA}}{0.7\text{ V}} \cong 2.57\text{ mS}$$

$$\text{(c)}g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{1.5\text{ mA}}{1.0\text{ V}} = 1.5\text{ mS}$$

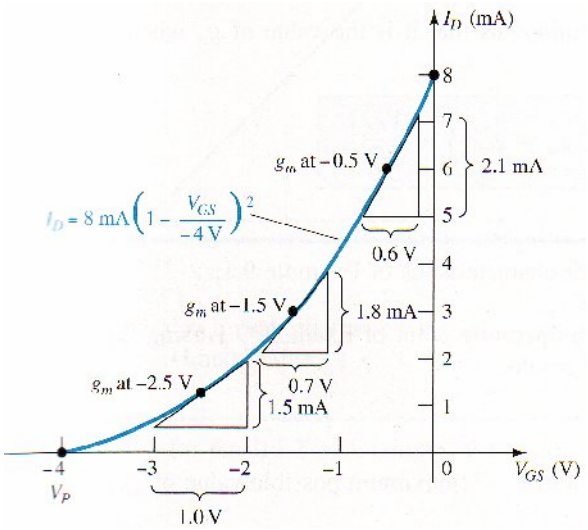


Fig9-2calculating g_m at various bias points

Mathematical Definition of g_m

The derivative of a function at a point is equal to the slope of the tangent line drawn at that point.

$$g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{Q\text{-pt.}} = \left.\frac{dI_D}{dV_{GS}}\right|_{Q\text{-pt.}} = \frac{d}{dV_{GS}}\left[I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2\right]$$

$$= I_{DSS}\frac{d}{dV_{GS}}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 2I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]\frac{d}{dV_{GS}}\left(1 - \frac{V_{GS}}{V_P}\right)$$

$$= 2I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]\left[\frac{d}{dV_{GS}}(1) - \frac{1}{V_P}\frac{dV_{GS}}{dV_{GS}}\right] = 2I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]\left[0 - \frac{1}{V_P}\right]$$

$$g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{V_{GS}}{V_P}\right] \qquad [9\text{-}4]$$

The maximum value of g_m for a JFET in which I_{DSS} and V_P have been specified

$$g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{0}{V_P}\right]$$

$$g_{m0} = \frac{2I_{DSS}}{|V_P|} \qquad [9\text{-}5]$$

*0 means the value of **g_m** when V_{GS} = 0 V, Eq[9-4] then becomes*

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right] \qquad [9\text{-}6]$$

***Example2:** For the JFET having the transfer char-of Ex1:*

(a) find the maximum value of g_m

(b) find the value of g_m at each operating point of Ex1: using Eq[9-6] and compare with graphical result

Solution:

a) $g_{m0} = \dfrac{2I_{DSS}}{|V_P|} = \dfrac{2(8\text{ mA})}{4\text{ V}} = \mathbf{4\text{ mS}}$ (maximum possible value of g_m)

b) At $V_{GS} = -0.5$ V,

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right] = 4\text{ mS}\left[1 - \frac{-0.5\text{ V}}{-4\text{ V}}\right] = \mathbf{3.5\text{ mS}}$$

At $V_{GS} = -1.5$ V,

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right] = 4\text{ mS}\left[1 - \frac{-1.5\text{ V}}{-4\text{ V}}\right] = \mathbf{2.5\text{ mS}}$$

At $V_{GS} = -2.5$ V,

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right] = 4\text{ mS}\left[1 - \frac{-2.5\text{ V}}{-4\text{ V}}\right] = \mathbf{1.5\text{ mS}}$$

*On specification sheet, **g_m** is provided as **y_{fs}** where **y** indicates it is part of an admittance equivalent circuit. The **f** signifies forward transfer parameter, and the **s** reveals that it is connected to the source terminal. In equation:*

$$g_m = y_{fs} \qquad [9\text{-}7]$$

***Plotting g_m vs. V_{GS}**: Eq [9-6], When V_{GS} is 1/2V_P, g_m will be 1/2 the maximum value (g_{m0})*

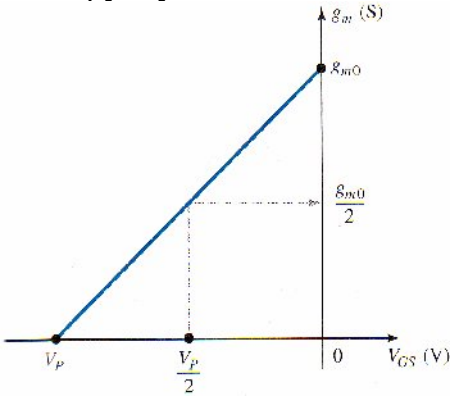


Fig 9-3 plot of g_m vs. V_{GS}

***Example 3:** Plot g_m vs. V_{GS} for the JFET of Ex 1: and Ex 2:*

Solution:

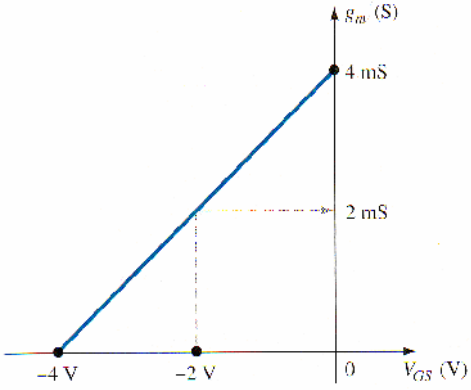


Fig9-4 g_m vs. V_{GS}, with I_{DSS} = 8 mA & V_P = -4 V

Impact of I_D on g_m :

$$1 - \frac{V_{GS}}{V_P} = \sqrt{\frac{I_D}{I_{DSS}}} \qquad [9\text{-}8]$$

Substituting Eq[9-8] into Eq.[9-6] will result in:

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_P}\right) = g_{m0}\sqrt{\frac{I_D}{I_{DSS}}} \qquad [9\text{-}9]$$

(a) If $I_D = I_{DSS}$,

$$g_m = g_{m0}\sqrt{\frac{I_{DSS}}{I_{DSS}}} = g_{m0}$$

(b) If $I_D = I_{DSS}/2$,

$$g_m = g_{m0}\sqrt{\frac{I_{DSS}/2}{I_{DSS}}} = 0.707g_{m0}$$

(c) If $I_D = I_{DSS}/4$,

$$g_m = g_{m0}\sqrt{\frac{I_{DSS}/4}{I_{DSS}}} = \frac{g_{m0}}{2} = 0.5g_{m0}$$

Example 4: *Plot I_D vs. g_m for the JFET of Ex 1: through Ex 3:*
Solution:

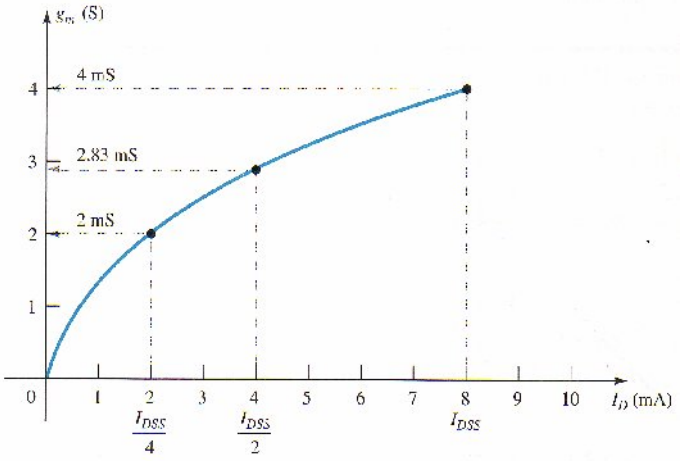


Fig9-5 g_m vs. V_{GS}, I_{DSS} = 8mA & V_P = -4V

$$Z_i\,(\text{FET}) = \infty\ \Omega \qquad [9\text{-}10]$$

$$Z_o\,(\text{FET}) = r_d = \frac{1}{y_{os}} \qquad [9\text{-}11]$$

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}\,=\,\text{constant}} \qquad [9\text{-}12]$$

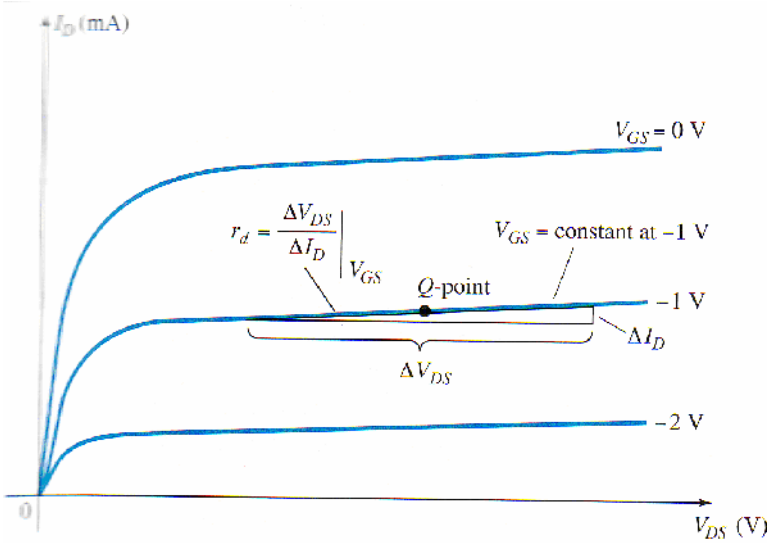


Fig9-9 r_d using FET drain char-

Example 5: *Determine the output impedance for the FET of fig9-7 for V_{GS} = 0V,-2V, 8V*

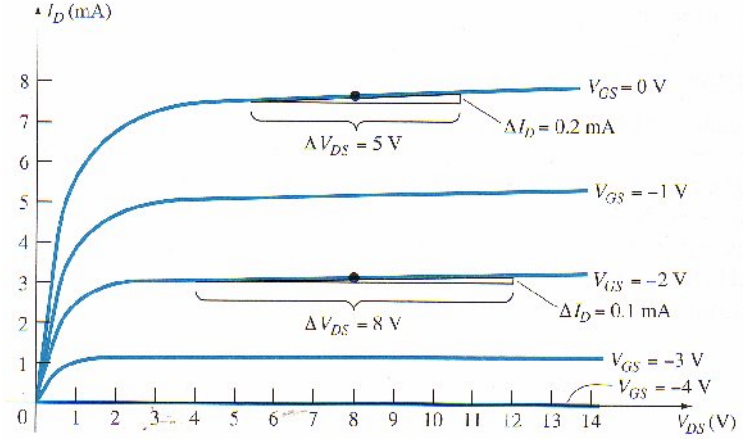


*Fig 9-7 Drain char-for r_d in **Ex5**:*

Solution: *For V_{GS}=0V, a tangent line is drawn and ΔV_{DS} is chosen as 5V, resulting in a ΔI_D of 0.2mA, substituting into Eq[9-12]*

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}=0\text{ V}} = \frac{5\text{ V}}{0.2\text{ mA}} = 25\text{ k}\Omega$$

For V_{GS}=-2V, a tangent line is drawn and ΔV_{DS} is chosen as 8V, resulting in a ΔI_D of 0.1mA, substituting into Eq[9-12]

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}=-2\text{ V}} = \frac{8\text{ V}}{0.1\text{ mA}} = 80\text{ k}\Omega$$

FET ac Equivalent Circuit

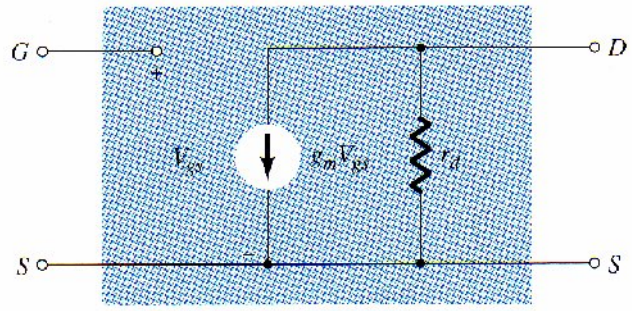


Fig9-8FET ac equivalent circuit

I_d *control by* ***V_{gs}*** *is a current source* ***$g_m V_{gs}$*** *connected from drain to source to establish a 180° phase shift*

Z_i *is open circuit at the input*

Z_o *is* ***r_d*** *from drain to source*

Example 6: *y_{fs} =3.8mS and y_{os} =20μS, Sketch the FET as equivalent model*

Solution:

$$g_m = y_{fs} = 3.8\text{ mS} \quad \text{and} \quad r_d = \frac{1}{y_{os}} = \frac{1}{20\ \mu\text{S}} = 50\text{ k}\Omega$$

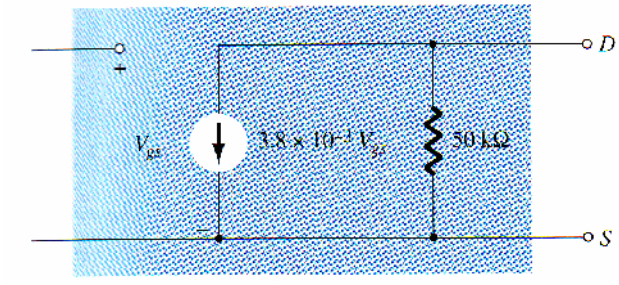


Fig9-9 FET ac model for Ex6:

1-JFET Fixed-Bias Configuration (Common-Source)

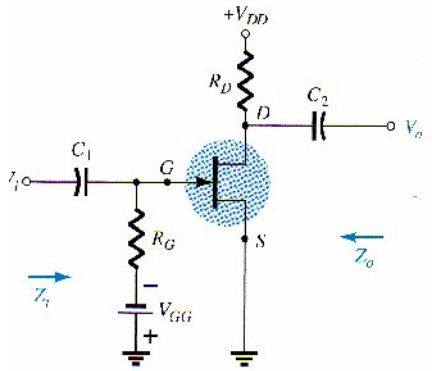


Fig9-10 JFET fixed configuration

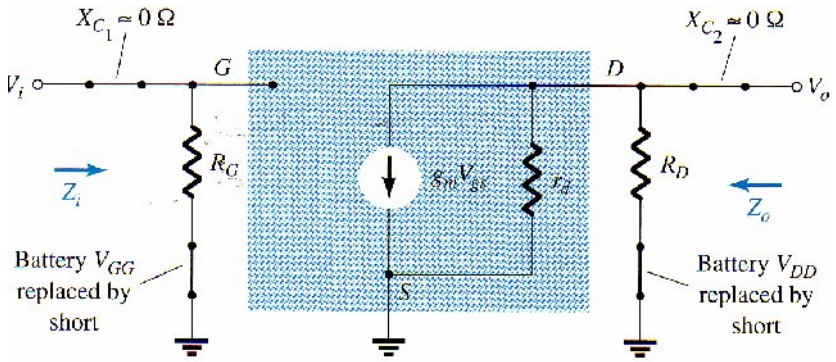


Fig9-11 JFET ac equivalent

g_m & r_d determined from the dc biasing arrangement specification sheet, V_{GG} & V_{DD} are set to zero by a short circuit equivalent

$$Z_i = R_G$$ [9-13]

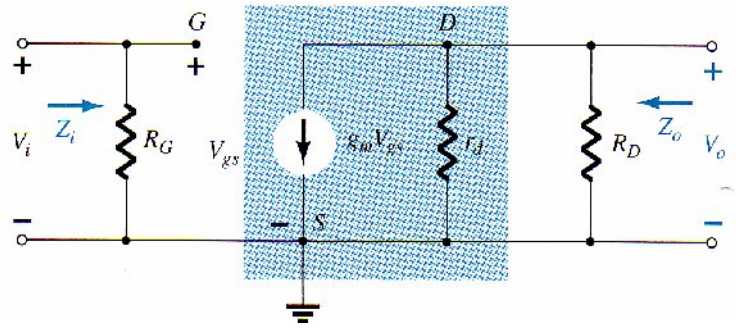
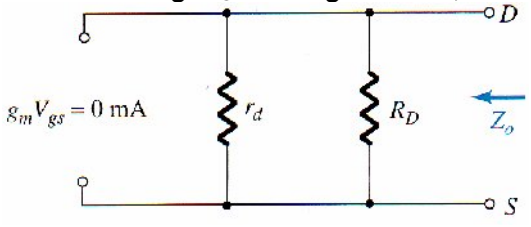


Fig9-12 Redrawn network

For obtaining Z_O Setting V_i = 0V, will establish V_{gs} as 0V also, this result $g_m V_{gs}$ = 0mA



$$Z_o = R_D \| r_d$$ [9-14]

$$Z_o \cong R_D \qquad r_d \geq 10R_D$$ [9-15]

$$V_o = -g_m V_{gs}(r_d \| R_D)$$
$$V_{gs} = V_i$$
$$V_o = -g_m V_i(r_d \| R_D)$$

$$A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D)$$ [9-16]

$$A_v = \frac{V_o}{V_i} = -g_m R_D \qquad r_d \geq 10R_D$$ [9-17]

Phase Relationship: *the* ***negative sign*** *in A_v means 180° phase shift between IP & OP*

Example 7: *configuration of Ex1: had V_{GSQ} = -2V & I_{DQ} = 5.625 mA, with I_{DSS} = 10 mA & V_p = -8V. The network is redrawn as fig9-13 with an applied signal V_i, the value of y_{os} is provided as 40µs, Determine (a) g_m (b) r_d (c) Z_i (d) Z_o (e) A_v (f) A_v ignoring the effect of r_d*

Solution:

(a) $$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(10\text{ mA})}{8\text{ V}} = 2.5\text{ mS}$$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 2.5\text{ mS}\left(1 - \frac{(-2\text{ V})}{(-8\text{ V})}\right) = \mathbf{1.88\text{ mS}}$$

(b) $$r_d = \frac{1}{y_{os}} = \frac{1}{40\ \mu\text{S}} = \mathbf{25\ k\Omega}$$

(c) $Z_i = R_G = \mathbf{1\ M\Omega}$

(d) $Z_o = R_D \| r_d = 2\text{ k}\Omega \| 25\text{ k}\Omega = \mathbf{1.85\ k\Omega}$

(e) $A_v = -g_m(R_D \| r_d) = -(1.88\text{ mS})(1.85\text{ k}\Omega)$
$= \mathbf{-3.48}$

(f) $A_v = -g_m R_D = -(1.88\text{ mS})(2\text{ k}\Omega) = \mathbf{-3.76}$

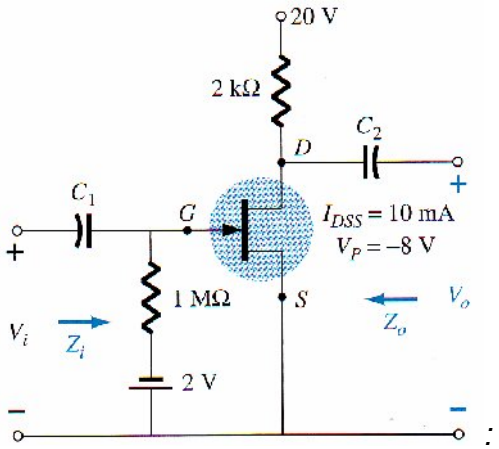


Fig9-13 Ex7

2-JFET Self-Bias Configuration (Common-Source)
Bypassed R_S

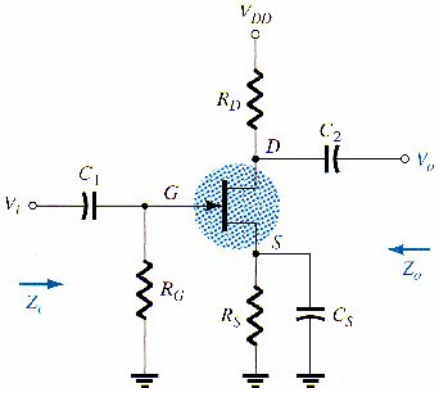


Fig9-14 Self-bias JFET configuration

Since the resulting configuration is the same as fig9-12, i.e. Z_i, Z_o & A_v will be the same

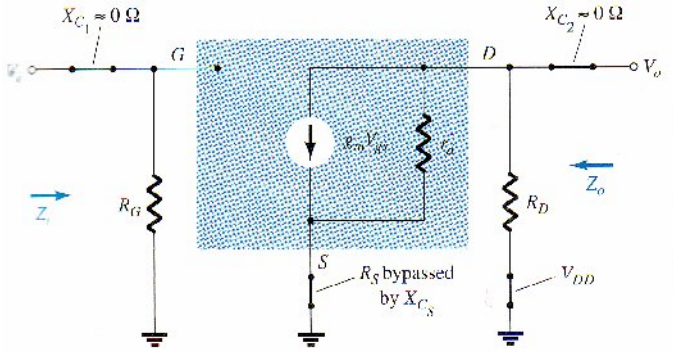


Fig 9-15 ac equivalent circuit

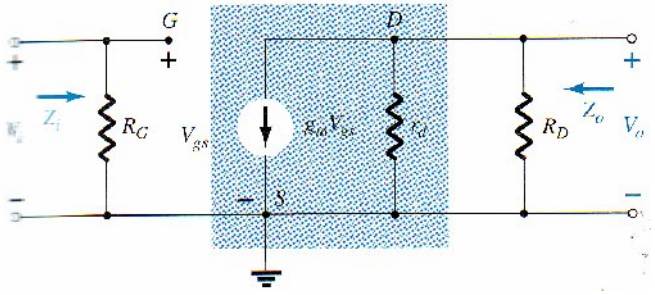


Fig 9-16 Redrawn network

$$Z_i = R_G \qquad [9\text{-}18]$$

$$Z_o = r_d \| R_D \qquad [9\text{-}19]$$

$$Z_o \cong R_D \quad r_d \geq 10R_D \qquad [9\text{-}20]$$

$$A_v = -g_m(r_d \| R_D) \qquad [9\text{-}21]$$

$$A_v = -g_m R_D \quad r_d \geq 10R_D \qquad [9\text{-}22]$$

Phase Relationship: *the* ***negative sign*** *in A_v means 180° phase shift between IP & OP*

Un-bypassed R_S

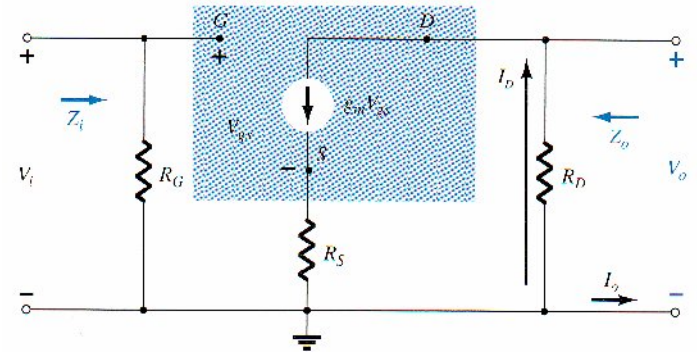


Fig9-17JFET with effect of R_S with r_d=∞Ω

Due to the open-circuit condition between the gate and the output network, Z_i=

$$Z_i = R_G \qquad [9\text{-}23]$$

$$Z_o = \left.\frac{V_o}{I_o}\right|_{V_i=0}$$ *Setting V_i=0V will result in the gate terminal being at ground potential(0V).The voltage across R_G is 0V, R_G "shorted out" of the picture. Applying KCL will result*

$$I_o + I_D = g_m V_{gs}$$

$$V_{gs} = -(I_o + I_D)R_S$$

$$I_o + I_D = -g_m(I_o + I_D)R_S = -g_m I_o R_S - g_m I_D R_S$$

$$I_o[1 + g_m R_S] = -I_D[1 + g_m R_S]$$

$$V_o = -I_D R_D$$

$$V_o = -(-I_o)R_D = I_o R_D$$

$$Z_o = \frac{V_o}{I_o} = R_D \qquad r_d = \infty\ \Omega$$

[9-24]

If r_d is included in the network, the equivalent will appear as shown in fig9-18

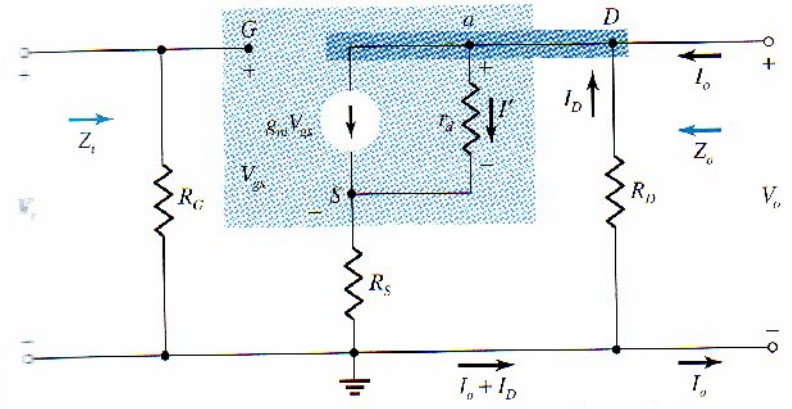


Fig9-18 r_d effect in self-bias JFET

$$Z_o = \left.\frac{V_o}{I_o}\right|_{V_i=0\text{ V}} = -\frac{I_D R_D}{I_o}$$ *We try to find an expression for I_o in terms of I_D applying KCL:*

$$I_o = g_m V_{gs} + I_{r_d} - I_D$$

$$V_{r_d} = V_o + V_{gs}$$

$$I_o = g_m V_{gs} + \frac{V_o + V_{gs}}{r_d} - I_D$$

$$I_o = \left(g_m + \frac{1}{r_d}\right)V_{gs} - \frac{I_D R_D}{r_d} - I_D \text{ using } V_o = -I_D R_D$$

$$V_{gs} = -(I_D + I_o)R_S$$

$$I_o = -\left(g_m + \frac{1}{r_d}\right)(I_D + I_o)R_S - \frac{I_D R_D}{r_d} - I_D$$

$$I_o\left[1 + g_m R_S + \frac{R_S}{r_d}\right] = -I_D\left[1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d}\right]$$

$$I_o = \frac{-I_D\left[1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d}\right]}{1 + g_m R_S + \frac{R_S}{r_d}}$$

$$Z_o = \frac{V_o}{I_o} = \frac{-I_D R_D}{\dfrac{-I_D\left(1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d}\right)}{1 + g_m R_S + \frac{R_S}{r_d}}}$$

$$Z_o = \frac{\left[1 + g_m R_S + \frac{R_S}{r_d}\right]}{\left[1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d}\right]} R_D \qquad \textit{[9-25a]}$$

For $r_d \geq 10R_D$, $\left(1 + g_m R_S + \frac{R_S}{r_d}\right) \gg \frac{R_D}{r_d}$ and $1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d}$

$\cong 1 + g_m R_S + \frac{R_S}{r_d}$ and

$$Z_o = R_D \Big|_{r_d \geq 10R_D} \qquad \textit{[9-25b]}$$

A_v: *for the network of fig9-18, applications of KVL on the input circuit result in:*

$$V_i - V_{gs} - V_{R_S} = 0$$

$$V_{gs} = V_i - I_D R_S$$

Voltage across r_d applying KVL

$$V_o - V_{R_S}$$

$$I' = \frac{V_o - V_{R_S}}{r_d}$$

Applying KCL will result

$$I_D = g_m V_{gs} + \frac{V_o - V_{R_S}}{r_d}$$

Substituting for V_{gs} from above and substituting for V_o and V_{RS} we have

$$I_D = g_m[V_i - I_D R_S] + \frac{(-I_D R_D) - (I_D R_S)}{r_d}$$

$$I_D\left[1 + g_m R_S + \frac{R_D + R_S}{r_d}\right] = g_m V_i$$

$$I_D = \frac{g_m V_i}{1 + g_m R_S + \frac{R_D + R_S}{r_d}}$$

The output voltage V_o is

$$= -I_D R_D = -\frac{g_m R_D V_i}{1 + g_m R_S + \frac{R_D + R_S}{r_d}}$$

$$A_v = \frac{V_o}{V_i} = -\frac{g_m R_D}{1 + g_m R_S + \dfrac{R_D + R_S}{r_d}} \qquad [9\text{-}26]$$

$$A_v = \frac{V_o}{V_i} = -\frac{g_m R_D}{1 + g_m R_S} \qquad r_d \geq 10(R_D + R_S) \qquad [9\text{-}27]$$

Phase Relationship: *the* ***negative sign*** *in A_v means 180° phase shift between IP & OP*

Example 8: *configuration of fig9-19 has V_{GSQ}=-2.6V & I_{DQ}=2.6mA, with I_{DSS}=8mA & V_P=-6V. The network is redrawn as fig9-20 with an applied signal V_i. The value of y_{os} is given as 20μS, Determine (a) g_m (b) r_d (c) Z_i (d) Z_o with and without r_d (e) A_v with and without r_d*

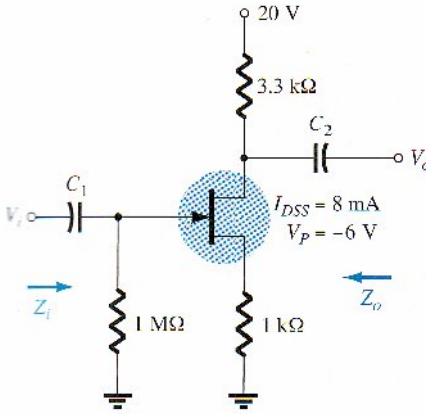


Fig9-19Ex8

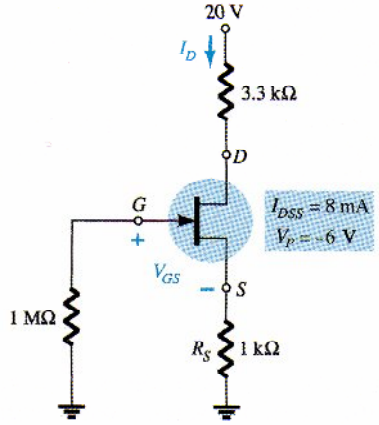


Fig9-20 Redrawn Ex8:

Solution:

(a) $$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(8\text{ mA})}{6\text{ V}} = 2.67\text{ mS}$$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 2.67\text{ mS}\left(1 - \frac{(-2.6\text{ V})}{(-6\text{ V})}\right) = \mathbf{1.51\text{ mS}}$$

(b) $$r_d = \frac{1}{y_{os}} = \frac{1}{20\ \mu\text{S}} = \mathbf{50\ k\Omega}$$

(c) $Z_i = R_G = \mathbf{1\ M\Omega}$

(d) With r_d:

$$r_d = 50\text{ k}\Omega > 10R_D = 33\text{ k}\Omega$$

Therefore,

$$Z_o = R_D = \mathbf{3.3\ k\Omega}$$

If $r_d = \infty\ \Omega$

$$Z_o = R_D = \mathbf{3.3\ k\Omega}$$

(e) With r_d:

$$A_v = \frac{-g_m R_D}{1 + g_m R_S + \dfrac{R_D + R_S}{r_d}} = \frac{-(1.51\text{ mS})(3.3\text{ k}\Omega)}{1 - (1.51\text{ mS})(1\text{ k}\Omega) + \dfrac{3.3\text{ k}\Omega + 1\text{ k}\Omega}{50\text{ k}\Omega}}$$

$$= \mathbf{-1.92}$$

Without r_d:

$$A_v = \frac{-g_m R_D}{1 + g_m R_S} = \frac{-(1.51\text{ mS})(3.3\text{ k}\Omega)}{1 + (1.51\text{ mS})(1\text{ k}\Omega)} = \mathbf{-1.98}$$

3-JFET Voltage-Divide Configuration (Common-Source)

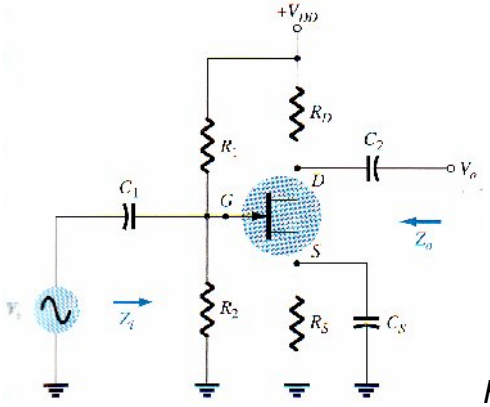


Fig9-21 JFET voltage-divider configuration

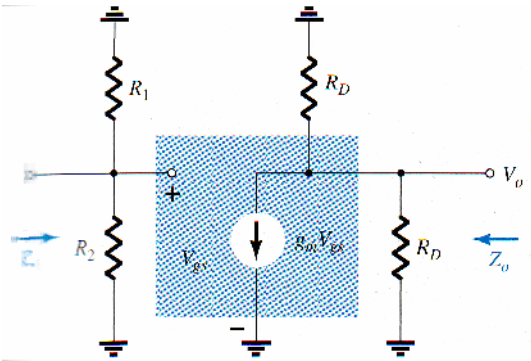


Fig9-22 Network under ac conditions

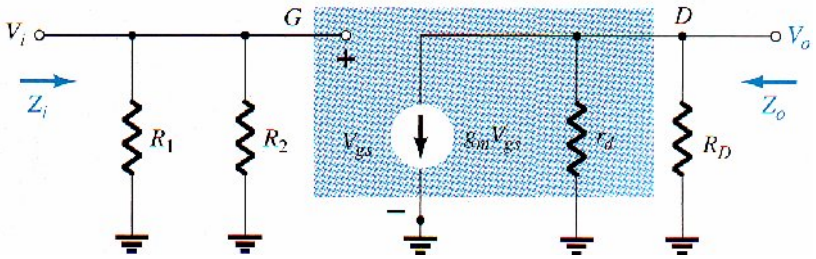


Fig9-23 Redrawn network

$$Z_i = R_1 \| R_2 \qquad [9\text{-}28]$$

$$Z_o = r_d \| R_D \qquad [9\text{-}29]$$

$$Z_o \cong R_D \quad r_d \geq 10R_D \qquad [9\text{-}30]$$

$$V_{gs} = V_i$$

$$V_o = -g_m V_{gs}(r_d \| R_D)$$

$$A_v = \frac{V_o}{V_i} = \frac{-g_m V_{gs}(r_d \| R_D)}{V_{gs}}$$

$$A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D) \qquad [9\text{-}31]$$

$$A_v = \frac{V_o}{V_i} \cong -g_m R_D \quad r_d \geq 10R_D \qquad [9\text{-}32]$$

4-JFET Source-Follower (Common-Drain Configuration)

The output is taken off the source terminal and when the dc supply is replaced by it's short-circuit equivalent, the drain is grounded (hence, the terminology common-drain)

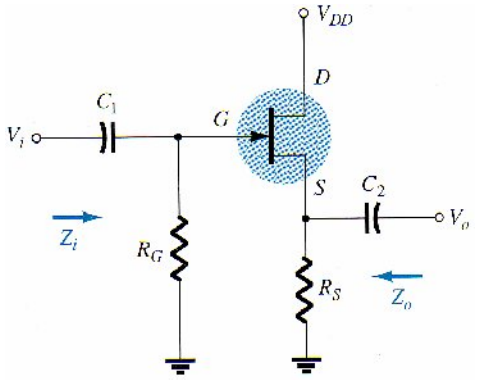


Fig9-24 JFET Source-Follower configuration

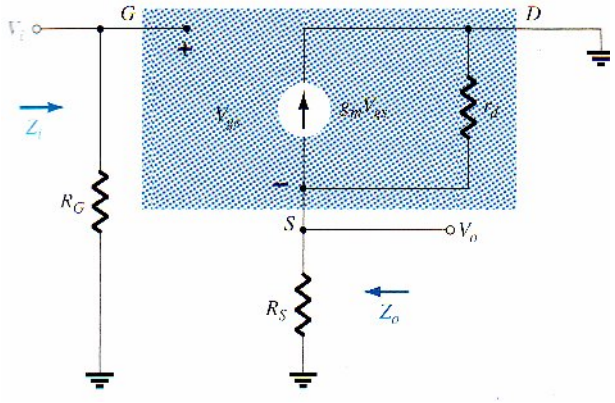


Fig9-25 JFET ac equivalent model

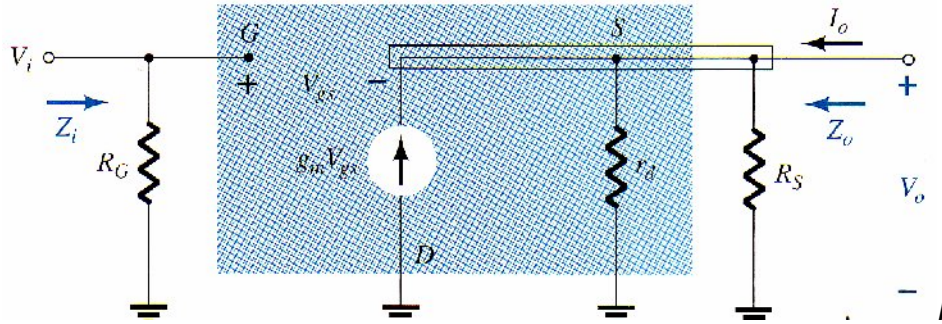
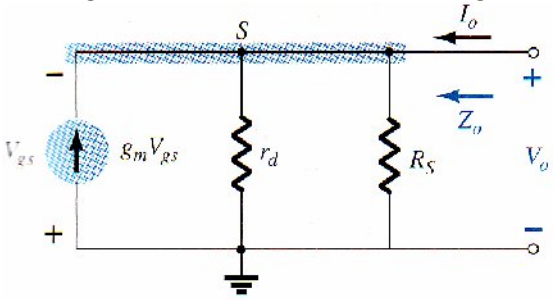


Fig9-26 redrawn the network

$$Z_i = R_G$$

[9-33]

Setting V_i = 0V will result in the gate terminal being connected directly to ground so that Z_o=



V_o= -V_{gs} applying KCL at node S

$$I_o + g_m V_{gs} = I_{r_d} + I_{R_S}$$

$$= \frac{V_o}{r_d} + \frac{V_o}{R_S}$$

$$I_o = V_o\left[\frac{1}{r_d} + \frac{1}{R_S}\right] - g_m V_{gs}$$

$$= V_o\left[\frac{1}{r_d} + \frac{1}{R_S}\right] - g_m[-V_o]$$

$$= V_o\left[\frac{1}{r_d} + \frac{1}{R_S} + g_m\right]$$

$$Z_o = \frac{V_o}{I_o} = \frac{V_o}{V_o\left[\frac{1}{r_d} + \frac{1}{R_S} + g_m\right]} = \frac{1}{\frac{1}{r_d} + \frac{1}{R_S} + g_m} = \frac{1}{\frac{1}{r_d} + \frac{1}{R_S} +}$$

$$Z_o = r_d \| R_S \| 1/g_m$$

[9-34]

$$Z_o \cong R_S \| 1/g_m \qquad r_d \geq 10R_S \qquad [9\text{-}35]$$

$$V_o = g_m V_{gs}(r_d \| R_S)$$

Applying KVL around the perimeter of the network of fig9-26 will result in:

$$V_i = V_{gs} + V_o$$

$$V_{gs} = V_i - V_o$$

$$V_o = g_m(V_i - V_o)(r_d \| R_S)$$

$$V_o = g_m V_i(r_d \| R_S) - g_m V_o(r_d \| R_S)$$

$$V_o[1 + g_m(r_d \| R_S)] = g_m V_i(r_d \| R_S)$$

$$A_v = \frac{V_o}{V_i} = \frac{g_m(r_d \| R_S)}{1 + g_m(r_d \| R_S)} \qquad [9\text{-}36]$$

$$A_v = \frac{V_o}{V_i} \cong \frac{g_m R_S}{1 + g_m R_S} \qquad r_d \geq 10R_S \qquad [9\text{-}37]$$

Since the bottom of Eq[9-37] is larger than the numerator by a factor of one, the gain can never be equal to or greater than one

Phase Relationship: *since* ***A_v is a positive quantity****, V_o and V_i are in phase*

Example 9: *A dc analysis of fig9-27 will result in V_{GSQ} = -2.86V & I_{DQ}=4.56mA, Determine (a) g_m (b) r_d (c) Z_i (d) Z_o with and without r_d (e) A_v with and without r_d*

Solution:

a) $$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(16\text{ mA})}{4\text{ V}} = 8\text{ mS}$$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 8\text{ mS}\left(1 - \frac{(-2.86\text{ V})}{(-4\text{ V})}\right) = \mathbf{2.28\text{ mS}}$$

b) $$r_d = \frac{1}{y_{os}} = \frac{1}{25\ \mu\text{S}} = \mathbf{40\ k\Omega}$$

c) $Z_i = R_G = \mathbf{1\ M\Omega}$

d) With r_d:

$$Z_o = r_d \| R_S \| 1/g_m = 40\text{ k}\Omega \| 2.2\text{ k}\Omega \| 1/2.28\text{ mS}$$
$$= 40\text{ k}\Omega \| 2.2\text{ k}\Omega \| 438.6\ \Omega$$
$$= \mathbf{362.52\ \Omega}$$

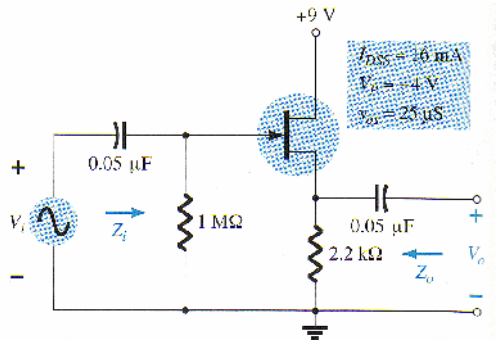


Fig9-27 Ex9:

Without r_d

$$Z_o = R_S \| 1/g_m = 2.2\text{ k}\Omega \| 438.6\ \Omega = \mathbf{365.69\ \Omega}$$

e) With r_d

$$A_v = \frac{g_m(r_d \| R_S)}{1 + g_m(r_d \| R_S)} = \frac{(2.28\text{ mS})(40\text{ k}\Omega \| 2.2\text{ k}\Omega)}{1 + (2.28\text{ mS})(40\text{ k}\Omega \| 2.2\text{ k}\Omega)}$$

$$= \frac{(2.28\text{ mS})(2.09\text{ k}\Omega)}{1 + (2.28\text{ mS})(2.09\text{ k}\Omega)} = \frac{4.77}{1 + 4.77} = \mathbf{0.83}$$

Without r_d:

$$A_v = \frac{g_m R_S}{1 + g_m R_S} = \frac{(2.28\ \text{mS})(2.2\ \text{k}\Omega)}{1 + (2.28\ \text{mS})(2.2\ \text{k}\Omega)}$$

$$= \frac{5.02}{1 + 5.02} = \mathbf{0.83}$$

Depletion-Type MOSFETs

The ac equivalent model for D-MOSFETs is exactly the same as that employed for JFETs as shown in fig9-28, the only difference is that V_{GSQ} can be positive for n-channel and negative for p-channel devices, the result is that g_m can be greater than g_{m0}

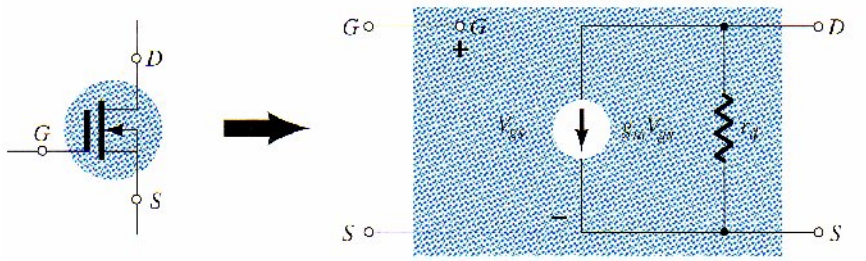


Fig9-28 D-MOSFET ac circuit

Example 10: *The network of fig9-29 was analyzed, resulting in V_{GSQ} = 0.35V & I_{DQ} = 7.6mA, Determine (a) g_m and compare to g_{mo} (b) r_d (c) Sketch the ac equivalent network (d) Z_i (e) Z_o (f) A_v*

Solution:

(a) $$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(6\ \text{mA})}{3\ \text{V}} = 4\ \text{mS}$$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 4\ \text{mS}\left(1 - \frac{(+0.35\ \text{V})}{(-3\ \text{V})}\right) = 4\ \text{mS}(1 + 0.117) = \mathbf{4.47\ mS}$$

(b) $$r_d = \frac{1}{y_{os}} = \frac{1}{10\ \mu\text{S}} = \mathbf{100\ k\Omega}$$

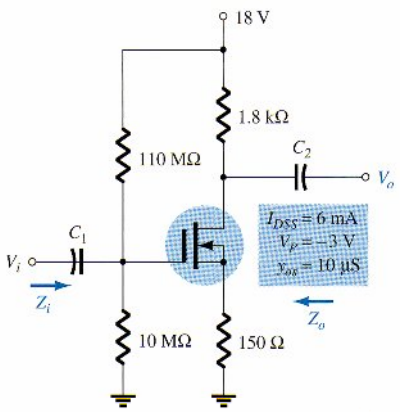


Fig9-29 network for Ex10:

(C) See fig9-30 the similarities with the network of JFET fixed bias, self bias (bypassed) & voltage divider configuration so that the same Equation applied

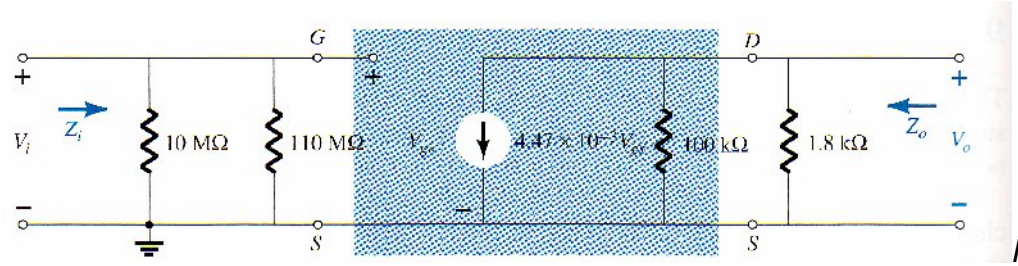


Fig9-30 ac equivalent

Enhancement-Type MOSFETs

For the E-MOSFETs, the relationship between output current and controlling voltage is

$$I_D = k(V_{GS} - V_{GS(\text{Th})})^2$$

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

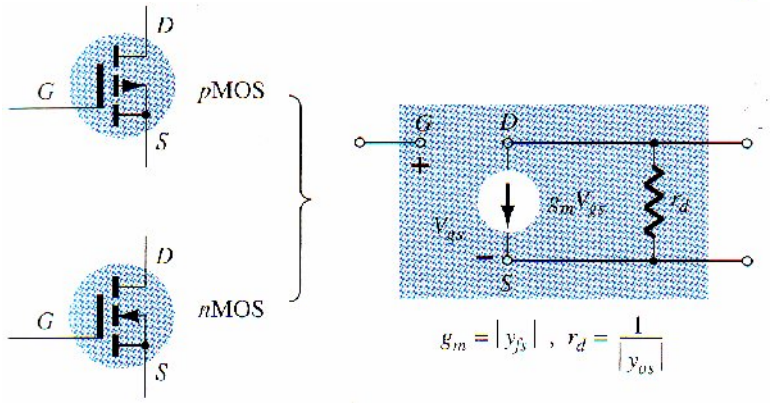


Fig 9-31 E-MOSFET ac circuit

$$g_m = \frac{dI_D}{dV_{GS}} = \frac{d}{dV_{GS}} k(V_{GS} - V_{GS(\text{Th})})^2 = k\frac{d}{dV_{GS}}(V_{GS} - V_{GS(\text{Th})})^2$$

$$= 2k(V_{GS} - V_{GS(\text{Th})})\frac{d}{dV_{GS}}(V_{GS} - V_{GS(\text{Th})}) = 2k(V_{GS} - V_{GS(\text{Th})})(1 - 0)$$

$$g_m = 2k(V_{GS_Q} - V_{GS(\text{Th})}) \qquad [9\text{-}38]$$

Can be determined from a given typical operating point on a specification sheet

1- E-MOSFET Voltage Divider Configuration

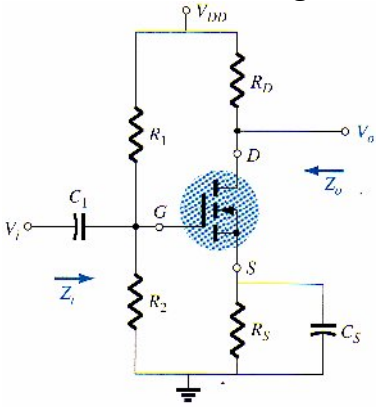


Fig9-32 E-MOSFET Voltage Divider

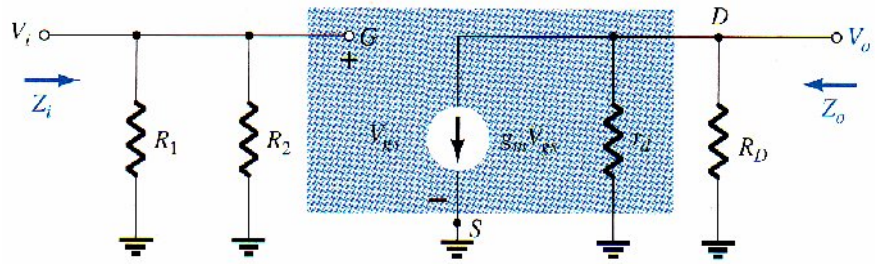


Fig9-33 ac equivalent circuit

$$Z_i = R_1 \| R_2 \qquad [9\text{-}39]$$

$$Z_o = r_d \| R_D \qquad [9\text{-}40]$$

$$Z_o \cong R_d \quad r_d \geq 10R_D \qquad [9\text{-}41]$$

$$A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D) \qquad [9\text{-}42]$$

$$A_v = \frac{V_o}{V_i} \cong -g_m R_D \qquad [9\text{-}43]$$

Designing FET Amplifier Network

Example 12: *Design the fixed-bias network of fig9-34 to have an ac gain of 10, that is determining the value of R_D*

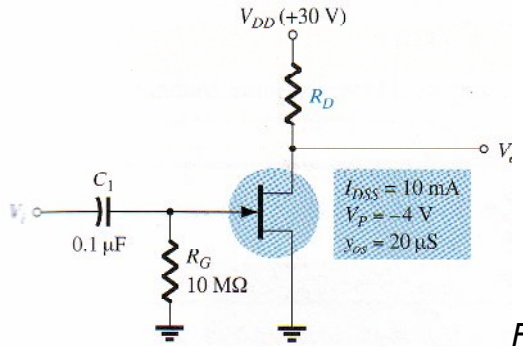


Fig 9-34 circuit for desired voltage gain in Ex11:

Solution:

$V_{GS_Q} = 0$ V, the level of g_m is g_{m0}. The gain is therefore determined by

$$A_v = -g_m(R_D \| r_d) = -g_{m0}(R_D \| r_d)$$

$$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(10\text{ mA})}{4\text{ V}} = 5\text{ mS}$$

$$-10 = -5\text{ mS}(R_D \| r_d)$$

$$R_D \| r_d = \frac{10}{5\text{ mS}} = 2\text{ k}\Omega$$

$$r_d = \frac{1}{y_{os}} = \frac{1}{20 \times 10^{-6}\text{ S}} = 50\text{ k}\Omega$$

$$R_D \| r_d = R_D \| 50\text{ k}\Omega = 2\text{ k}\Omega$$

$$\frac{R_D(50\text{ k}\Omega)}{R_D + 50\text{ k}\Omega} = 2\text{ k}\Omega$$

$$50R_D = 2(R_D + 50\text{ k}\Omega) = 2R_D + 100\text{ k}\Omega$$

$$48R_D = 100\text{ k}\Omega$$

$$R_D = \frac{100\text{ k}\Omega}{48} \cong 2.08\text{ k}\Omega$$

The closest standard value is 2KΩ, which would be employed for this region, the resulting level of V_{DSQ} would then be determined as follows:

$$V_{DS_Q} = V_{DD} - I_{D_Q}R_D = 30\text{ V} - (10\text{ mA})(2\text{ k}\Omega) = \mathbf{10\text{ V}}$$

Z_i and Z_o are set by the levels of R_G and R_D, respectively. That is,

$$Z_i = R_G = \mathbf{10\text{ M}\Omega}$$

$$Z_o = R_D \| r_d = 2\text{ k}\Omega \| 50\text{ k}\Omega = \mathbf{1.92\text{ k}\Omega} \cong R_D = 2\text{ k}\Omega$$

Example 13: *Choose the value of R_D and R_S for the network of fig 9-35 that will result in a gain of 8 using a relatively high level of g_m for this device defined at V_{GSQ} = 1/4 V_P*

Solution:

$$V_{GS_Q} = \frac{1}{4}V_P = \frac{1}{4}(-4\text{ V}) = -1\text{ V}$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS_Q}}{V_P}\right)^2 = 10\text{ mA}\left(1 - \frac{(-1\text{ V})}{(-4\text{ V})}\right)^2 = 5.625\text{ mA}$$

ing g_m,

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right)$$

$$= 5\text{ mS}\left(1 - \frac{(-1\text{ V})}{(-4\text{ V})}\right) = 3.75\text{ mS}$$

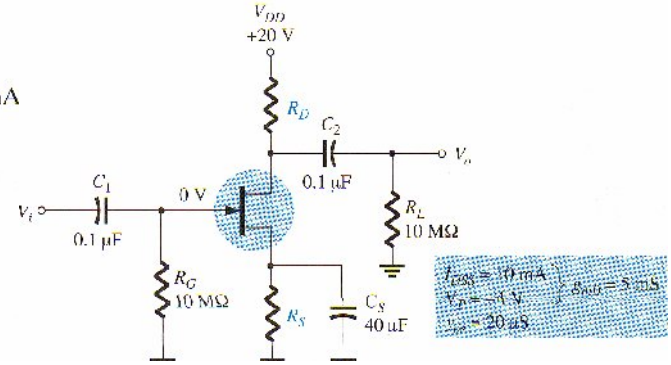


Fig9-35 network for desired voltage gain

$$|A_v| = g_m(R_D \| r_d)$$

$$8 = (3.75\text{ mS})(R_D \| r_d)$$

$$R_D \| r_d = \frac{8}{3.75\text{ mS}} = 2.13\text{ k}\Omega$$

$$r_d = \frac{1}{y_{os}} = \frac{1}{20\ \mu\text{S}} = 50\text{ k}\Omega$$

$$R_D \| 50\text{ k}\Omega = 2.13\text{ k}\Omega$$

$$R_D = \mathbf{2.2\ k\Omega}$$

$$V_{GS_Q} = -I_D R_S$$

$$-1\text{ V} = -(5.625\text{ mA})R_S$$

$$R_S = \frac{1\text{ V}}{5.625\text{ mA}} = 177.8\ \Omega$$

The closest standard value is 180Ω, in this example; R_S does not appear in the ac design because of the shorting effect of C_S

Example 13: *Determine R_D and R_S for the network of fig9-35 to establish a gain of 8 of the by-pass capacitor C_S is removed*

Solution: *V_{GSQ} and I_D are still -1V and 5.625mA, and since the equation V_{GS}=-$I_D R_S$ has not changed, R_S continues to equal the standard value of 180Ω*

$$A_v = -\frac{g_m R_D}{1 + g_m R_S}$$

$$|8| = \left|\frac{-(3.75\text{ mS})R_D}{1 + (3.75\text{ mS})(180\ \Omega)}\right| = \frac{(3.75\text{ mS})R_D}{1 + 0.675}$$

$$8(1 + 0.675) = (3.75\text{ mS})R_D$$

$$R_D = \frac{13.4}{3.75\text{ mS}} = 3.573\text{ k}\Omega$$

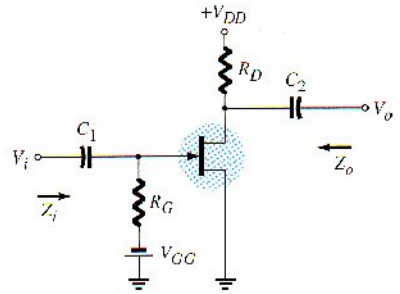
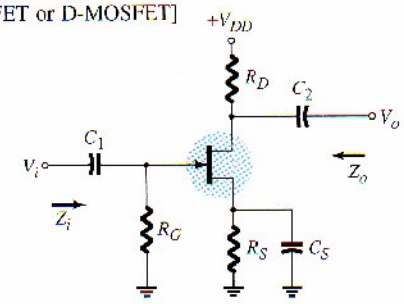
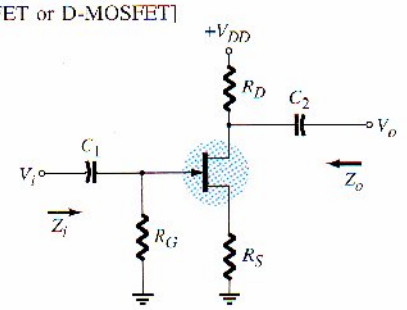
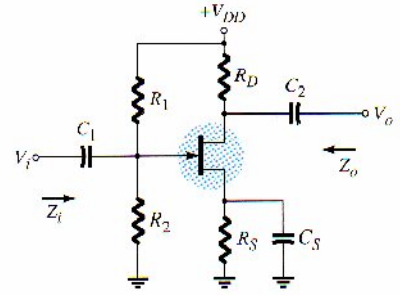
With the closest standard value at 3.6KΩ, we can now test the condition:

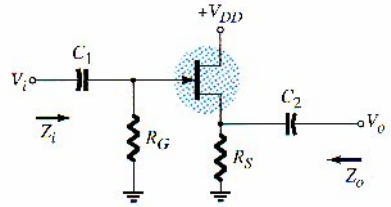
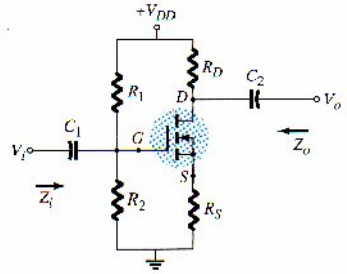
$$r_d \geq 10(R_D + R_S)$$

$$50\text{ k}\Omega \geq 10(3.6\text{ k}\Omega + 0.18\text{ k}\Omega) = 10(3.78\text{ k}\Omega)$$

$$50\text{ k}\Omega \geq 37.8\text{ k}\Omega$$

SUMMARY TABLE

Configuration	Z_i	Z_o	$A_v = \frac{V_o}{V_i}$
Fixed-bias [JFET or D-MOSFET] 	High (10 MΩ) $= R_G$	Medium (2 kΩ) $= R_D \| r_d$ $\cong R_D$ $(r_d \geq 10R_D)$	Medium (−10) $= -g_m(r_d \| R_D)$ $\cong -g_m R_D$ $(r_d \geq 10R_D)$
Self-bias bypassed R_S [JFET or D-MOSFET] 	High (10 MΩ) $= R_G$	Medium (2 kΩ) $= R_D \| r_d$ $\cong R_D$ $(r_d \geq 10R_D)$	Medium (−10) $= -g_m(r_d \| R_D)$ $\cong -g_m R_D$ $(r_d \geq 10R_D)$
Self-bias unbypassed R_S [JFET or D-MOSFET] 	High (10 MΩ) $= R_G$	$= \frac{\left[1 + g_m R_S + \frac{R_S}{r_d}\right] R_D}{\left[1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d}\right]}$ $= R_D$ $r_d \geq 10R_D$ or $r_d = \infty\Omega$	Low (−2) $= \frac{g_m R_D}{1 + g_m R_S + \frac{R_D - R_S}{r_d}}$ $\cong \frac{g_m R_D}{1 + g_m R_S}$ $[r_d \geq 10(R_D + R_S)]$
Voltage-divider bias [JFET or D-MOSFET] 	High (10 MΩ) $= R_1 \| R_2$	Medium (2 kΩ) $= R_D \| r_d$ $\cong R_D$ $(r_d \geq 10R_D)$	Medium (−10) $= -g_m(r_d \| R_D)$ $\cong -g_m R_D$ $(r_d \geq 10R_D)$

Configuration	Z_i	Z_o	$A_v = \frac{V_o}{V_i}$
Source-follower [JFET or D-MOSFET] 	High (10 MΩ) $= R_G$	Low (100 kΩ) $= r_d \| R_S \| 1/g_m$ $\cong R_S \| 1/g_m$ $(r_d \geq 10 R_S)$	Low (< 1) $= \frac{g_m(r_d \| R_S)}{1 + g_m(r_d \| R_S)}$ $\cong \frac{g_m R_S}{1 + g_m R_S}$ $(r_d \geq 10 R_S)$
Voltage-divider bias E-MOSFET 	Medium (1 MΩ) $= R_1 \| R_2$	Medium (2 kΩ) $= R_D \| r_d$ $\cong R_D$ $(R_d \geq 10 R_D)$	Medium (−10) $= -g_m(r_d \| R_D)$ $\cong -g_m R_D$ $(r_d \geq 10 R_D)$

Important Conclusion and Concept

1- The trans-conductance parameter g_m is determined by the ratio of the change in drain current associated with a particular change in gate-to-source voltage

2- On specification sheets, g_m is provided as y_{fs}

3-When V_{GS} is one-half the pinch-off value; g_m is one-half the maximum value

4- When I_D is one-fourth the saturation level of I_{DSS} , g_m is one-half the value at saturation

5- The output impedance of FETs is similar in magnitude to that of conventional BJTs

6- On specification sheets the output impedance r_d is provided as 1/ yos .

7- The voltage gain for the fixed-bias and self-bias JFET configurations (with a by passed source capacitance) is the same.

8- The ac analysis of JFETs and depletion-type MOSFETs is the same.

9- The ac equivalent network for E-MOSFETs is the same as that employed for the JFETs and D-MOSFETs, the only difference is the equation for g_m

10- The magnitude of the gain of FET networks is typically between 2 and 20. The self-bias configuration (without a bypass source capacitance) and the source follower are low-gain configurations

11- There is no phase shift between input and output for the source-follower

12- The output impedance for most FET configurations is determined primarily by R_D For the source-follower configuration it is determined by R_S and g_m

Equations

$$g_m = y_{fs} = \frac{\Delta I_D}{\Delta V_{GS}}$$

$$g_{m0} = \frac{2I_{DSS}}{|V_P|}$$

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right]$$

$$g_m = g_{m0}\sqrt{\frac{I_D}{I_{DSS}}}$$

$$r_d = \frac{1}{y_{os}} = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}=\text{constant}}$$

JFETs and depletion-type MOSFETs ($r_d \geq 10R_D$, $r_d \geq 10R_S$):

Fixed-bias:

$$Z_i = R_G$$
$$Z_o \cong R_D$$
$$A_v = -g_m R_D$$

Self-bias (bypassed R_S):

$$Z_i = R_G$$
$$Z_o \cong R_D$$
$$A_v = -g_m R_D$$

Self-bias (unbypassed R_S):

$$Z_i = R_G$$
$$Z_o = R_D$$
$$A_v \cong \frac{-g_m R_D}{1 + g_m R_S}$$

Voltage-divider bias:

$$Z_i = R_1 \| R_2$$
$$Z_o = R_D$$
$$A_v = -g_m R_D$$

Source-follower:

$$Z_i = R_G$$
$$Z_o = R_S \| 1/g_m$$
$$A_v = \frac{g_m R_S}{1 + g_m R_S}$$

Enhancement-type MOSFETs ($g_m = 2k(V_{GS_Q} - V_{GS(\text{Th})})$

Voltage-divider bias:

$$Z_i = R_1 \| R_2$$
$$Z_o \cong R_D$$
$$A_v = -g_m R_D$$