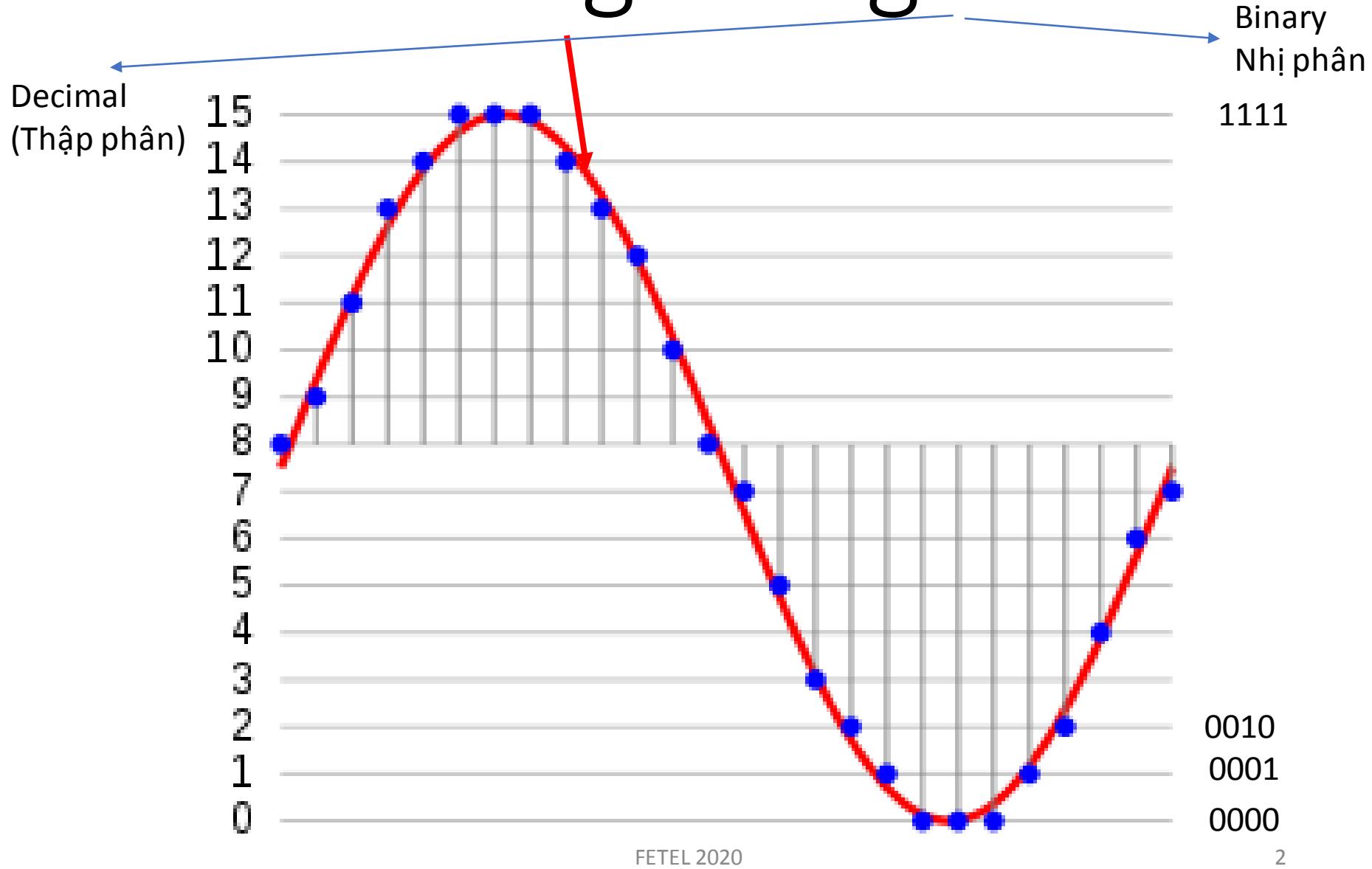


Digital Electronics

- What
- Why
- How

Analog & Digital

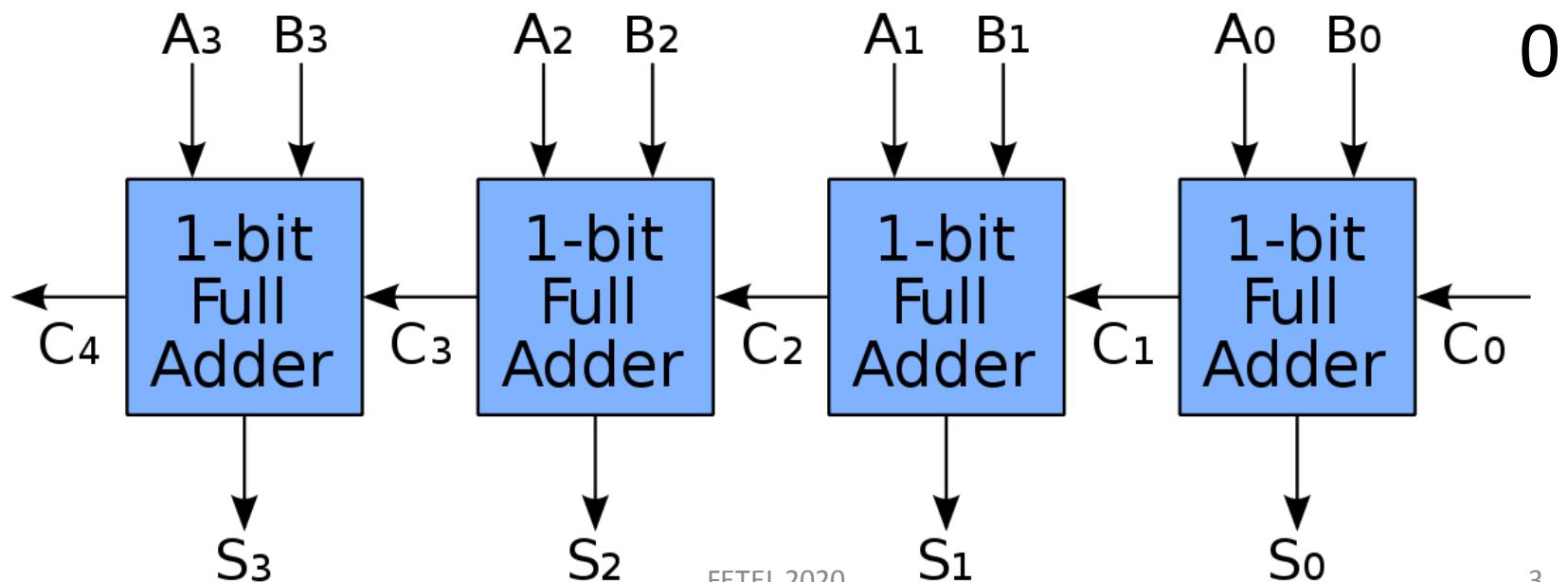


4 Bit Binary Adder

Ex: 0110

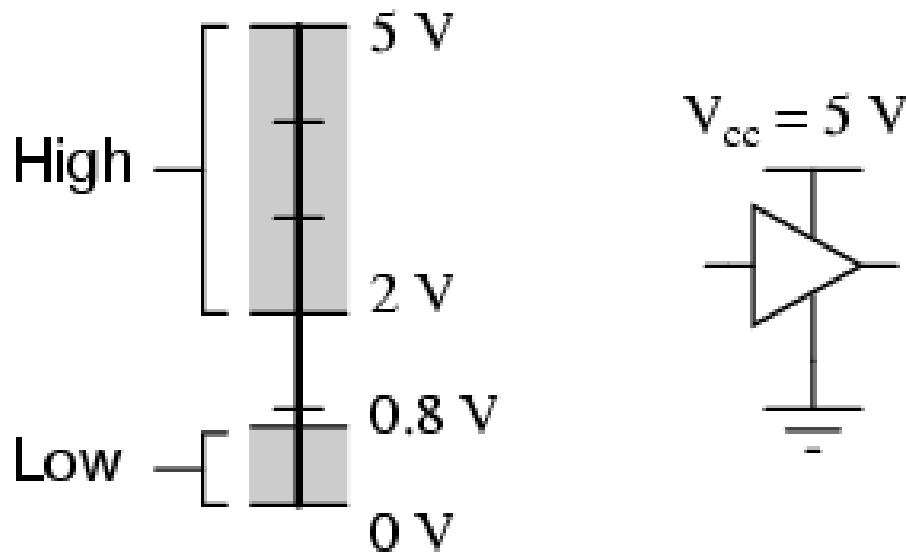
+

0101

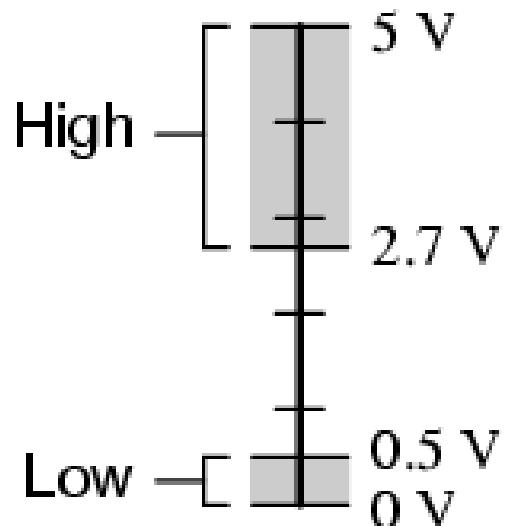


Logic 0 and Logic 1

*Acceptable TTL gate
input signal levels*



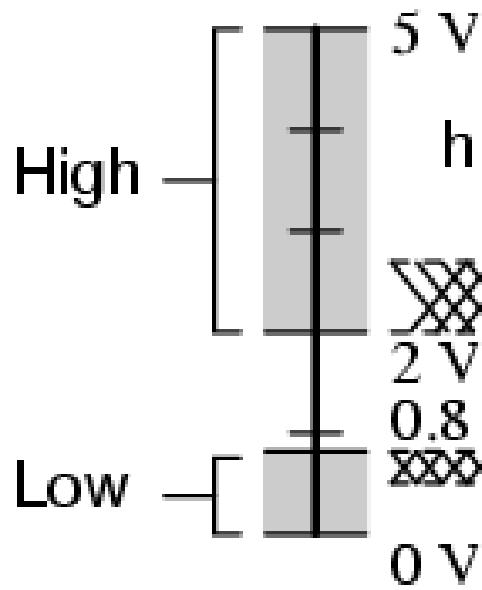
*Acceptable TTL gate
output signal levels*



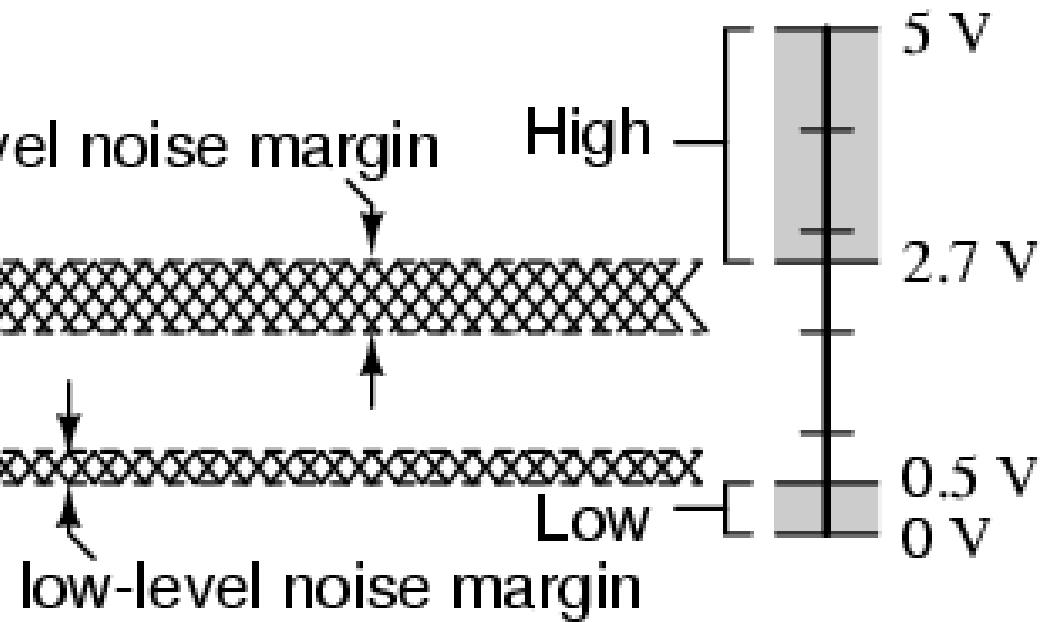
In this example, the range of input voltage (V_{ih}) can represent a HIGH (logic 1) is from 2 V to 5 V for the 5 V logic.....

Noise Margin

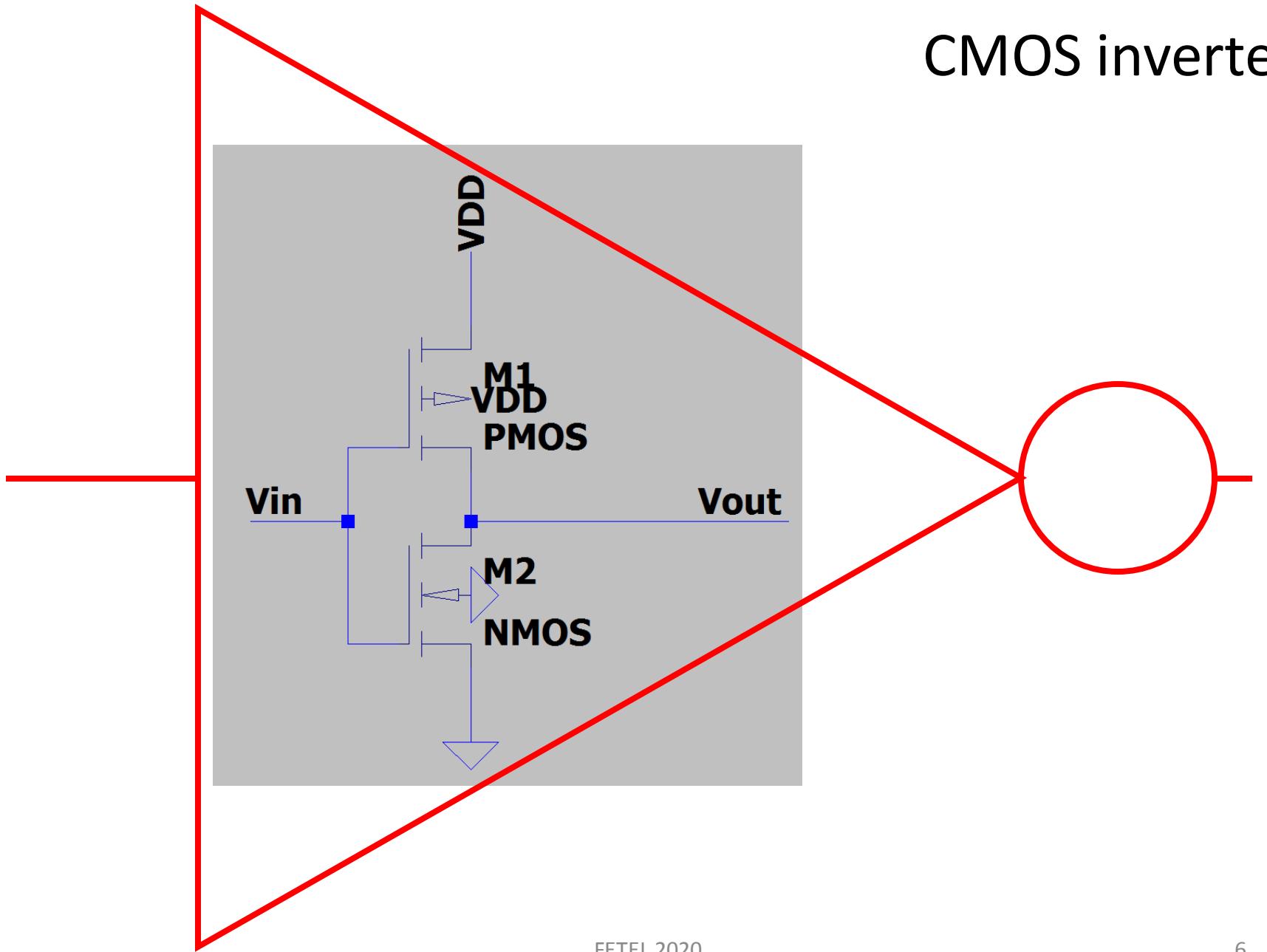
*Acceptable TTL gate
input signal levels*

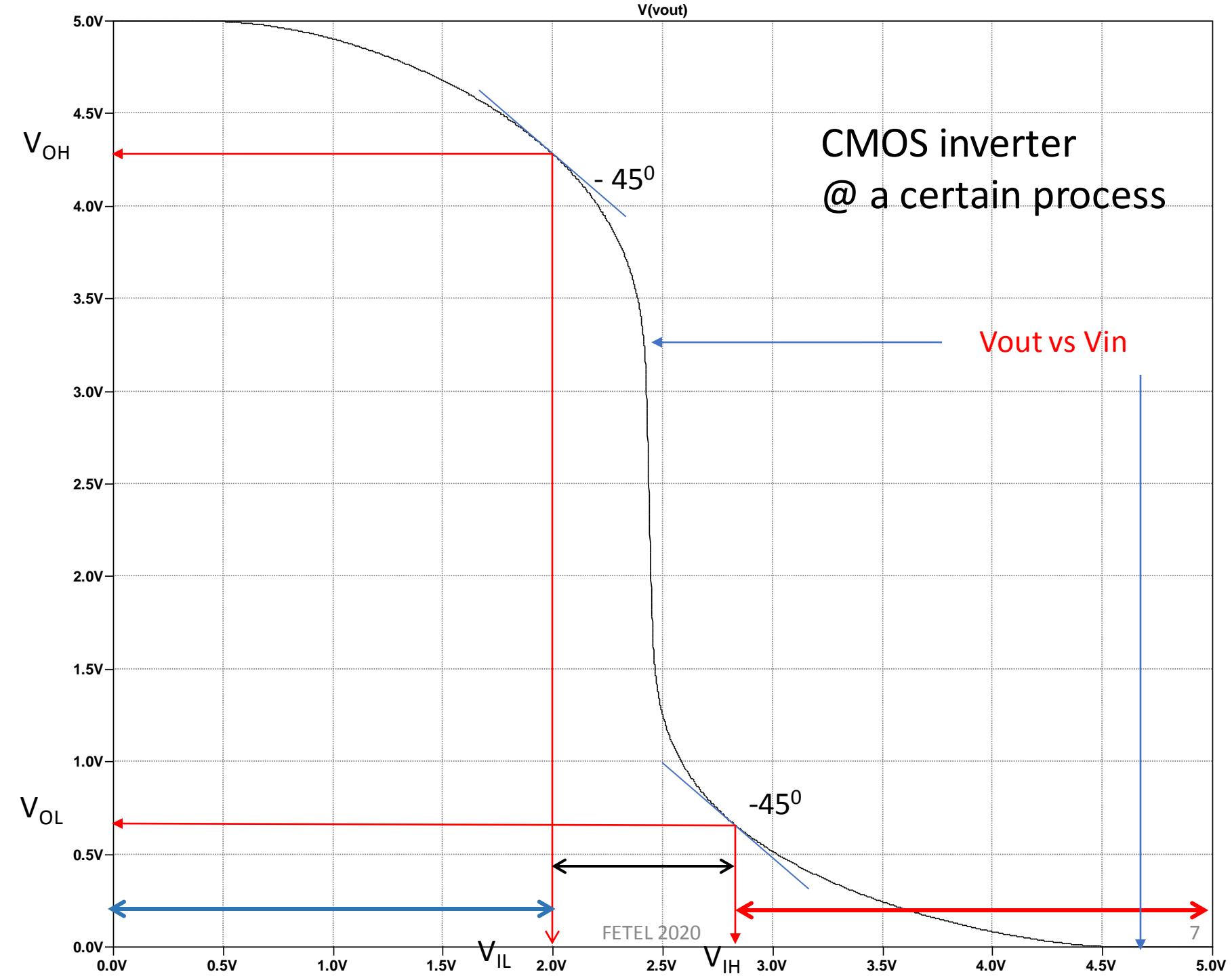


*Acceptable TTL gate
output signal levels*



CMOS inverter





How to find V_{IH} , V_{IL} , V_{OH} , V_{OL}

→ Datasheet



SN5404, SN54LS04, SN54S04, SN7404, SN74LS04, SN74S04 HEX INVERTERS

SDLS029C – DECEMBER 1983 – REVISED JANUARY 2004

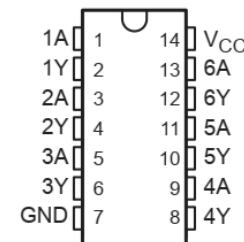
- Dependable Texas Instruments Quality and Reliability

description/ordering information

These devices contain six independent inverters.

SN5404 . . . J PACKAGE
SN54LS04, SN54S04 . . . J OR W PACKAGE
SN7404, SN74S04 . . . D, N, OR NS PACKAGE
SN74LS04 . . . D, DB, N, OR NS PACKAGE

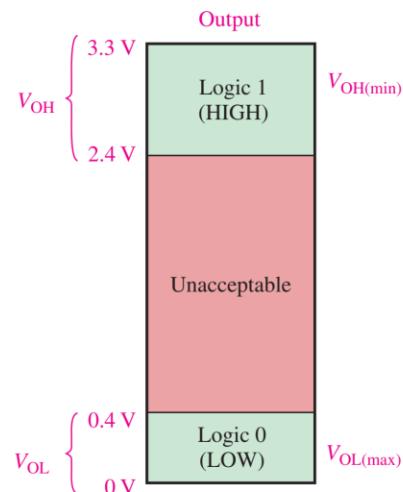
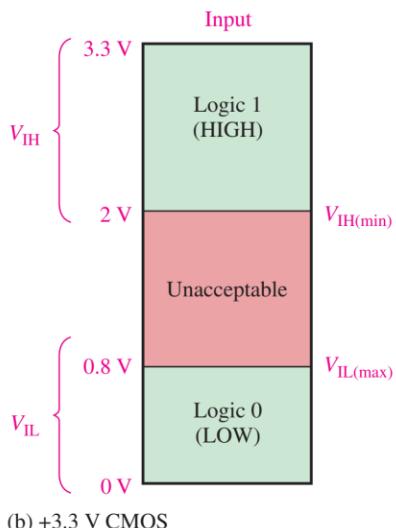
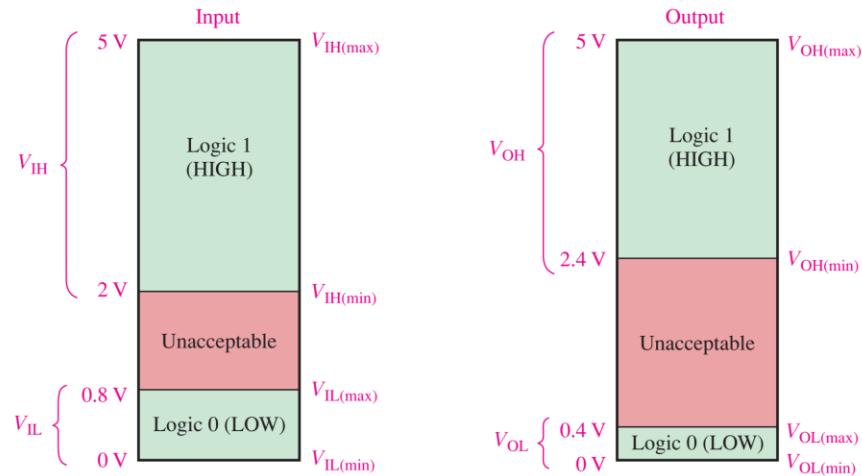
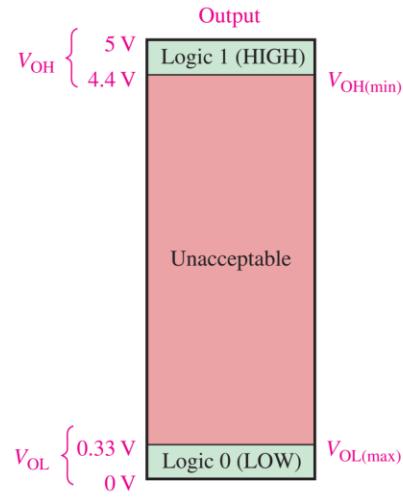
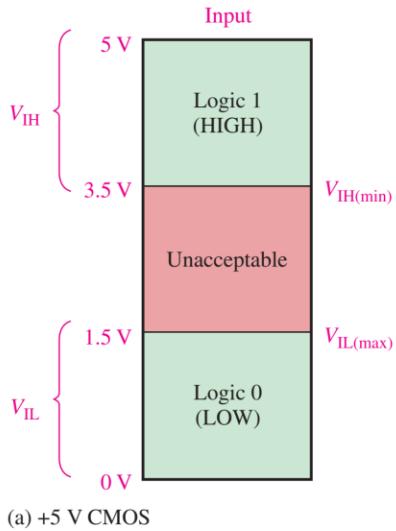
(TOP VIEW)



			SN54LS04			SN74LS04			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage				0.7			0.8	V

PARAMETER	TEST CONDITIONS†	SN54LS04			SN74LS04			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V
V _{OH}	V _{CC} = MIN, V _{IL} = MAX, I _{OH} = -0.4 mA	2.5	3.4		2.7	3.4		V
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V	I _{OL} = 4 mA	EFTPL 2020	0.25	0.4		0.48	V
		I _{OL} = 8 mA					0.25	

V_{IH} , V_{IL} , V_{OH} , V_{OL} of some technologies

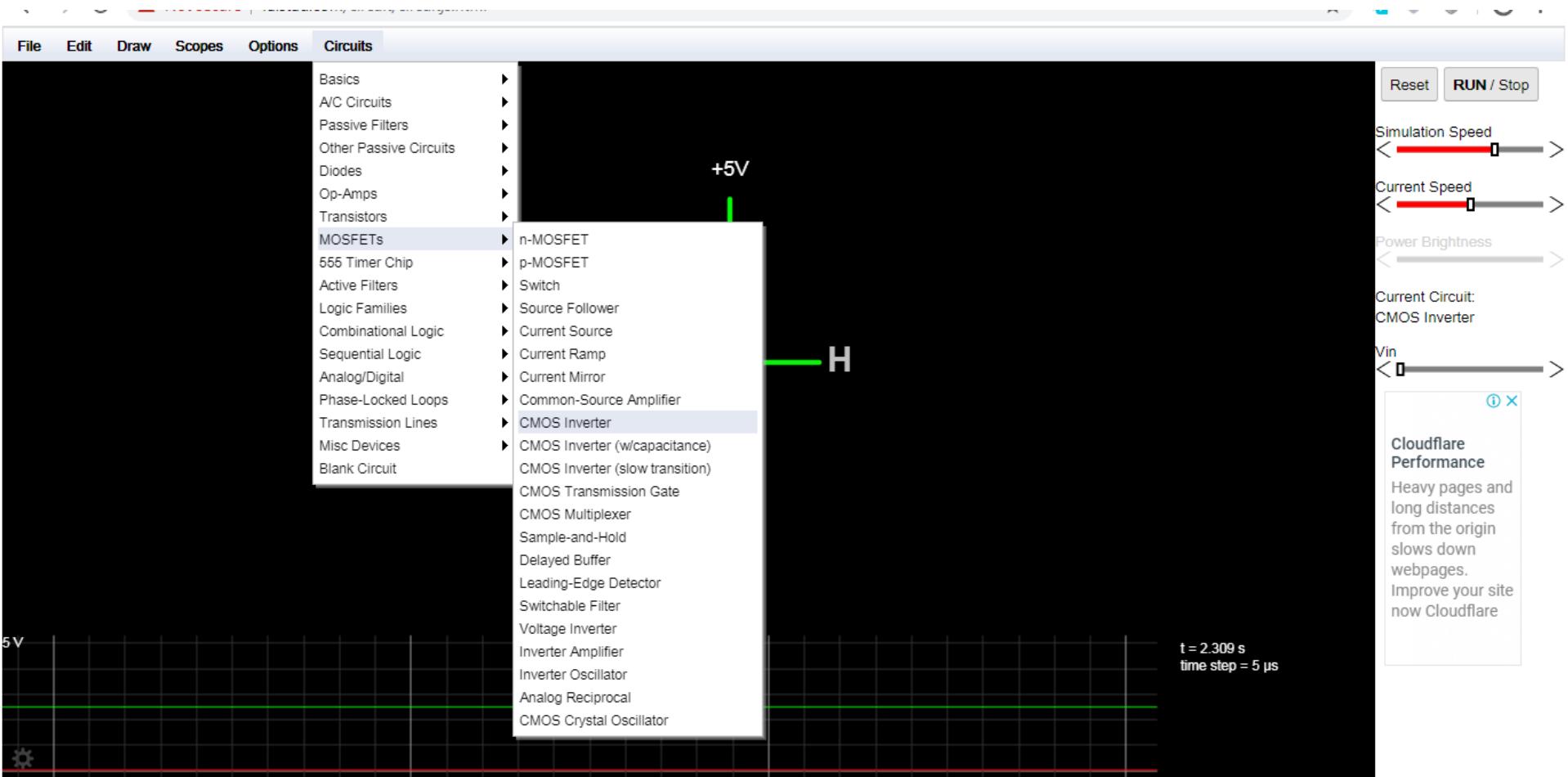


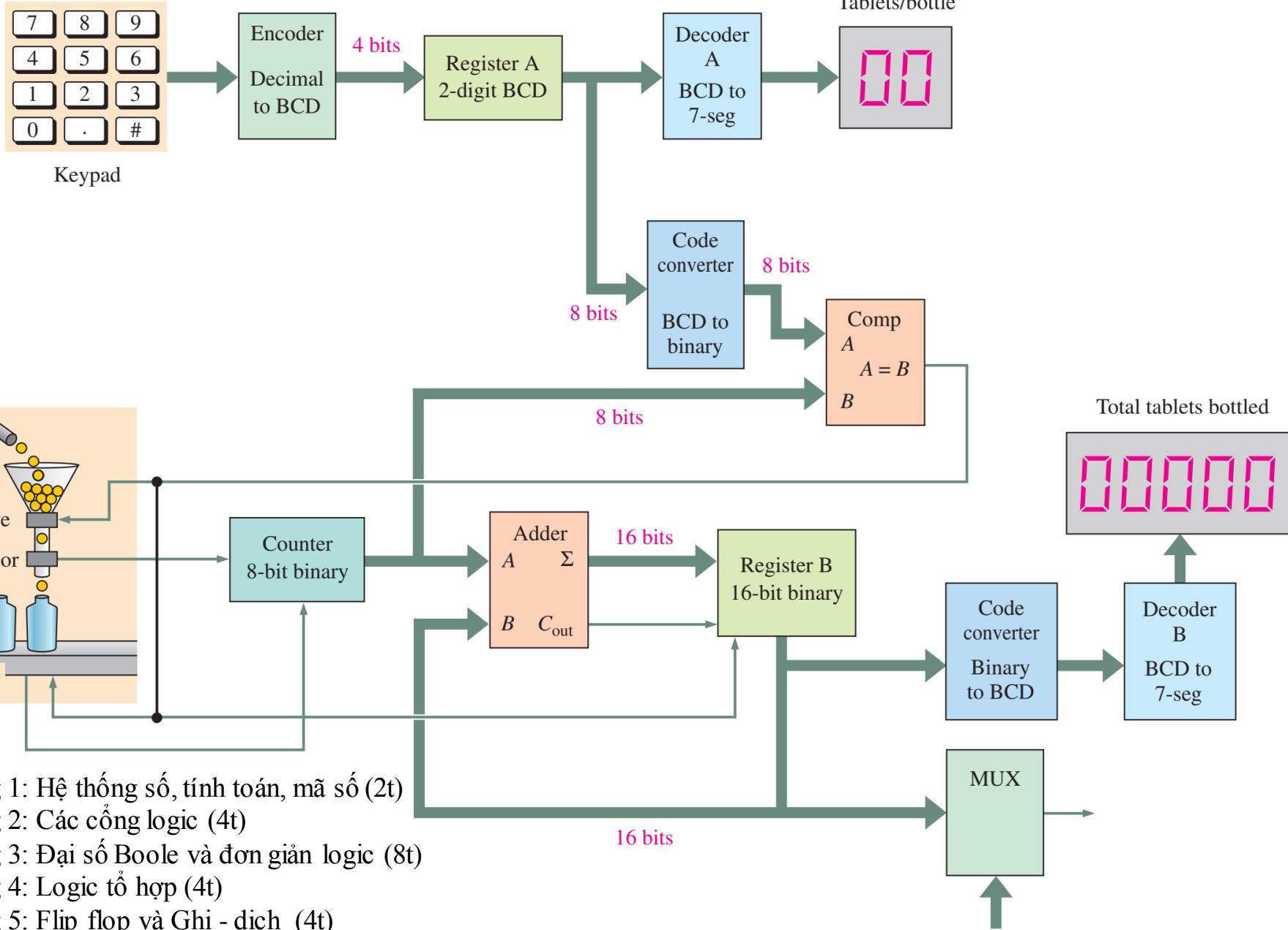
Input and output logic levels for TTL

Input and output logic levels for CMOS

Demo

- <http://www.falstad.com/circuit/circuitjs.html>





Chương 1: Hệ thống số, tính toán, mã số (2t)

Chương 2: Các cổng logic (4t)

Chương 3: Đại số Boole và đơn giản logic (8t)

Chương 4: Logic tổ hợp (4t)

Chương 5: Flip flop và Ghi - dịch (4t)

Chương 6: Mạch đếm (4t)

