4. Bipolar Junction Transistors

4.1 Basic Operation of the *npn* Bipolar Junction Transistor

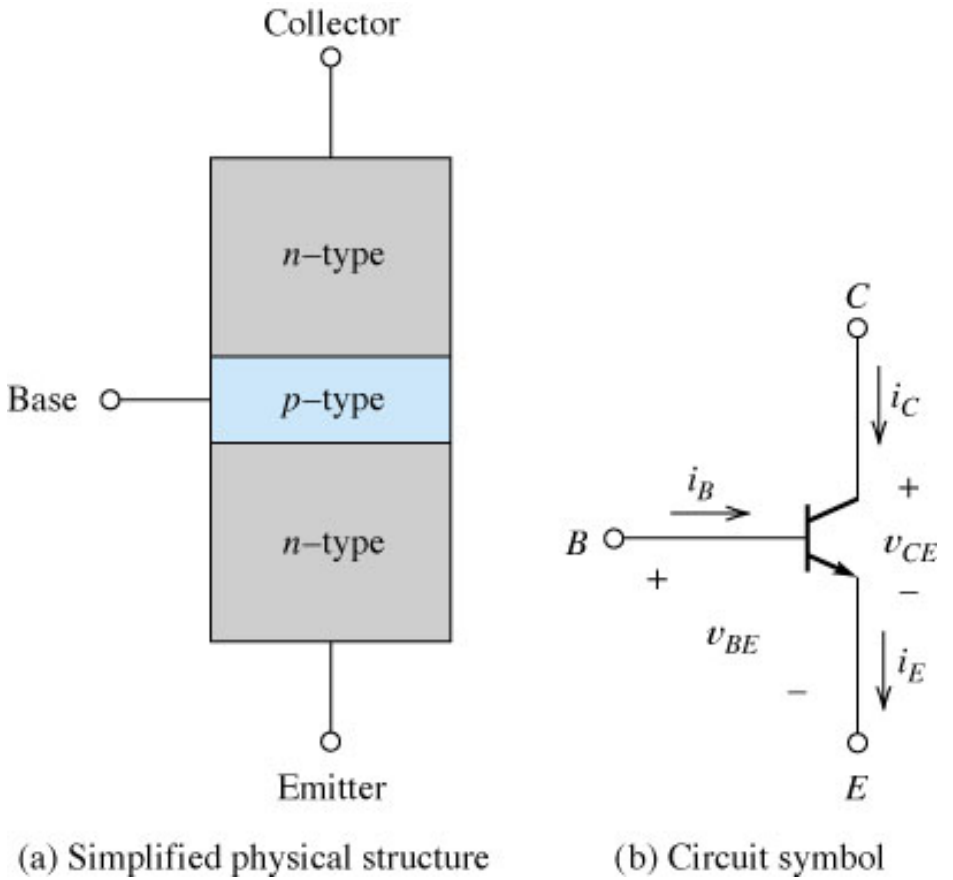


Figure 4.1 The *npn* BJT.

npn BJT consists of thin *p*-type layer between two *n*-type layers;

Layers: **emitter**, **base**, **collector**;

Two interacting *pn* junctions: emitter-base and base-collector;

Emitter region is doped very heavily, compared with the base region

Basic Operation in the Active region

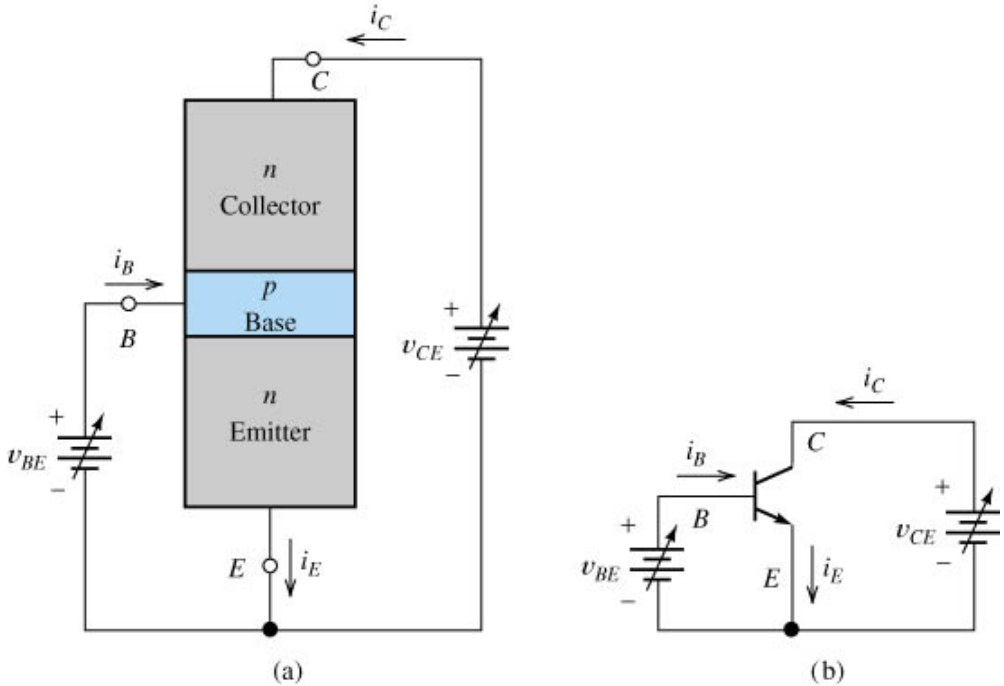


Figure 4.2 An *npn* transistor with variable biasing sources (common-emitter configuration).

Shokley equation for the emitter current

$$i_E = I_{ES}\left[\exp\left(\frac{v_{BE}}{V_T}\right) - 1\right] \qquad (4.1)$$

$I_{ES} = 10^{-12}$ .. 10^{-17}A – saturation current

$V_T = 26$mV – thermal voltage

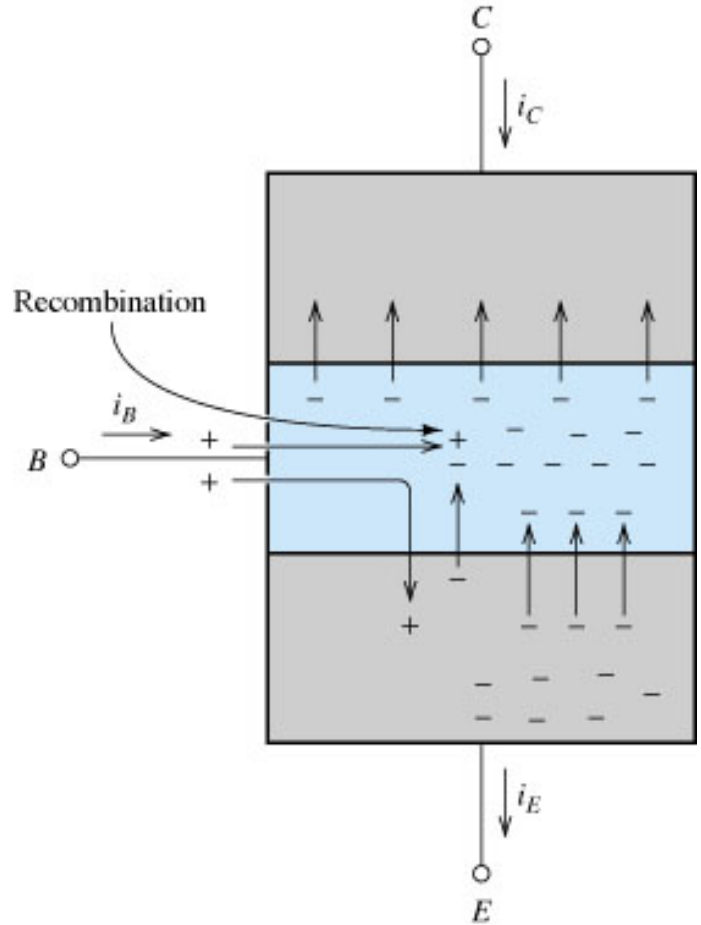


Figure 4.3 Current flow for an npn BJT in the active region. Most of the current is due to electrons moving from the emitter through the base to the collector. Base current consists of holes crossing from the base into the emitter and of holes that recombine with electrons in the base.

First - Order Common - Emitter Characteristics

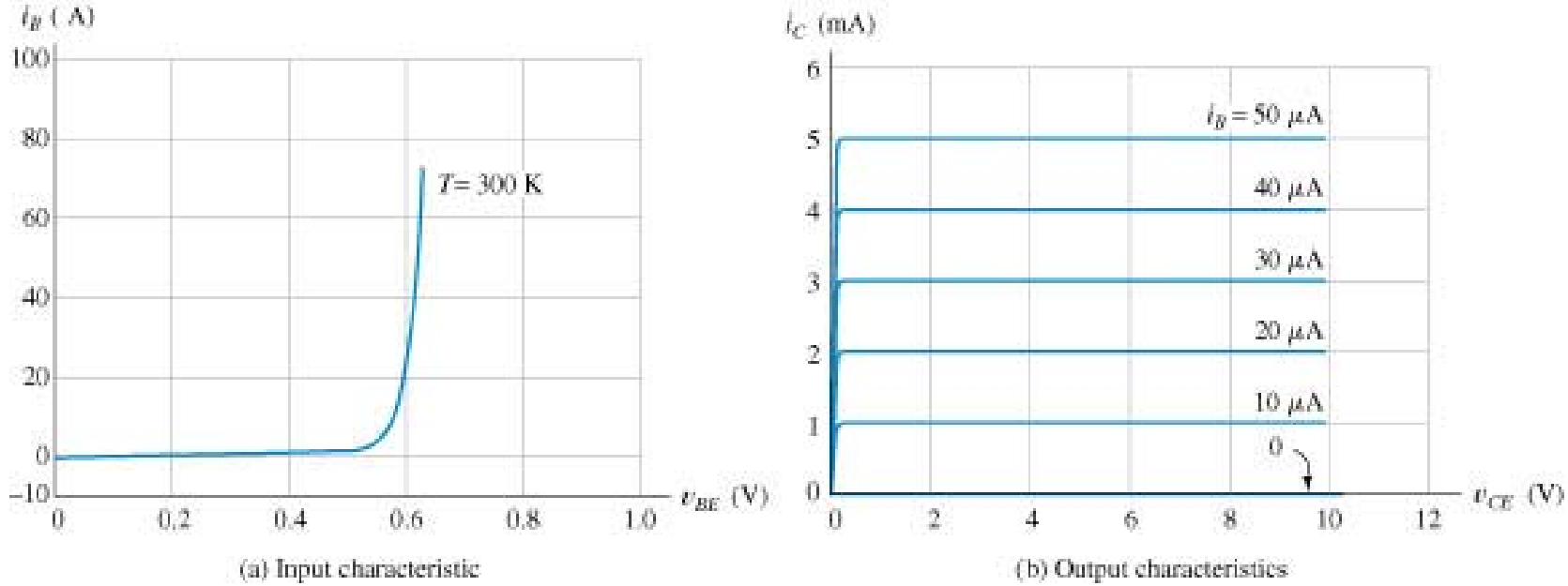


Figure 4.4 Common-emitter characteristics of a typical *npn* BJT.

Amplification by the BJT

In Figure 4.4: If $i_B = 30\mu A$, $i_C = 3mA$ – 100 times more

$$\beta = \frac{i_C}{i_B} \qquad (4.2)$$

β - **common-emitter current gain**.
Typically β = 10 .. 1000

Factors Affecting the Current Gain

- Doping of the emitter area compared with the base area
- Base region should be thin;
- Geometry of the device

Device Equations

$$i_E = i_C + i_B \tag{4.3}$$

$$\alpha = \frac{i_C}{i_E} \tag{4.4}$$

α - **common-base current gain**.
Typically α = 0.9 .. 0.999

$$i_C = \alpha I_{ES}\left[exp\left(\frac{v_{BE}}{V_T}\right) - 1\right] \tag{4.5}$$

$$I_s = \alpha I_{ES} \tag{4.6}$$

I_s – **scale current**

$$i_C \cong I_s \exp\left(\frac{v_{BE}}{V_T}\right) \tag{4.7}$$

$$i_B = (1-\alpha) i_E \tag{4.8}$$

$$i_B = (1-\alpha) I_{ES}\left[exp\left(\frac{v_{BE}}{V_T}\right) - 1\right] \tag{4.9}$$

$$i_C = \beta\, i_B \tag{4.11}$$

$$\beta = \frac{i_C}{i_B} = \frac{\alpha}{1-\alpha} \tag{4.10}$$

$$\alpha = \frac{\beta}{1+\beta}$$

Example 4.1 Using Device Curves to Determine α and β

Determine the values of α and β for the transistor with the characteristics shown in Figure 4.4.

Solution:

For example:

at v_{CE}=4 V and i_B=30 μA; i_C=3 mA;

$$\beta = \frac{i_C}{i_B} = \frac{3\ mA}{30\ \mu A} = 100$$

$$\alpha = \frac{\beta}{\beta + 1} = 0.99$$

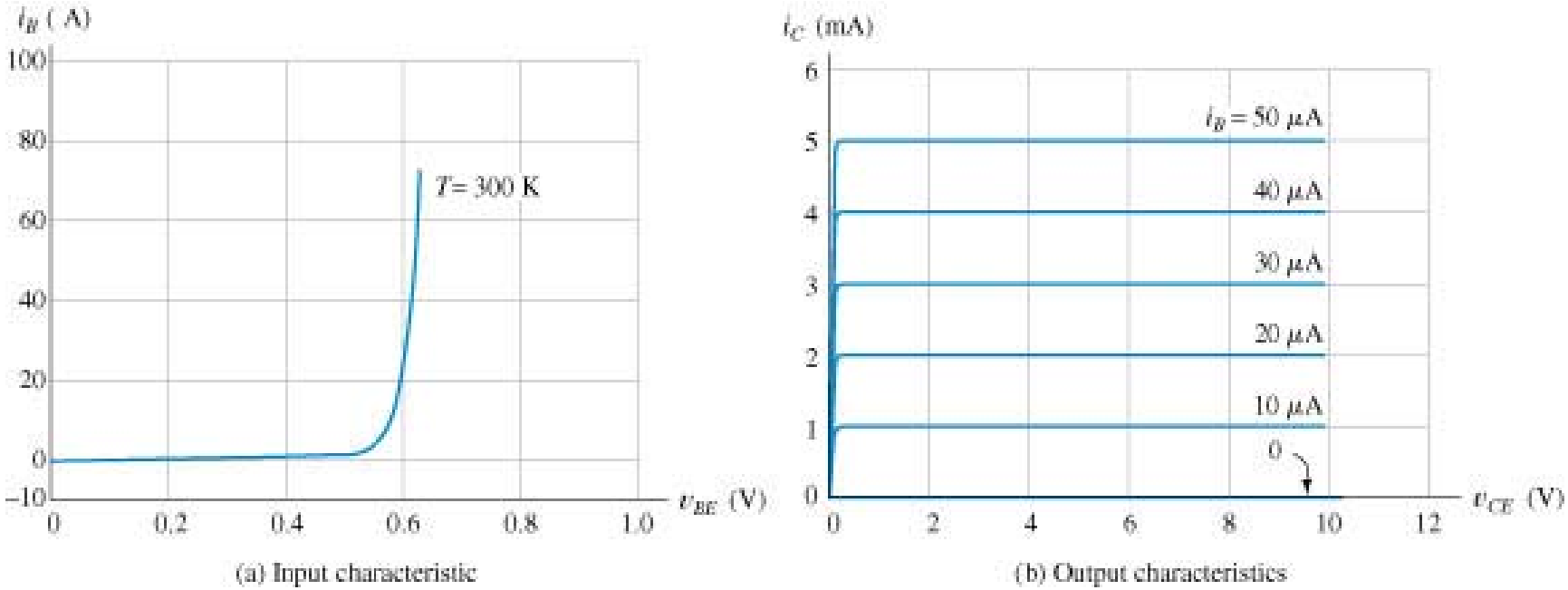


Figure 4.4 Common-emitter characteristics of a typical *npn* BJT.

Secondary Effects

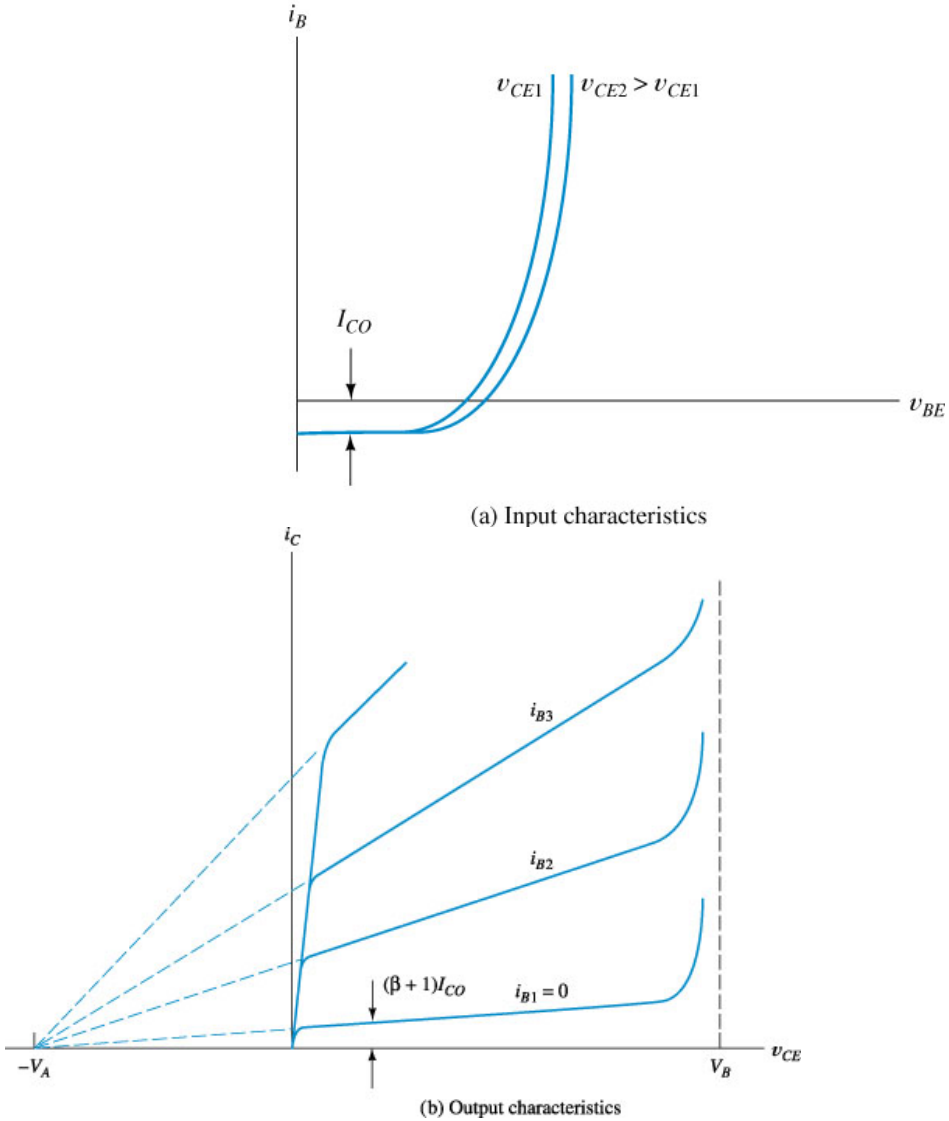


Figure 4.5 Common-emitter characteristics displaying exaggerated secondary effects.

Base - Width Modulation

Base-width modulation: the dependence of the base width from v_{CE}.
Base-width modulation affects i_B and i_C.

V_A – Early voltage

Collector Breakdown

Avalanche breakdown in the depletion region of the collector-base junction

Punch-through

Leakage Current

I_{CO} – **reverse leakage current.** Flows from collector to the base.

4.2 Load - Line Analysis of a Common - Emitter Amplifier

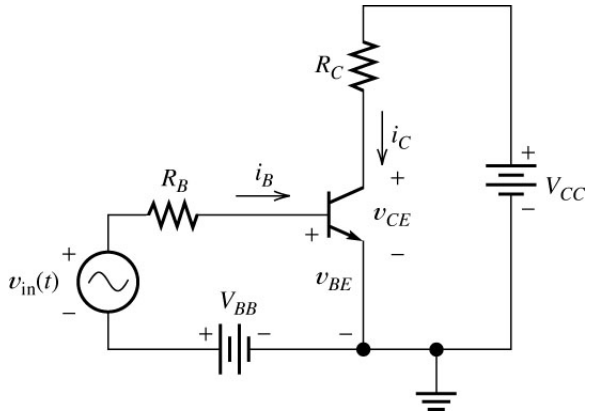


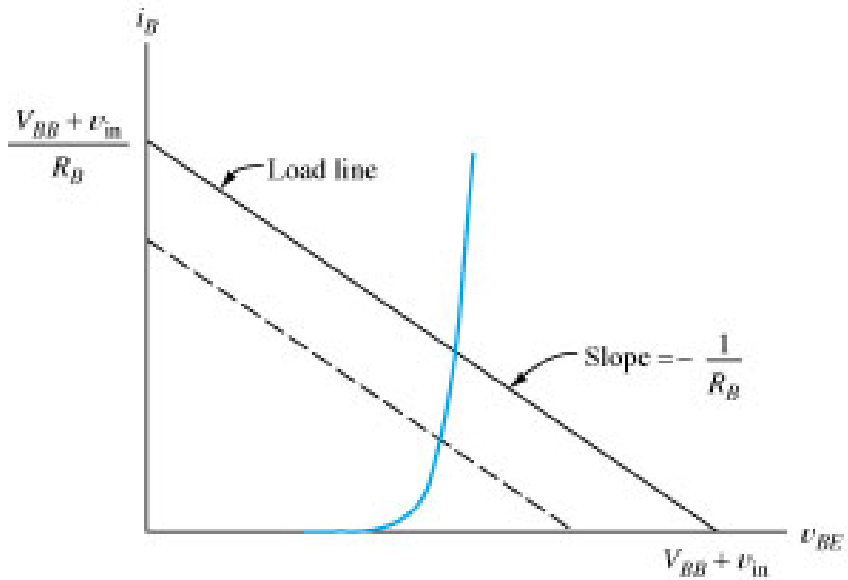
Figure 4.10 Common-emitter amplifier.

Analysis of the Input Current

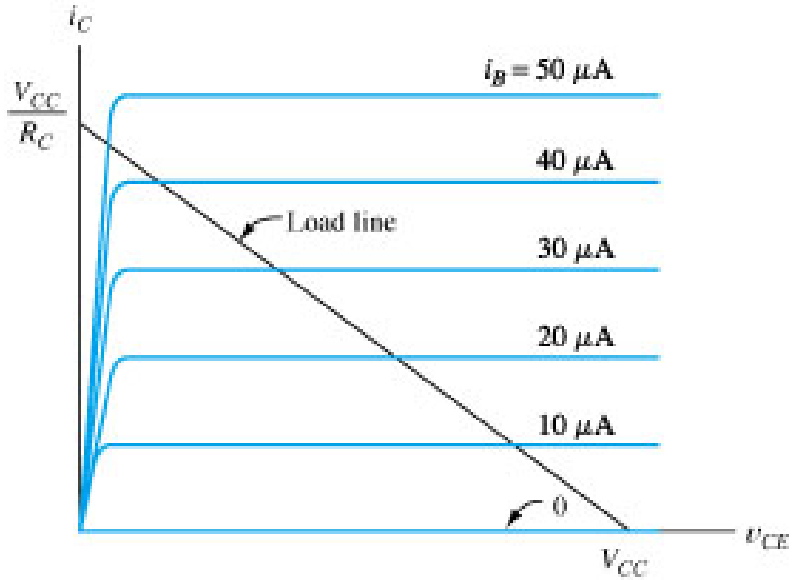
$$V_{BB} + v_{in}(t) = R_B i_B(t) + v_{BE}(t) \qquad (4.13)$$

Analysis of the Output Circuit

$$V_{CC} = R_C i_C + v_{CE} \qquad (4.14)$$



(a) Input (load line shifts to dashed line for a smaller value of v_{in})



(b) Output

Figure 4.11 Load-line analysis of the amplifier of Figure 4.10.

Example 4.2 Graphical Determination of Q-point and Peak Signal Swings

Suppose that the current of Figure 4.10 has V_{CC}=10 V, V_{BB}=1.6 V, R_B=40 kΩ and R_C=2 kΩ. The input signal is a 0.4 V peak, 1 kHz sinusoid given by $v_{in}(t)$=0.4sin(2000πt). The common-emitter characteristics for the transistor are shown in Figure 4.12a and b. Find the maximum, minimum and *Q*-point values for $v_{CE.}$

Solution

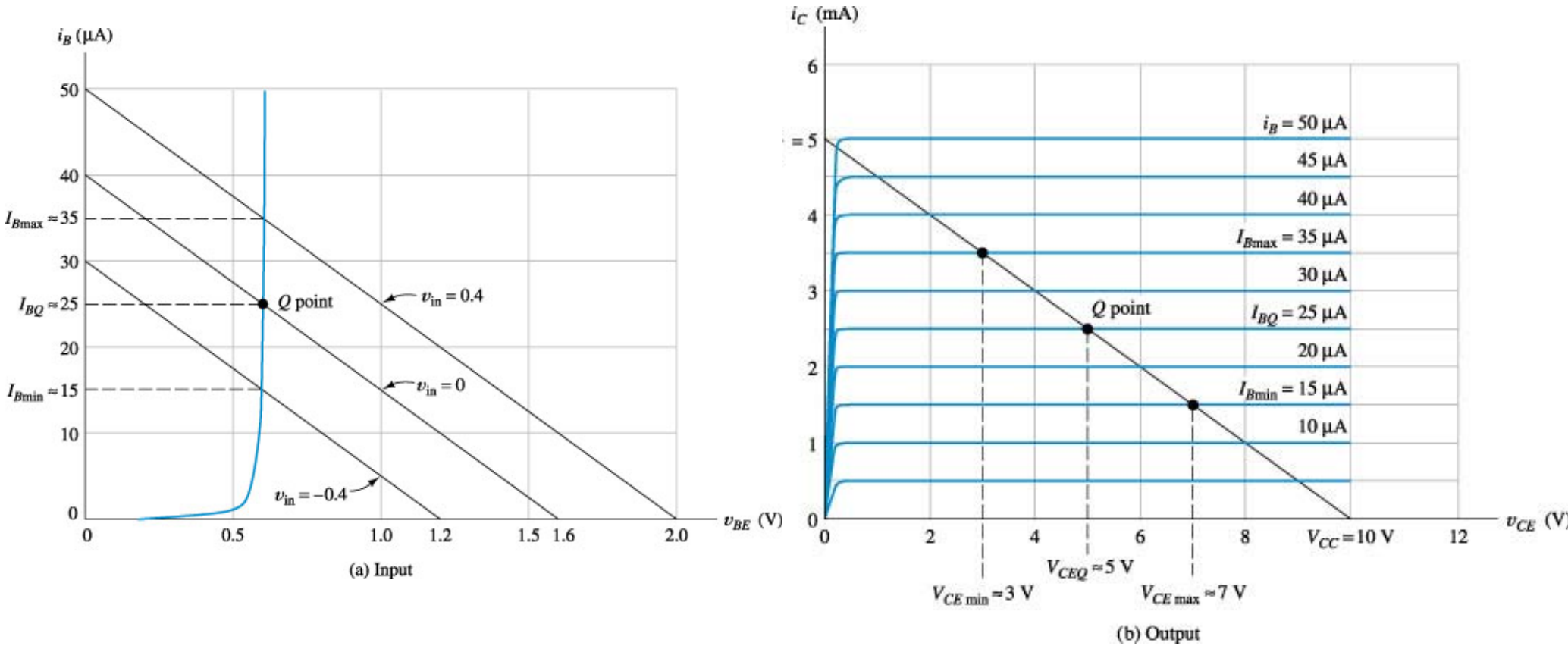


Figure 4.12 Load-line analysis for Example 4.2.

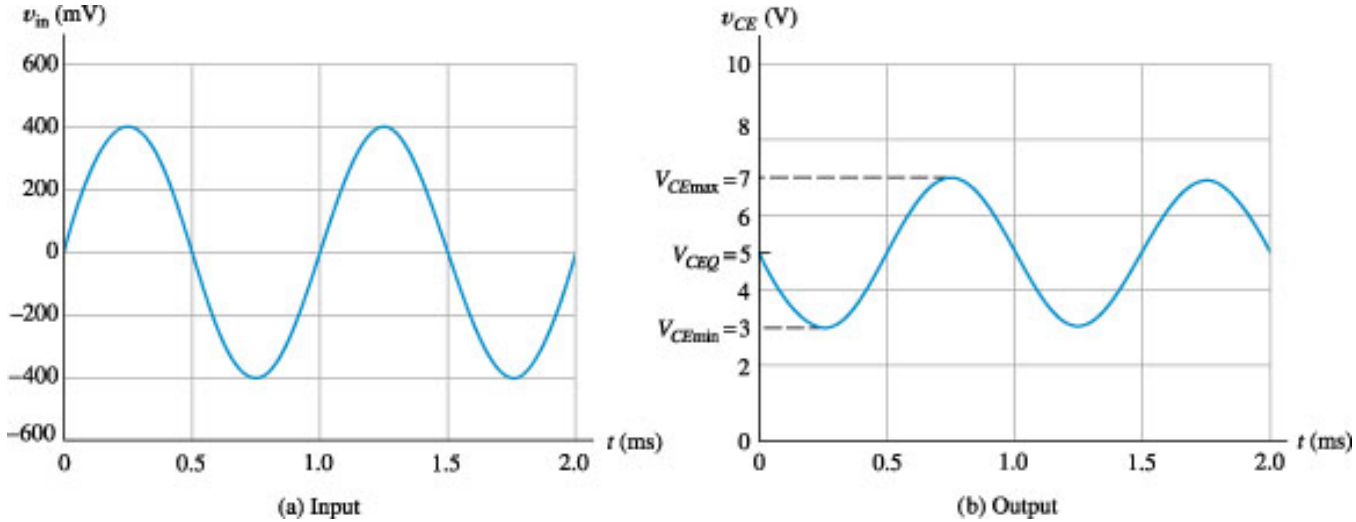


Figure 4.13 Voltage waveforms for the amplifier of Figure 4.10. See Example 4.2.

Gain in Example 4.2:

Amplitude at the input: 0.4V

Amplitude at the output

$$7 - 5 = 2\text{V}$$

$$A_v = \frac{2}{0.4} = 5$$

Distortion

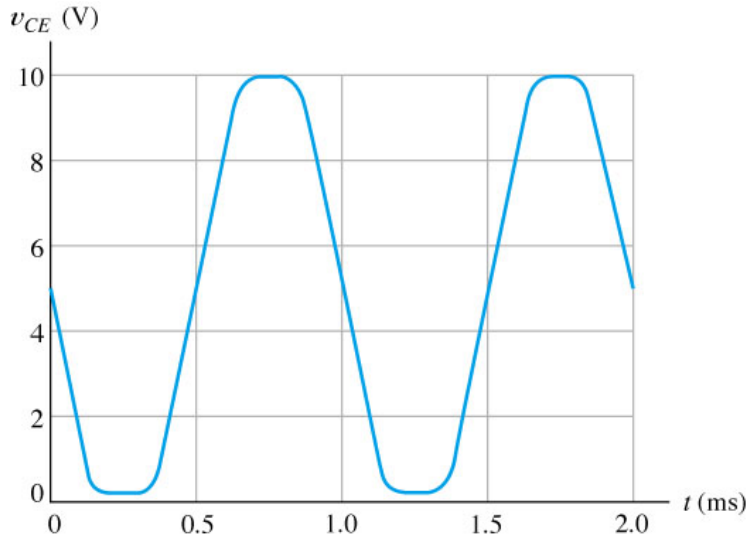


Figure 4.14 Output of the amplifier of Example 4.2 for $v_{in}(t) = 1.2 \sin(2000\pi t)$ showing gross distortion.

Cutoff: $v_{BE} < 0.6\text{V}$ and $i_B \approx 0$

Saturation region: i_B is large and i_C is not proportional to it.

When transistor enters in cutoff or in saturation, clipping of the output signal occurs.

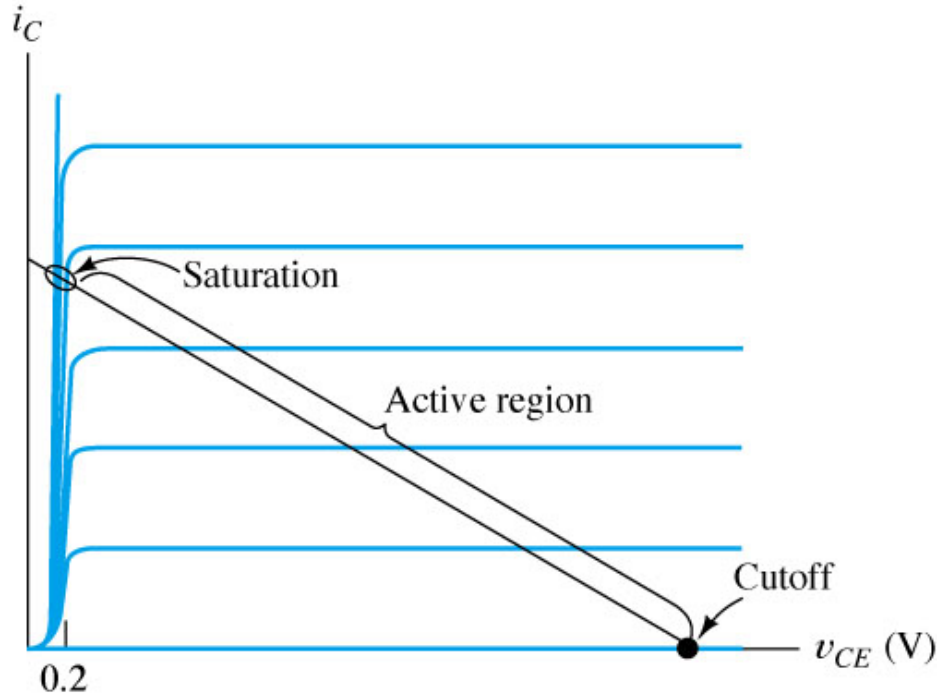


Figure 4.15 Amplification occurs in the active region. Clipping occurs when the instantaneous operating point enters saturation or cutoff. In saturation, $v_{CE} < 0.2$ V.

4.3 The *pnp* Bipolar Junction Transistor

***pnp* transistor**: thin n type semiconductor layer between two p type semiconductor layers

Basic charge carriers: holes

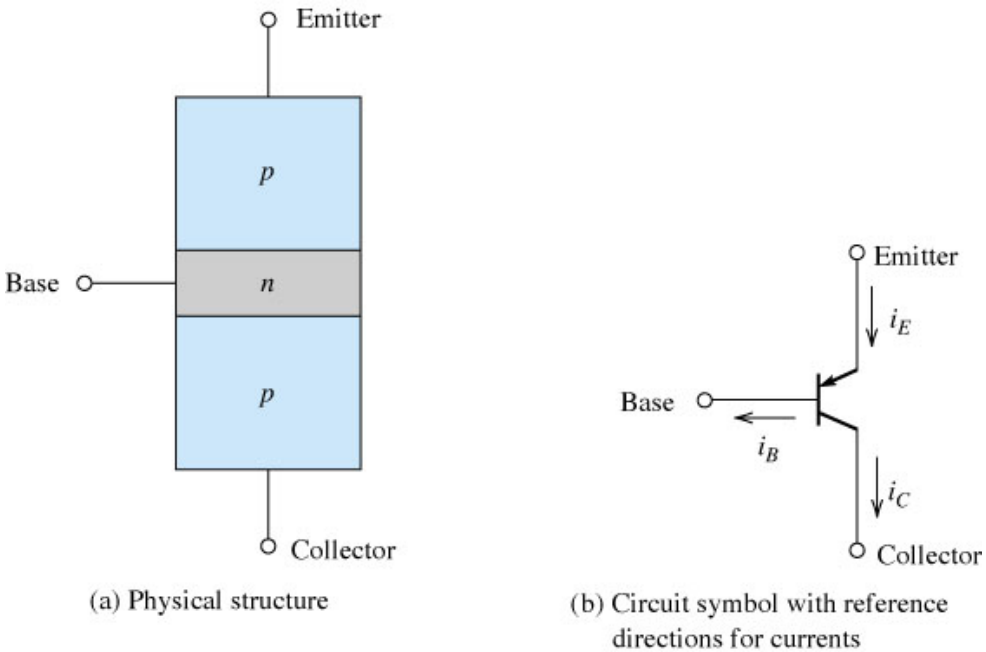


Figure 4.16 The *pnp* BJT.

All relationships between the currents and voltages in a pnp BJT are the same as in npn BJT. There are two basic differences:

- The currents flow in opposite directions;
- The voltages have opposite polarities.

$$i_C = \alpha i_E \tag{4.15}$$

$$i_B = (1-\alpha) i_E \tag{4.16}$$

$$i_C = \beta i_B \tag{4.17}$$

$$i_E = i_C + i_B \tag{4.18}$$

$$i_E = I_{ES}\left[exp\left(\frac{-v_{BE}}{V_T}\right) - 1\right] \tag{4.19}$$

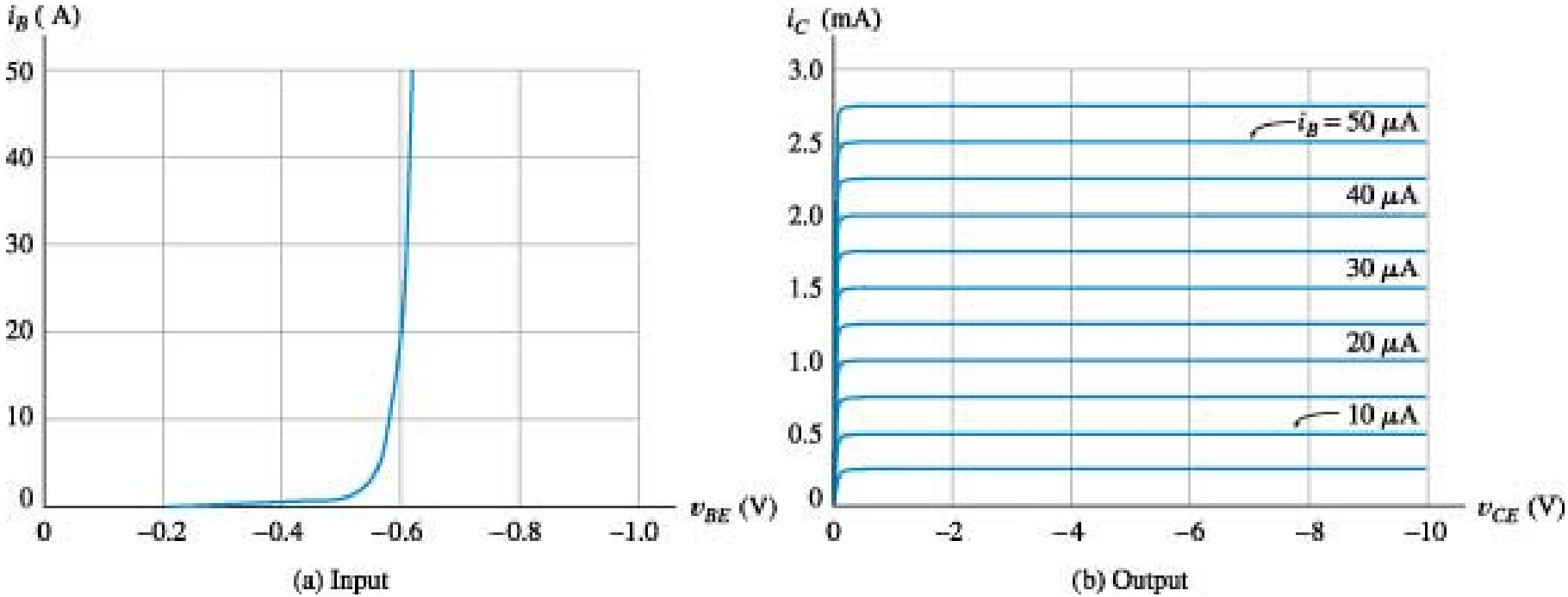


Figure 4.17 Common-emitter characteristics for a *pnp* BJT. Pay attention that the voltages are negative.

4.4 Large - Signal DC Circuit Models

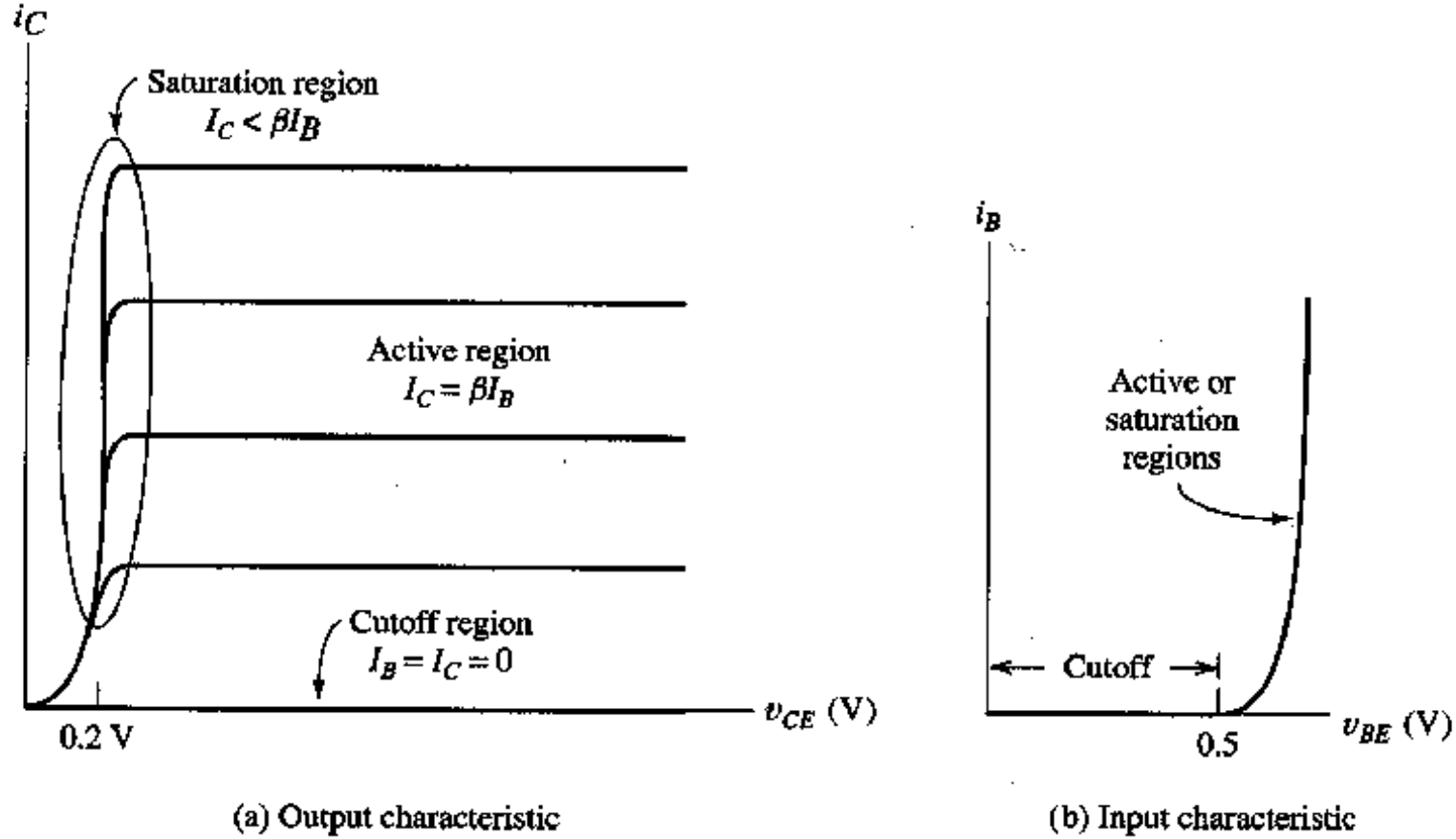


Figure 4.20 Regions of operation on the characteristics of an *npn* BJT.

Active region: $I_B > 0$; $V_{CE} > 0.2\text{V}$
Saturation region: $I_B > 0$; $\beta I_B > I_C > 0$
Cutoff region: $V_{BE} < 0.5\text{V}$; $V_{BC} < 0.5\text{V}$;

Active - Region Model

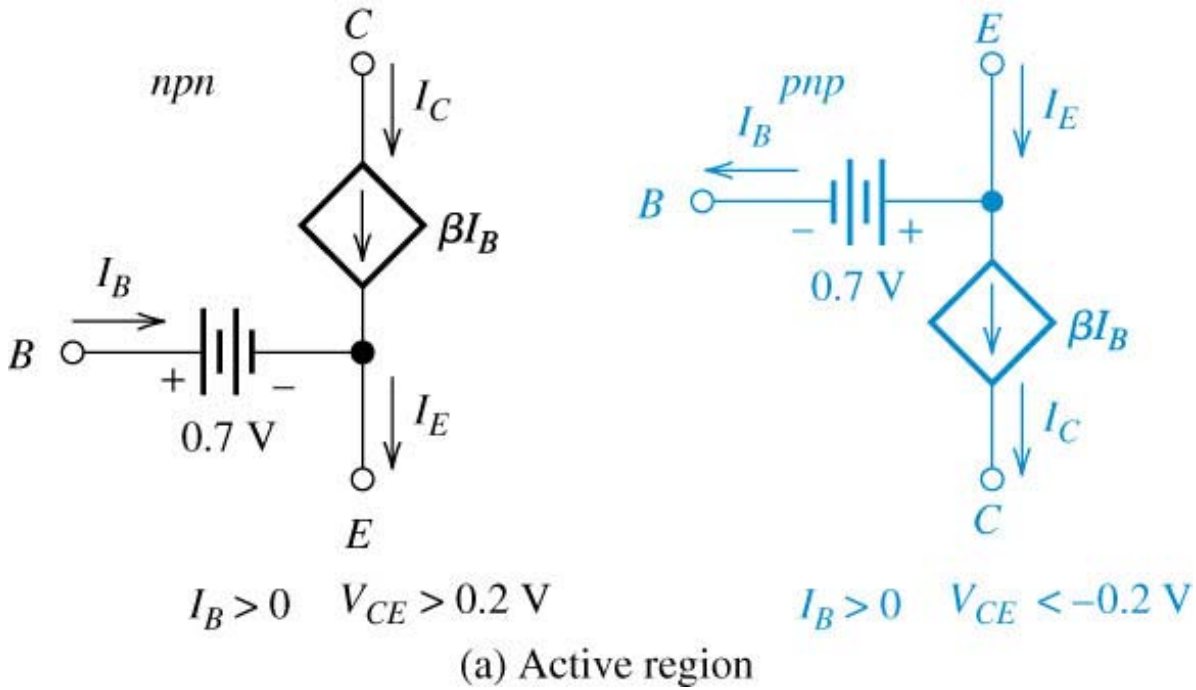
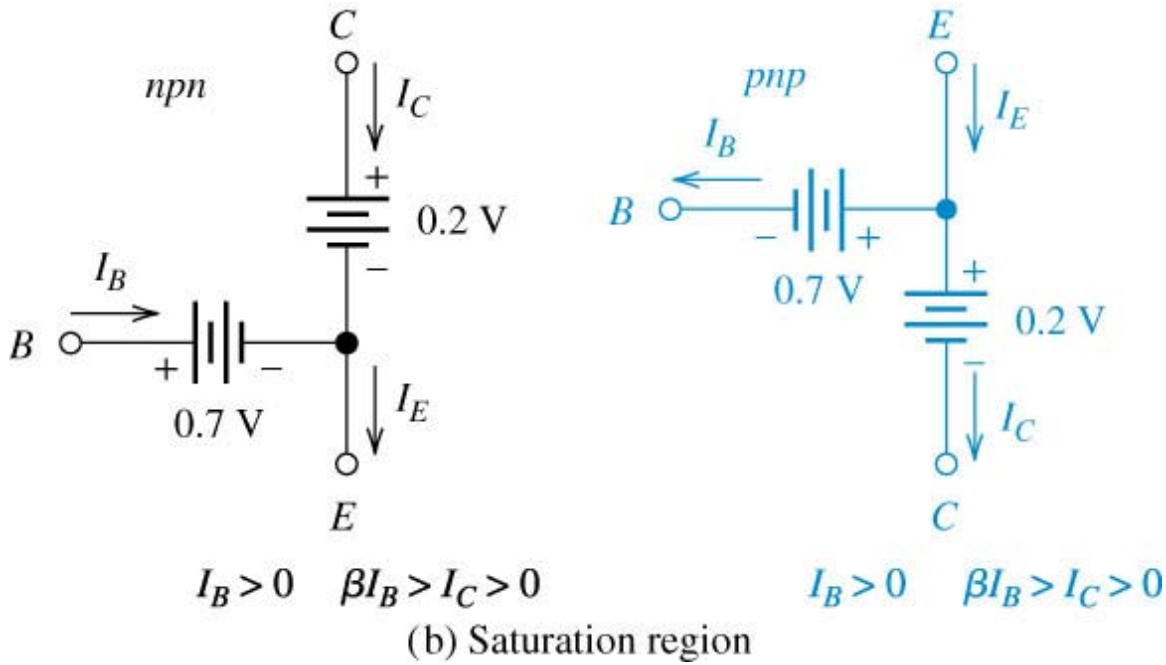


Figure 4.19a BJT large-signal models. (*Note:* Values shown are appropriate for typical small-signal silicon devices at a temperature of 300K.)

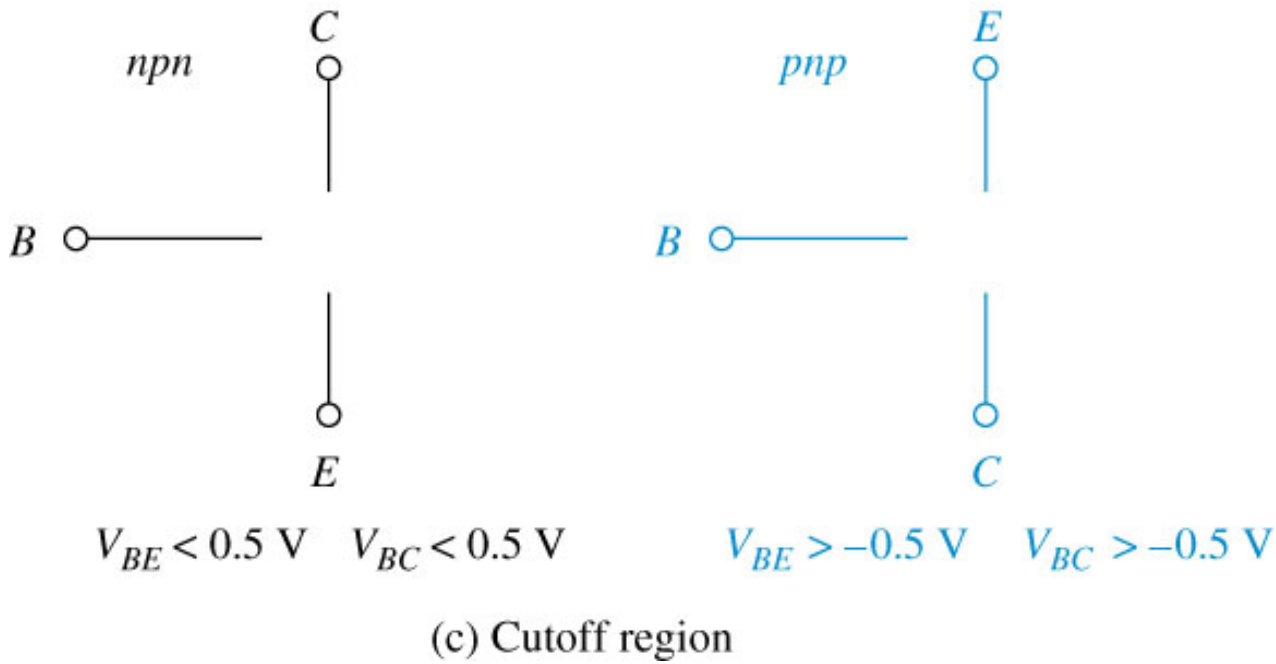
Saturation - Region Model



(b) Saturation region

Figure 4.19b BJT large-signal models. (*Note:* Values shown are appropriate for typical small-signal silicon devices at a temperature of 300K.)

Cutoff - Region Model



(c) Cutoff region

Figure 4.19c BJT large-signal models. (*Note:* Values shown are appropriate for typical small-signal silicon devices at a temperature of 300K.)

Example 4.3 Determination of BJT Operation Region

A given transistor has β =100. Determine the region of operation if (a) I_B = 50μA and I_C = 3mA; (b) I_B = 50μA and V_{CE} = 5V; (c) V_{BE} = -2V and V_{CE} = -1V.

Solution:

(a) I_B = 50μA > 0 – active or saturation region;
$\beta I_B = 100 \times 50 \times 10^{-6} = 5\text{mA} > I_C$ – saturation region.

(b) I_B = 50μA > 0 – active or saturation region;
V_{CE} = 5V > 0.2V – active region.

(c) V_{BE} = -2V < 0.5V – most probably cutoff;
V_{CE} = -1V < 0.5V – this confirms cutoff region.

4.5 Large - Signal DC Analysis of BJT Circuits

Step 1: Assume an operation region for the BJT and replace it by the corresponding large signal equivalent circuit.

Step 2: Solve the circuit to find I_C, I_B, and V_{CE}.

Step 3: Check to see if the values found in Step 2 are consistent with the assumed operating state. If so the solution is complete; otherwise return to Step 1.

Example 4.4 The Fixed - Base Bias Circuit

The DC bias circuit shown in Figure 4.21a has R_B=200 kΩ, R_C=1 kΩ and V_{CC}=15 V. The transistor has β = 100. Solve for I_C and V_{CE}.

Solution:

First assumption: *Cutoff*. The equivalent circuit is in Figure 4.21(b).

$I_B = 0$ – thus the voltage drop across R_B is zero.

Thus $V_{BE} = V_{CC} = 15\text{V} > 0.5\text{V}$.

The assumption is not valid.

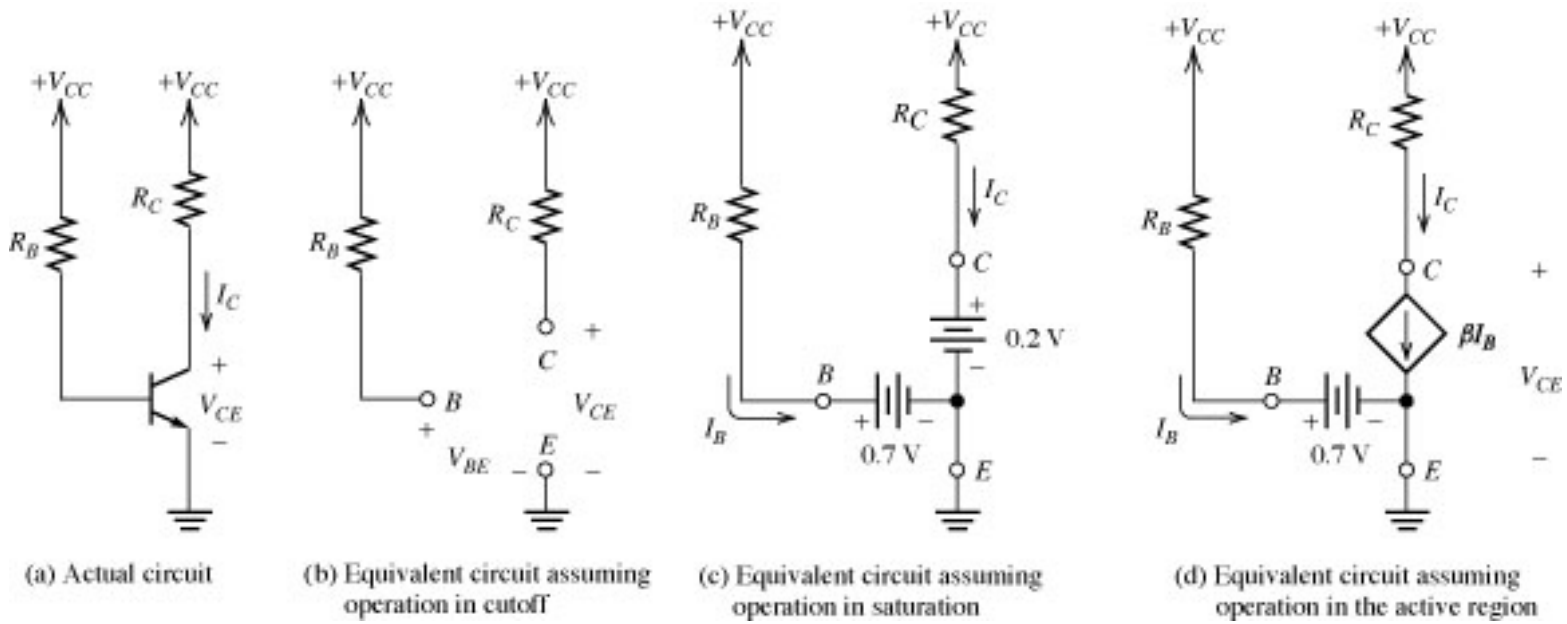


Figure 4.21 Bias circuit of Examples 4.4 and 4.5.

Second assumption: *Saturation*. The equivalent circuit is in Figure 4.21c.

$$I_C = \frac{V_{CC} - 0.2}{R_C} = \frac{15 - 0.2}{1 \times 10^3} = 14.8\text{mA}$$

$$I_B = \frac{V_{CC} - 0.7}{R_B} = \frac{15 - 0.7}{200 \times 10^3} = 71.5\,\mu\text{A}$$

$$\beta I_B = 100 \times 71.5 \times 10^{-6} = 7.15\text{mA} < I_C$$

The assumption is not valid.

Third assumption: *Active region*. The equivalent circuit is in Figure 4.21d.

$$I_B = \frac{V_{CC} - 0.7}{R_B} = \frac{15 - 0.7}{200 \times 10^3} = 71.5\,\mu\text{A}$$

$$I_C = \beta I_B = 7.15\text{mA}$$

$$V_{CE} = V_{CC} - R_C I_C = 15 - 7.15 \times 10^{-3} \times 1 \times 10^3 = 7.85\text{V}$$

$I_B > 0$; $V_{CE} > 0.2\text{V}$. The conditions are met.

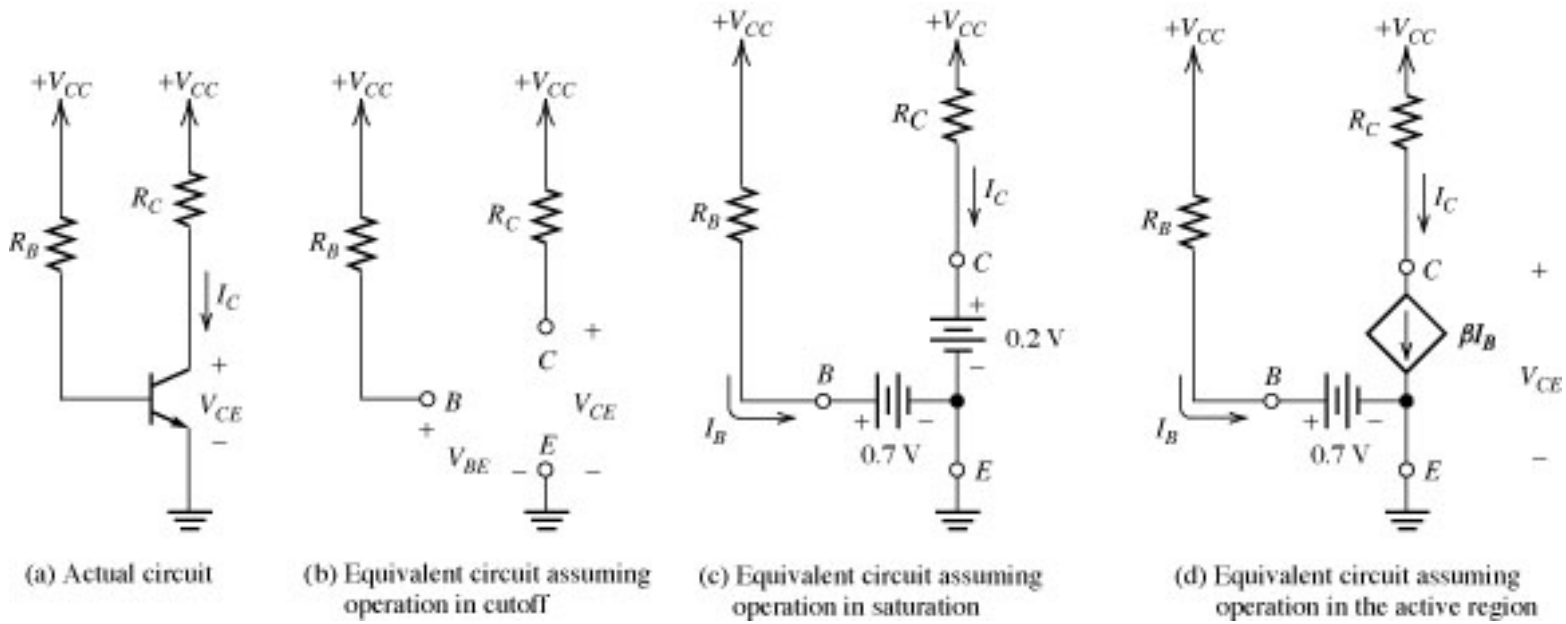


Figure 4.21 Bias circuit of Examples 4.4 and 4.5.

Example 4.5 The Fixed - Base Bias Circuit with Higher Beta

Repeat example 4.4 with β=300.

Solution: First, we assume that the circuit operating in the active region.

$$I_B = \frac{V_{CC} - 0.7}{R_B} = 71.5\ \mu A$$

$$I_C = \beta I_B = 21.45\ mA$$

$$V_{CE} = V_{CC} - R_C I_C = -6.45\text{V} < 0.2\text{V}$$

One of the requirements for the active region V_{CE}>0.2 V is not met.

Next we assume that the transistor is in saturation.

$$I_C = \frac{V_{CC} - 0.2}{R_C} = 14.8\ mA$$

$$I_B = \frac{V_{CC} - 0.7}{R_B} = 71.5\ \mu A$$

$$\beta I_B = 300 \times 71.5 \times 10^{-6} = 21.45\text{mA} > 14.8\text{mA}$$

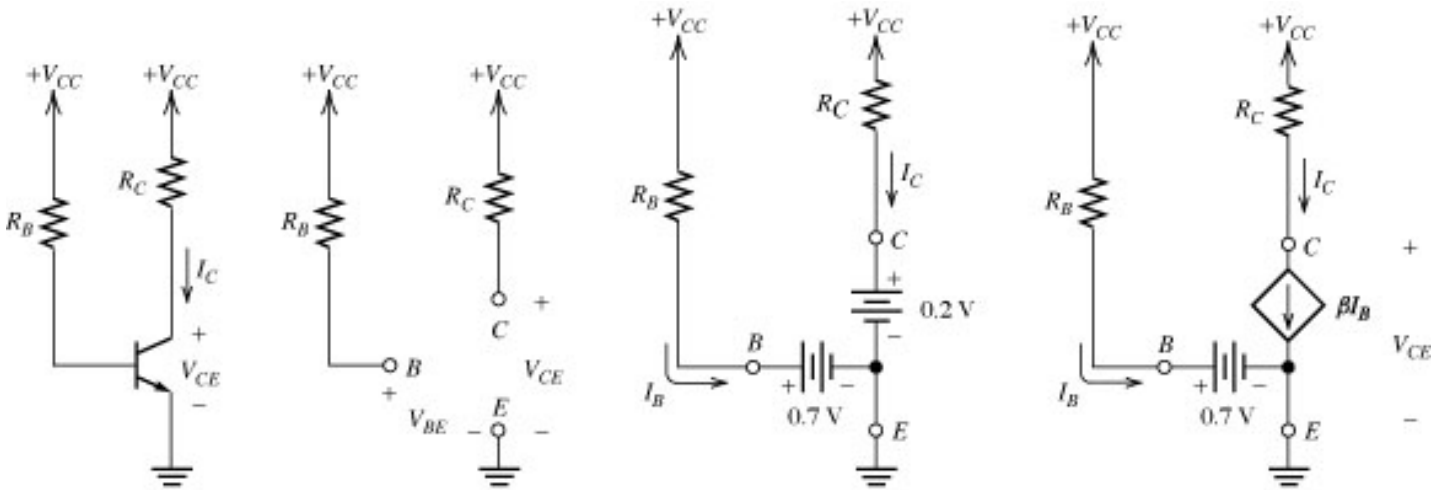
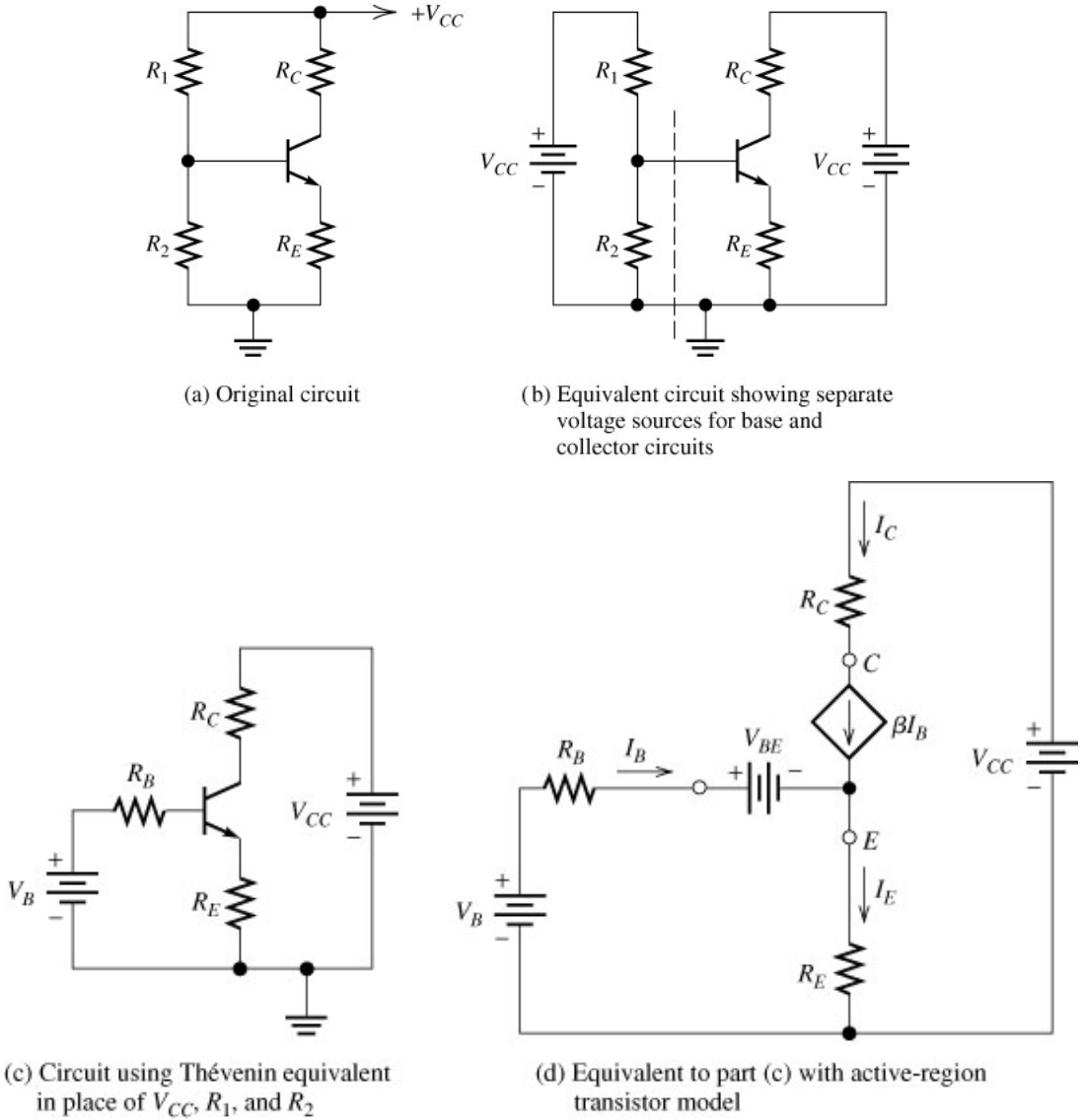


Figure 4.21 Bias circuit of Examples 4.4 and 4.5.

Analysis for the Four - Resistor Bias Circuit



(a) Original circuit

(b) Equivalent circuit showing separate voltage sources for base and collector circuits

(c) Circuit using Thévenin equivalent in place of V_{CC}, R_1, and R_2

(d) Equivalent to part (c) with active-region transistor model

Figure 4.28 Four-resistor bias circuit.

$$R_B = \frac{1}{1/R_1 + 1/R_2} = R_1 \,||\, R_2 \qquad (4.21)$$

$$V_B = \frac{R_2}{R_1 + R_2} V_{CC} \qquad (4.22)$$

$$V_B = R_B I_B + V_{BE} + R_E I_E \qquad (4.23)$$

$$I_E = (\beta + 1) I_B$$

$$I_B = \frac{V_B - V_{BE}}{R_B + (\beta + 1) R_E} \qquad (4.24)$$

$$V_{CE} = V_{CC} - R_C I_C - R_E I_E \qquad (4.25)$$

Discrete Bias - Circuit Design

The principal goal of bias circuit design is to achieve nearly identical operating point for the BJTs, even though the BJT parameters may vary significantly from unit to unit.

In the design usually are given the supply voltage V_{CC}, the collector current I_C in the quiescent point and often V_{CE} in the quiescent point.

The design steps are:

1. Choice of V_{CE}, if it is not specified. A good choice is

$$V_{CE} = \frac{V_{CC}}{3}$$

2. Determining of the voltage drop V_E across R_E and the voltage $V_{CC} - V_C$, which is across R_C. A good choice is

$$V_E = V_{CC} - V_C = \frac{V_{CC} - V_{CE}}{2}$$

3. $I_B = I_C / \beta$

4. Choice of the current I_2 to be $I_2 = (10..20)I_B$.

5. Since $I_E = (\beta+1)I_B \approx I_C$

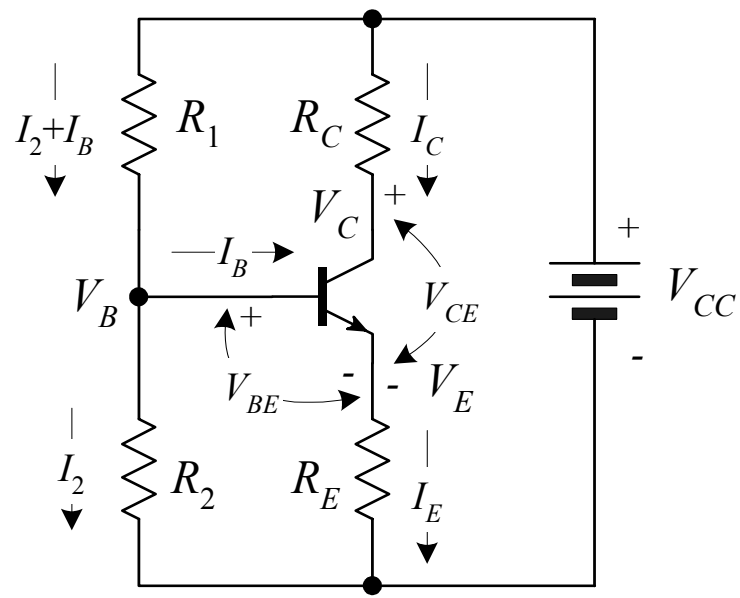
$$R_E = V_E / I_E \approx V_E / I_C$$

6. $V_B = V_E + V_{BE} = V_E + 0.7$

7. $R_2 = V_B / I_2$

$$R_1 = (V_{CC} - V_B)/(I_B + I_2)$$

$$R_C = (V_{CC} - V_C)/I_C$$

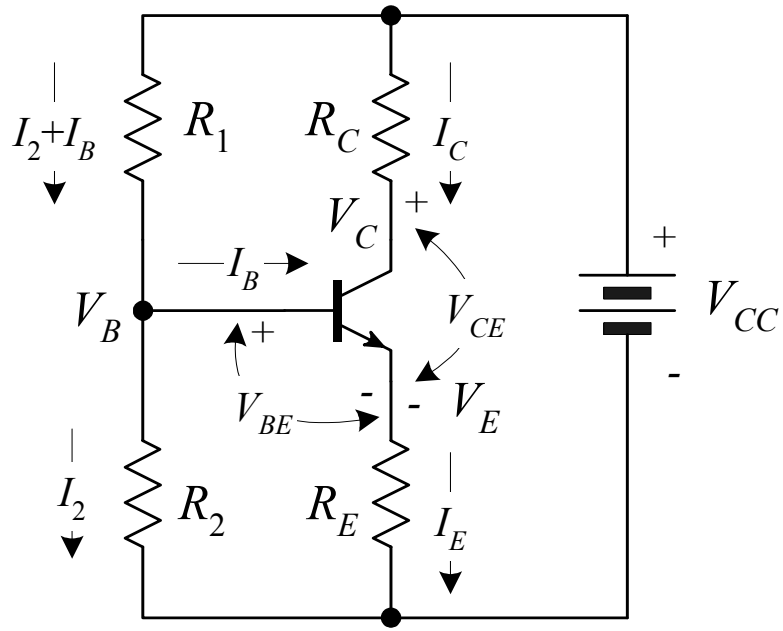


Four-resistor bias circuit.

How the circuit stabilize the quiescent point?

Assume that the emitter current I_C is increased, due to some reason. Then

- Emitter current I_E is increased also, since $I_E \approx I_C$.
- V_E increases since $V_E = I_E R_E$
- I_2 is at least 10 times more than I_B. It is the basic part of the current through R_1. Thus the both currents are stable and depend very weak on the variation of the currents in the BJT.
- The stable currents through R_1 and R_2 define a stable voltage V_B.
- $V_{BE} = V_B - V_E$ and the increasing of V_E decreases V_{BE}.
- Smaller V_{BE} means smaller base current I_B (see the input characteristic in Figure 4.4).
- $I_C = \beta I_B$ and the smaller base current returns the collector current to its initial value.



Four-resistor bias circuit.

Problem D4.39. Four-resistor bias circuit design.

Suppose that $V_{CC} = 20\text{V}$, $R_C = 1\text{k}\Omega$, and a quiescent point of $I_{CQ} = 5\text{mA}$ is desired. The transistor has β ranging from 50 to 150. Design a four resistor bias circuit. Use standard 5%-tolerance resistors.

Solution:

Since R_C is specified we can determine the voltage drop across it and the voltage V_C

$$V_{CC} - V_C = I_{CQ}R_C = 5\times10^{-3}\times1\times10^{3} = 5\text{V}$$

$$V_C = 20 - 5 = 15\text{V}$$

$$V_E = V_{CE} = V_C/2 = 15/2 = 7.5\text{V}$$

$$V_B = V_E + V_{BE} = 7.5 + 0.7 = 8.2\text{V}$$

To determine I_B, we take the smallest value of β. In this way we will determine the largest value of I_B and the largest value of I_2. If β is higher, the condition for I_2 will be also satisfied.

$$I_B = I_C/\beta = 5\times10^{-3}/50 = 100\mu\text{A}$$

$$I_2 = 10I_B = 10\times100\times10^{-6} = 1\text{mA}$$

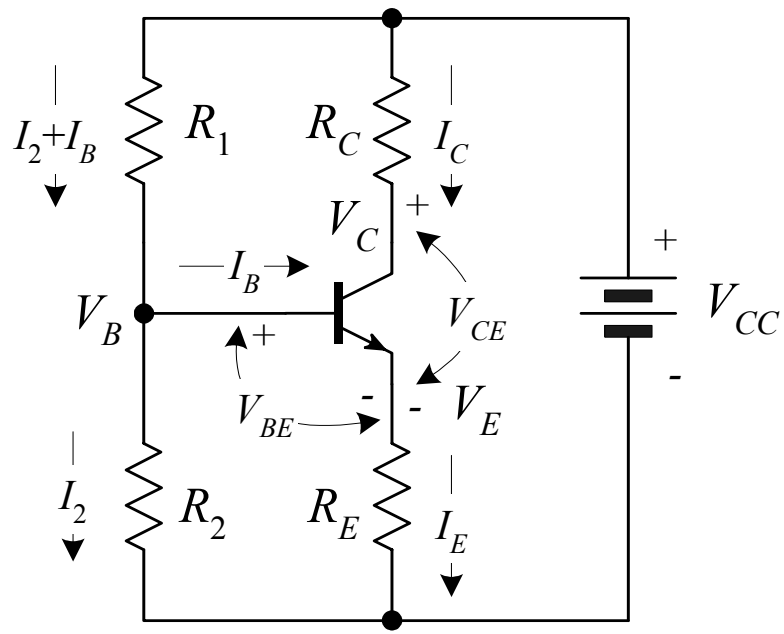
$$R_E = V_E/I_E = 7.5/\left(5\times10^{-3}\right) = 1500\Omega$$

$$R_2 = V_B/I_2 = 8.2/\left(1\times10^{-3}\right) = 8.2\text{k}\Omega$$

$$R_1 = \left(V_{CC} - V_B\right)/\left(I_2 + I_B\right)$$

$$= \left(20 - 8.2\right)/\left(1\times10^{-3} + 100\times10^{-6}\right) = 10.7\text{k}\Omega$$

The 5%-tolerance standard values for the resistors are $R_E = 1.5\text{k}\Omega$, $R_1 = 8.2\text{k}\Omega$, $R_2 = 11\text{k}\Omega$.



Four-resistor bias circuit.

4.6 Small - Signal Equivalent Circuits

Small - Signal Current - Voltage Relationship

$$i_B = (1-\alpha) I_{ES}\left[exp\left(\frac{v_{BE}}{V_T}\right) - 1 \right] \tag{4.28}$$

$$I_{BQ} + i_b(t) = (1-\alpha) I_{ES}\, exp\left(\frac{V_{BEQ} + v_{be}(t)}{V_T}\right) \tag{4.29}$$

$$I_{BQ} + i_b(t) = (1-\alpha) I_{ES}\, exp\left(\frac{V_{BEQ}}{V_T}\right) exp\left(\frac{v_{be}(t)}{V_T}\right) \tag{4.30}$$

$$I_{BQ} = (1-\alpha) I_{ES}\, exp\left(\frac{V_{BEQ}}{V_T}\right) \tag{4.31}$$

$$I_{BQ} + i_b(t) = I_{BQ}\, exp\left(\frac{v_{be}(t)}{V_T}\right) \tag{4.32}$$

$$\exp(x) \cong 1 + x \tag{4.33}$$

$$I_{BQ} + i_b(t) \cong I_{BQ}\left(1 + \frac{v_{be}(t)}{V_T}\right) \tag{4.34}$$

$$i_b(t) = \frac{v_{be}(t)}{r_\pi} \tag{4.35}$$

$$r_\pi = \frac{V_T}{I_{BQ}} \tag{4.36}$$

$$r_\pi = \frac{\beta V_T}{I_{CQ}} \tag{4.37}$$

$$i_C(t) = \beta\, i_B(t) \tag{4.38}$$

$$I_{CQ} + i_c(t) = \beta\, I_{BQ} + \beta\, i_b(t) \tag{4.39}$$

$$i_c(t) = \beta\, i_b(t) \tag{4.40}$$

Small - Signal Equivalent Circuit for the BJT

$$i_c(t) = \frac{\beta}{r_\pi} v_{be}(t)$$

$$g_m = \frac{\beta}{r_\pi} \qquad (4.41)$$

$$g_m = \frac{I_{CQ}}{V_T} \qquad (4.42)$$

$$v_{be}(t) = r_\pi i_b(t) \quad \text{and} \quad i_c(t) = g_m v_{be}(t)$$

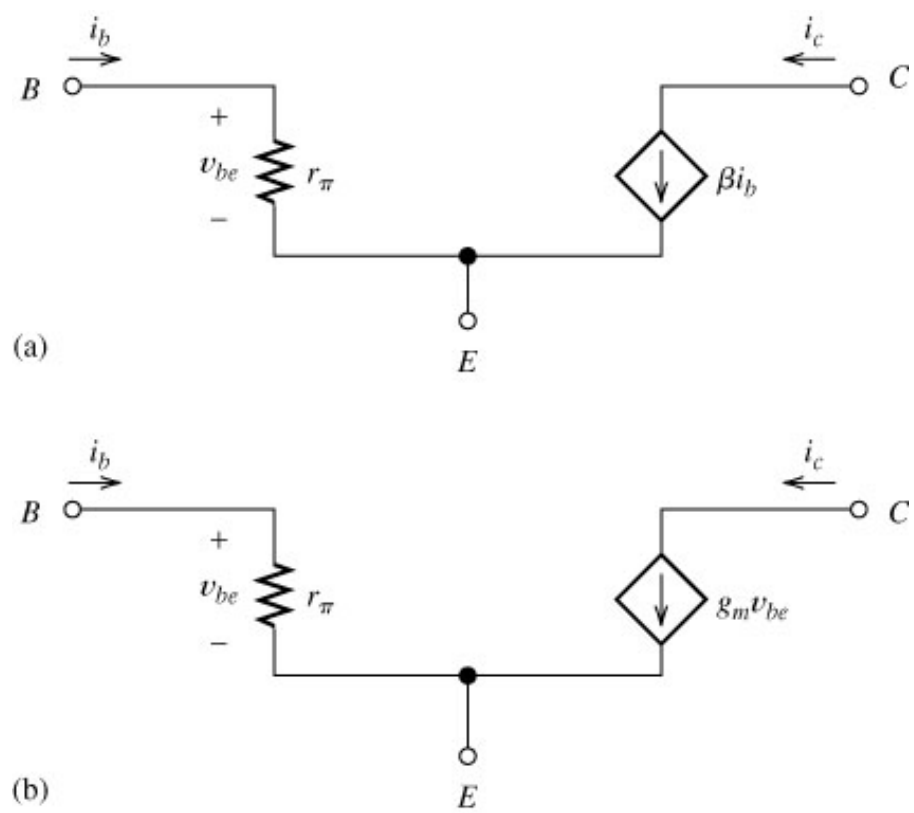


Figure 4.33 Small-signal equivalent circuits for the BJT.

Exercise 4.19 At room temperature, a certain transistor has β=100. Compute the values of g_m and r_π for I_{CQ}=10 mA. Repeat for I_{CQ}=1 mA

Solution:

$$\text{At } I_C = 10\text{mA}: \quad r_\pi = \frac{\beta V_T}{I_{CQ}} = \frac{100 \times 0.026}{10 \times 10^{-3}} = 260\Omega; \quad g_m = \frac{\beta}{r_\pi} = \frac{100}{260} \approx 385\text{mS}$$

$$\text{At } I_C = 1\text{mA}: \quad r_\pi = \frac{\beta V_T}{I_{CQ}} = \frac{100 \times 0.026}{1 \times 10^{-3}} = 2600\Omega; \quad g_m = \frac{\beta}{r_\pi} = \frac{100}{2600} \approx 38.5\text{mS}$$

4.7 The Common - Emitter Amplifier

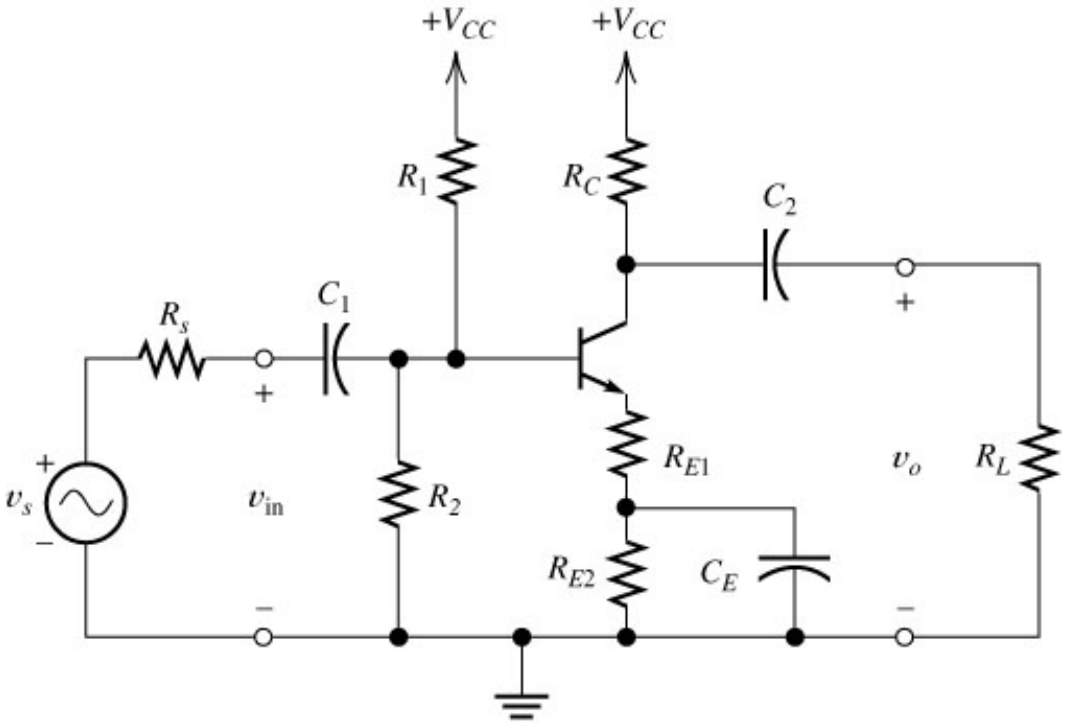


Figure 4.34 Common-emitter amplifier.

R_1, R_2, R_C and R_{E1}+R_{E2} form the four resistor biasing circuit;

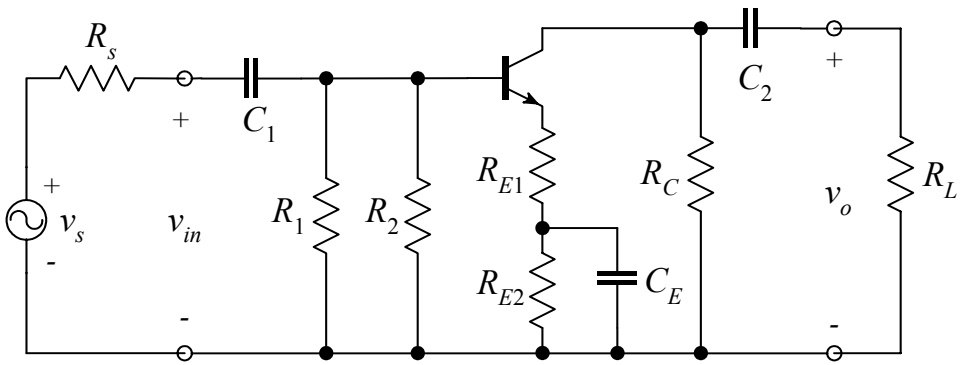
C_1 and C_2 are **coupling capacitors**;

C_E is **bypass capacitor**.

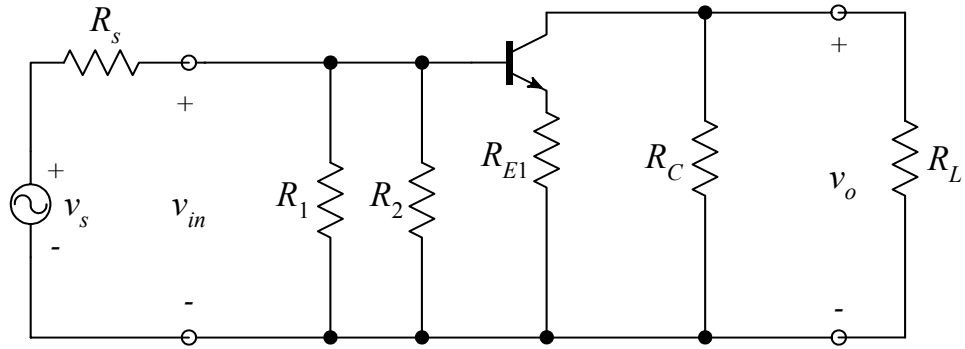
For ac signal the supply voltage is short circuit.

If $R_{E1} = 0$ the input signal is between the base and the emitter (ground); the output signal is between collector and the emitter ($+V_{CC}$, which is ground for ac signal) – **common-emitter** amplifier.

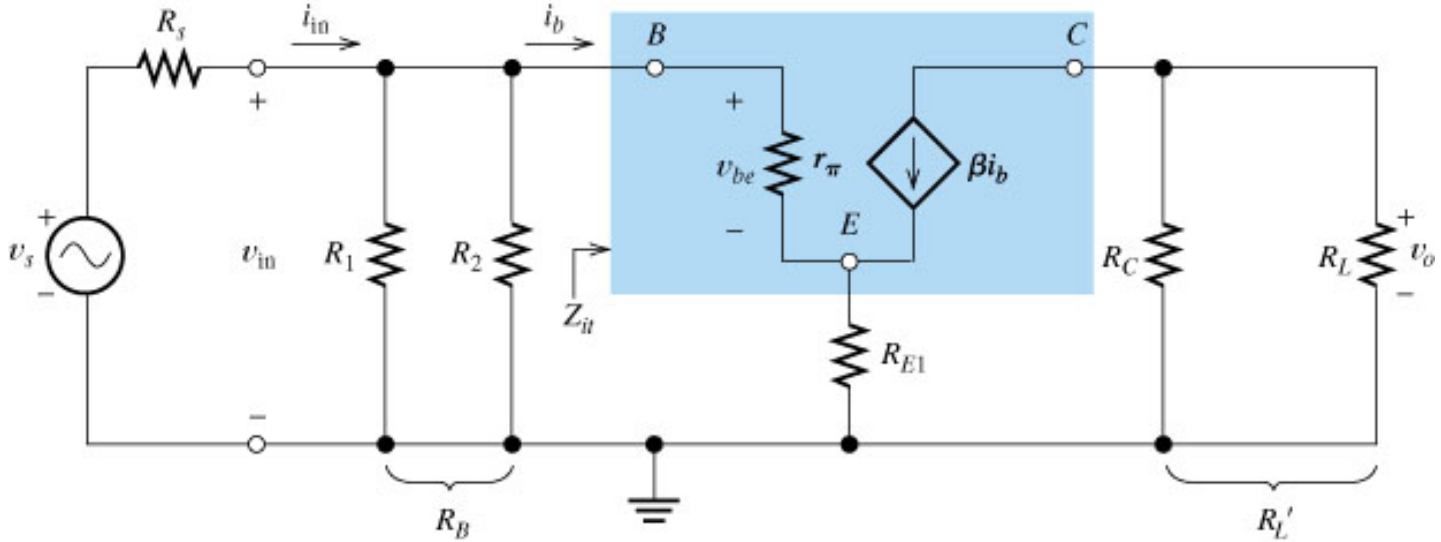
The Small - Signal Equivalent Circuit



The first step in creating the small-signal equivalent circuit: the dc voltage sources are replaced by short circuits



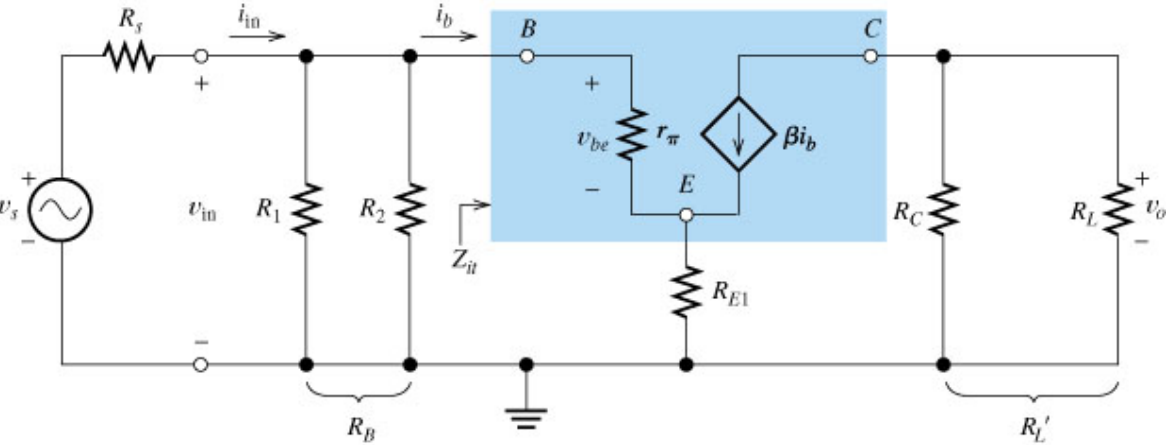
The second step in creating the small-signal equivalent circuit for mid-band region: the coupling capacitors and the bypass capacitors are replaced by short circuits



(b) Small-signal midband equivalent circuit

Figure 4.34 Common-emitter amplifier. (b) Final small-signal mid-band equivalent circuit.

Voltage Gain



(b) Small-signal midband equivalent circuit

Figure 4.34 Common-emitter amplifier.

Simplifications:

$$R_B = R_1 \,||\, R_2 = \frac{1}{1/R_1 + 1/R_2} \qquad (4.43)$$

$$R_L' = R_L \,||\, R_C = \frac{1}{1/R_L + 1/R_C} \qquad (4.44)$$

$$\begin{aligned} v_{in} &= v_{be} + i_e R_{E1} \\ &= r_\pi i_b + R_{E1}(\beta+1) i_b \end{aligned} \qquad (4.45)$$

$$v_o = -R_L' \beta\, i_b \qquad (4.46)$$

$$A_v = \frac{v_o}{v_{in}} = -\frac{\beta R_L'}{r_\pi + (\beta+1)R_{E1}} \qquad (4.47)$$

If $R_{E1} = 0$: $\quad A_v = -\dfrac{\beta R_L'}{r_\pi}$

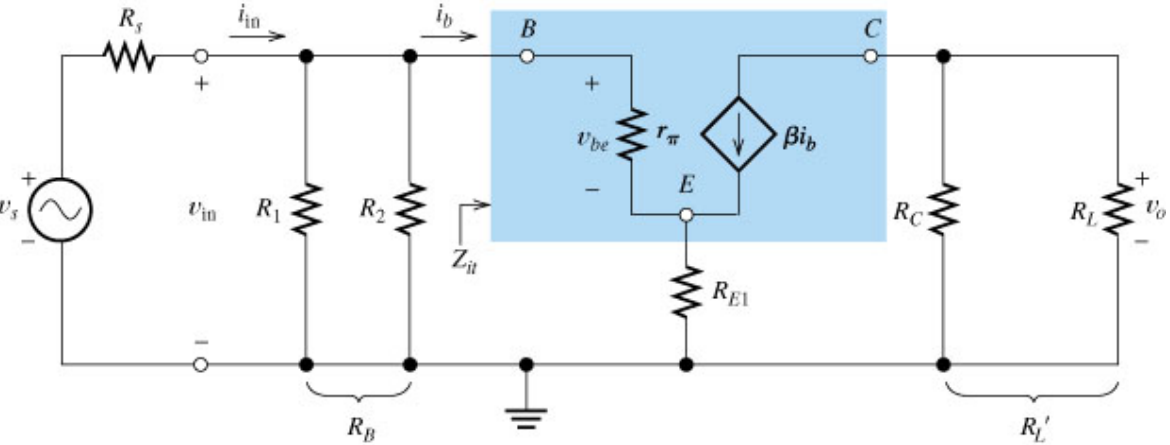
If $(\beta+1)R_{E1} >> r_\pi$: $\quad A_v \cong -\dfrac{\beta R_L'}{(\beta+1)R_{E1}} \approx -\dfrac{R_L'}{R_{E1}}$

and the voltage gain doesn't depend on BJT parameters.

Open circuit voltage gain (when $R_L = \infty$)

$$A_{vo} = \frac{v_o}{v_{in}} = -\frac{\beta R_C}{r_\pi + (\beta+1)R_{E1}} \qquad (4.48)$$

Input Impedance



(b) Small-signal midband equivalent circuit

Figure 4.34 Common-emitter amplifier.

$$Z_{it} = \frac{v_{in}}{i_b} = r_\pi + (\beta + 1)R_{E1} \qquad (4.49)$$

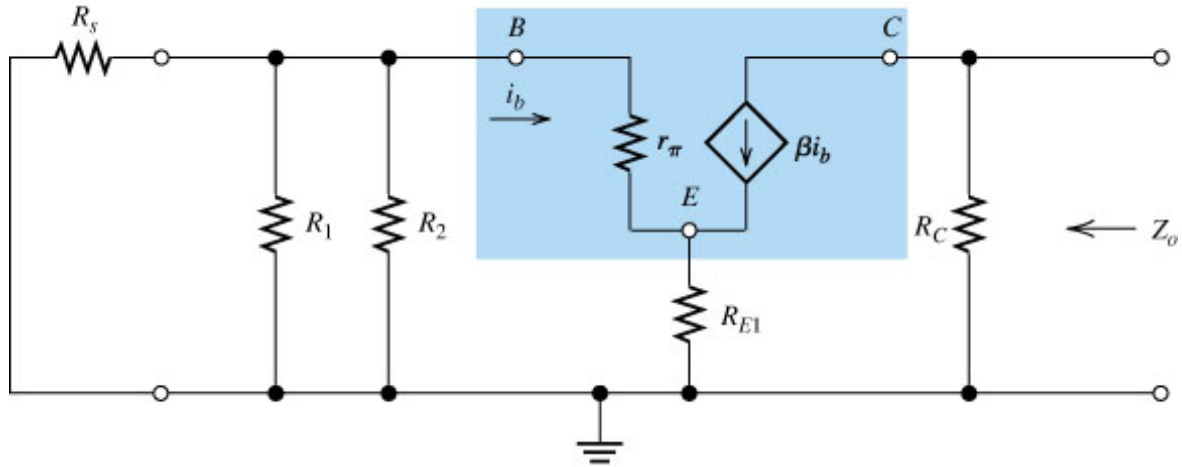
$$Z_{in} = \frac{v_{in}}{i_{in}} = \frac{1}{1/R_B + 1/Z_{it}} \qquad (4.50)$$

Current Gain and Power Gain

$$A_i = \frac{i_o}{i_{in}} = A_v \frac{Z_{in}}{R_L} \qquad (4.51)$$

$$G = A_i A_v \qquad (4.52)$$

Output Impedance



(c) Equivalent circuit used to find Z_o

Figure 4.34 Common-emitter amplifier.

$i_b = 0$ and $\beta i_b = 0$. Thus there is an open circuit between C and E.

$$Z_o = R_C \qquad (4.53)$$

Example 4.9 Calculation of Common - Emitter Amplifier Performance

a) Find A_v, A_{vo}, Z_{in}, A_i, G, and Z_o for the amplifier shown in Figure 4.35.

b) Repeat part (a) if the emitter resistor R_E is split in into R_{E1}=100 Ω and R_{E2}=900 Ω, with bypass capacitor in the parallel with R_{E2}.

β of the BJT is 100 and from dc analysis is found that the quiescent point is I_{CQ} = 4.12mA and V_{CE} = 6.72V.

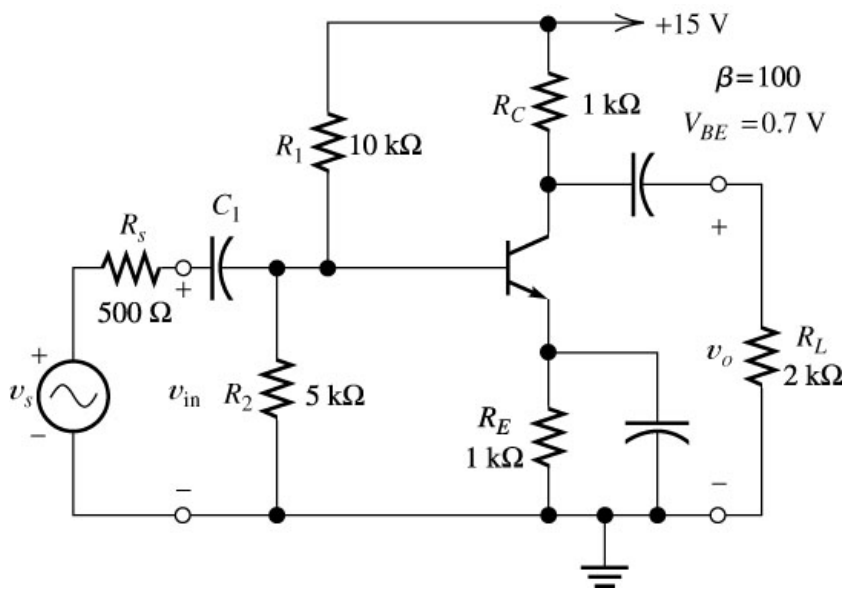


Figure 4.35 Common-emitter amplifier of Example 4.9.

Solution:

$$r_\pi = \frac{\beta V_T}{I_{CQ}} = \frac{100 \times 0.026}{4.12 \times 10^{-3}} = 631\Omega$$

$$R_B = \frac{1}{1/R_1 + 1/R_2} = \frac{1}{1/\left(10 \times 10^3\right) + 1/\left(5 \times 10^3\right)} = 3.33\ k\Omega$$

$$R_L^{'} = \frac{1}{1/R_L + 1/R_C} = \frac{1}{1/\left(2 \times 10^3\right) + 1/\left(1 \times 10^3\right)} = 667\ \Omega$$

a)

$$A_v = \frac{v_o}{v_{in}} = -\frac{\beta R_L^{'}}{r_\pi} = -\frac{100 \times 667}{631} = -106$$

$$A_{vo} = \frac{v_o}{v_{in}} = -\frac{\beta R_C}{r_\pi} = -\frac{100 \times 1 \times 10^3}{631} = -158$$

$$Z_{it} = r_\pi = 631\Omega$$

$$Z_{in} = \frac{v_{in}}{i_{in}} = \frac{1}{1/R_B + 1/Z_{it}}$$

$$= \frac{1}{1/\left(3.33 \times 10^3\right) + 1/631} = 531\,\Omega$$

$$A_i = \frac{i_o}{i_{in}} = A_v \frac{Z_{in}}{R_L} = -106\frac{531}{2 \times 10^3} = -28.1$$

$$G = A_i\, A_v = \left(-28.1\right) \times \left(-106\right) = 2980$$

$$Z_o = R_C = 1\text{k}\Omega$$

b)

$$A_v = \frac{v_o}{v_{in}} = -\frac{\beta R_L^{'}}{r_\pi + \left(\beta + 1\right)R_{E1}}$$

$$= -\frac{100 \times 667}{631 + \left(100 + 1\right) \times 100} = -6.21$$

$$A_{vo} = \frac{v_o}{v_{in}} = -\frac{\beta R_C}{r_\pi + \left(\beta + 1\right)R_{E1}}$$

$$= -\frac{100 \times 1 \times 10^3}{631 + \left(100 + 1\right) \times 100} = -9.31$$

$$Z_{it} = \frac{v_{in}}{i_b} = r_\pi + \left(\beta + 1\right)R_{E1} = 631 + \left(100 + 1\right) \times 100 = 10.7\,k\Omega$$

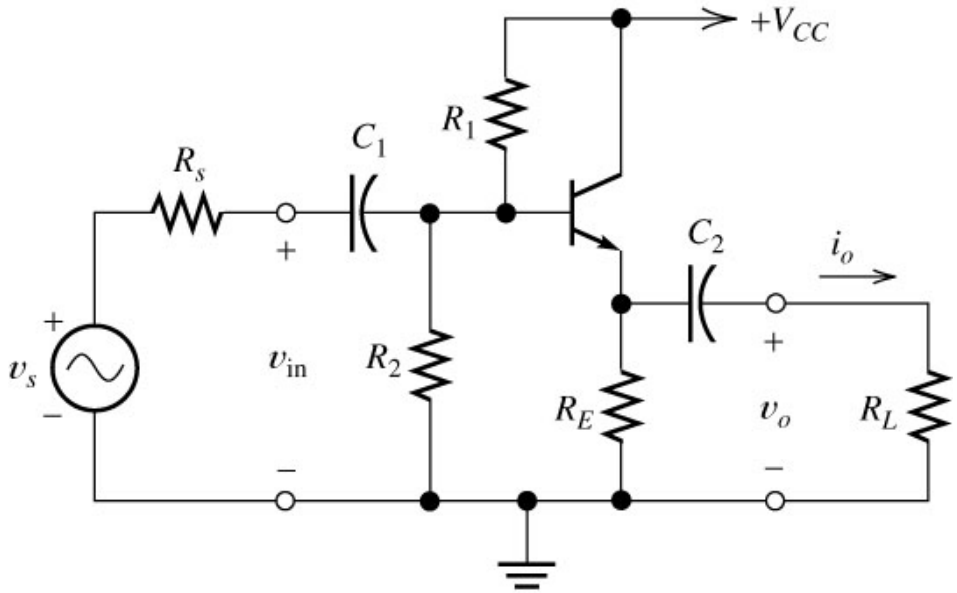
$$Z_{in} = \frac{1}{1/R_B + 1/Z_{it}} = \frac{1}{1/\left(3.33 \times 10^3\right) + 1/\left(10.7 \times 10^3\right)} = 2.54\,k\Omega$$

$$A_i = \frac{i_o}{i_{in}} = A_v \frac{Z_{in}}{R_L} = -6.21\frac{2.54 \times 10^3}{2 \times 10^3} = -7.89$$

$$G = A_i\, A_v = \left(-7.89\right) \times \left(-6.21\right) = 49.0$$

$$Z_o = R_C = 1\text{k}\Omega$$

4.8 The Emitter Follower



(a) Actual circuit

Figure 4.36 Emitter follower.

R_1, R_2, and R_E are from the four resistor biasing circuit.

C_1 and C_2 are **coupling capacitors**.

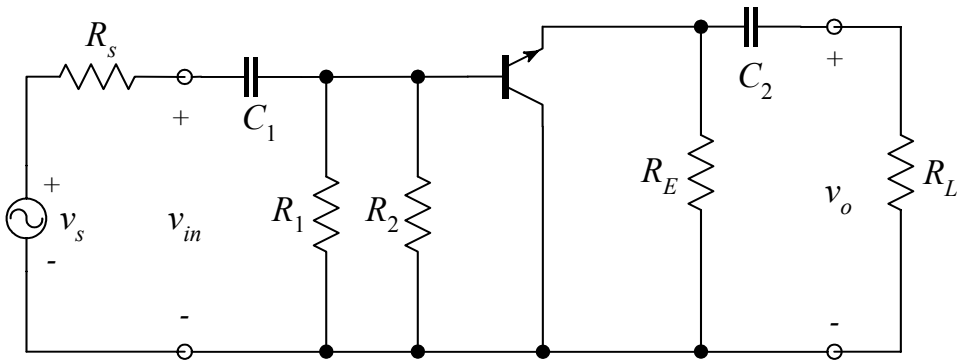
The input signal is between the base and the ground (the collector, since the supply voltage is short circuit for the ac signal); the output signal is between the emitter and the ground (the collector) – **common-collector** amplifier.

$$v_{in} = v_{be} + v_o$$

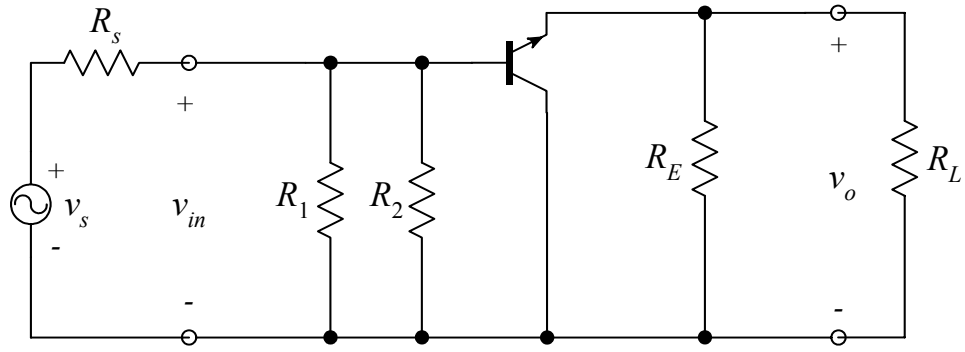
Thus $v_{in} > v_o$ and $A_v < 1$. Usually $A_v \approx 1$ – **emitter follower**.

Typical application as a buffer amplifier, since it has high input impedance and small output impedance.

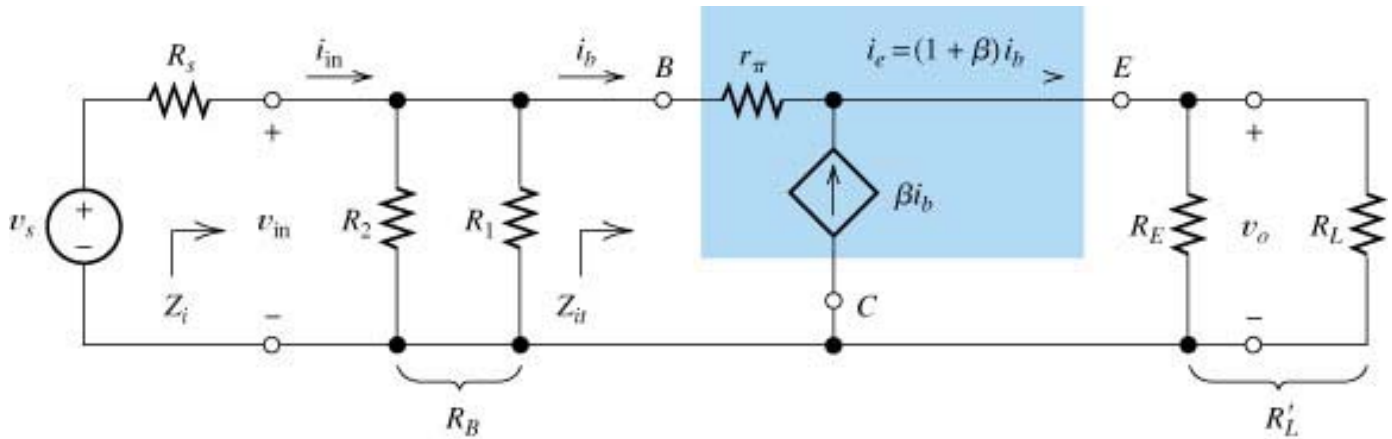
Small - Signal Equivalent Circuit



The first step in creating the small-signal equivalent circuit: the dc voltage sources are replaced by short circuits



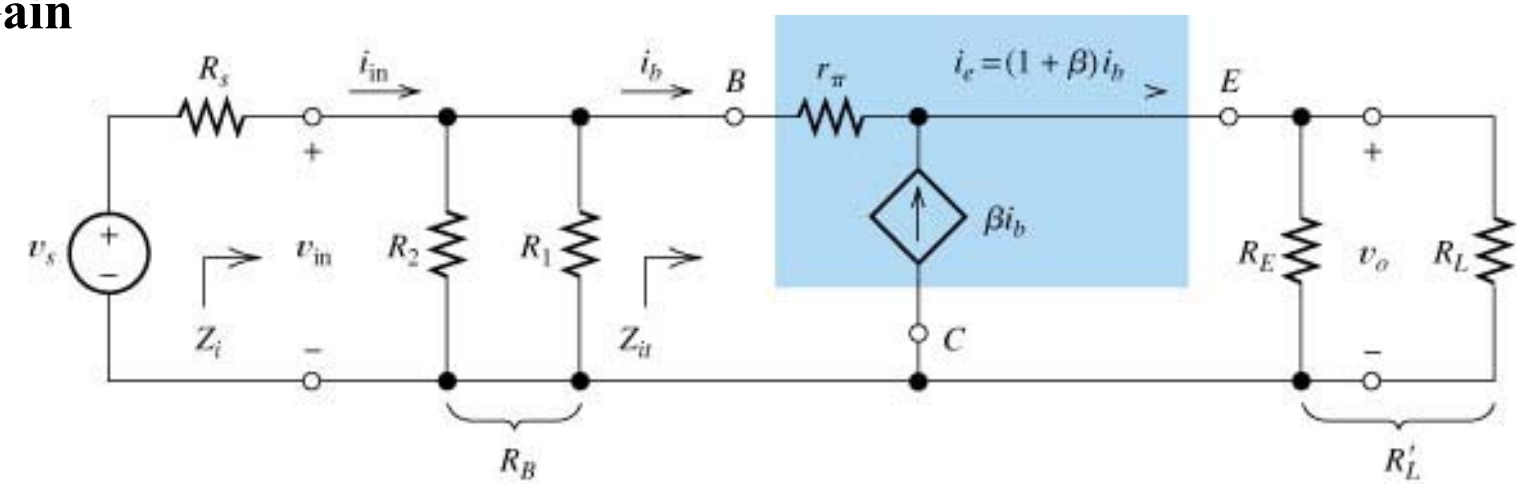
The second step in creating the small-signal equivalent circuit for mid-band region: the the coupling capacitors and the bypass capacitors are replaced by short circuits



(b) Small-signal midband equivalent circuit

Figure 4.36 Emitter follower. (b) Final small-signal mid-band equivalent circuit.

Voltage Gain



(b) Small-signal midband equivalent circuit

Figure 4.36 Emitter follower.

Simplifications:

$$R_B = R_1 \,||\, R_2 = \frac{1}{1/R_1 + 1/R_2} \qquad (4.54)$$

$$R_L' = R_L \,||\, R_E = \frac{1}{1/R_L + 1/R_E} \qquad (4.55)$$

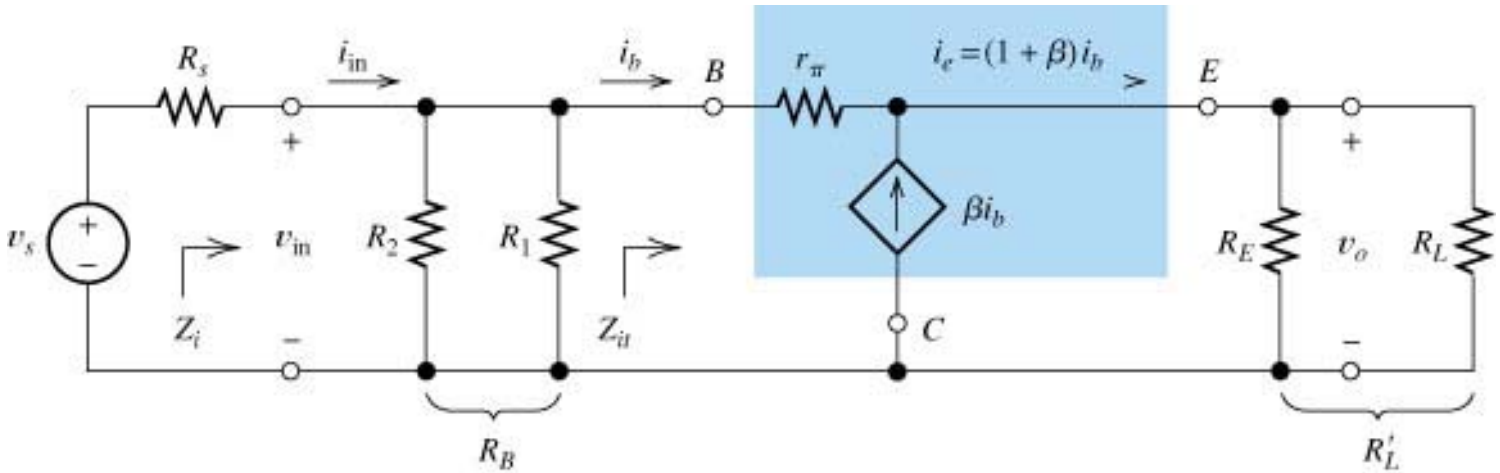
$$v_o = (1+\beta) R_L' i_B \qquad (4.56)$$

$$v_{in} = r_\pi i_b + (1+\beta) i_B R_L' \qquad (4.57)$$

$$A_v = \frac{(1+\beta) R_L'}{r_\pi + (1+\beta) R_L'} < 1 \qquad (4.58)$$

Since usually $(1+\beta)R_L' >> r_\pi$ $\quad A_v \approx 1$.

Input Impedance



(b) Small-signal midband equivalent circuit

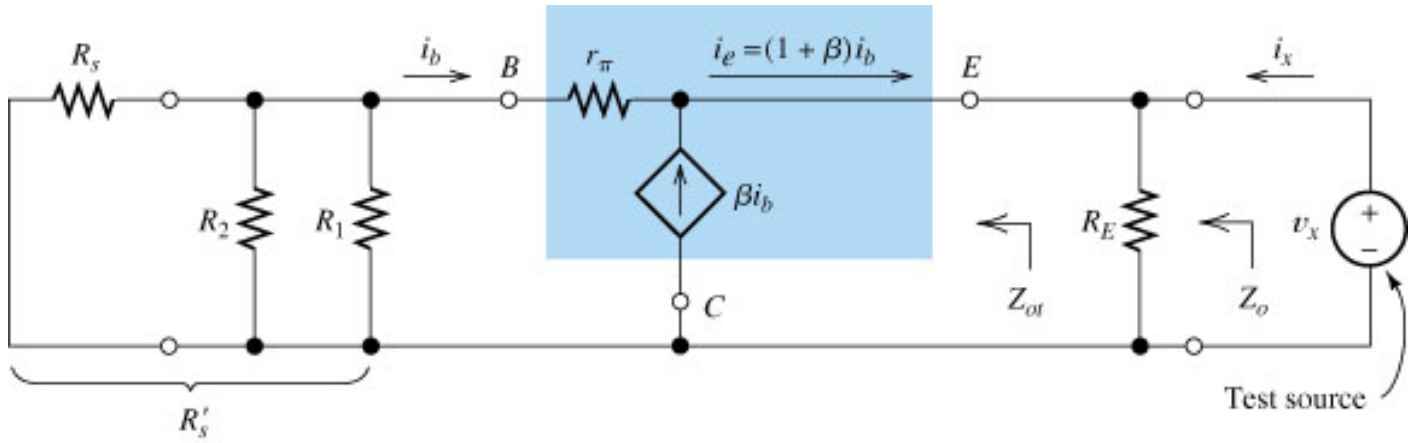
Figure 4.36 Emitter follower.

$$Z_i = \frac{1}{1/R_B + 1/Z_{it}} \qquad (4.59)$$

$$Z_{it} = \frac{v_{in}}{i_b} = r_\pi + (1+\beta)R'_L \qquad (4.60)$$

For small power BJT $R_L{}'$ is in the range of kOhms and β ~ 100. Thus the range of Z_{it} is hundreds of kOhms.

Output Impedance



(c) Equivalent circuit used to find output impedance Z_o

Figure 4.36 Emitter follower.

$$Z_o = \frac{v_x}{i_x} \tag{4.61}$$

$$i_b + \beta i_b + i_x = \frac{v_x}{R_E} \tag{4.62}$$

$$R_s^{'} = \frac{1}{1/R_s + 1/R_1 + 1/R_2} \tag{4.63}$$

$$v_x + r_\pi i_b + R_s^{'} i_b = 0 \tag{4.64}$$

$$Z_o = \frac{v_x}{i_x} = \frac{1}{(1+\beta)/(R'_s + r_\pi) + (1/R_E)} \tag{4.65}$$

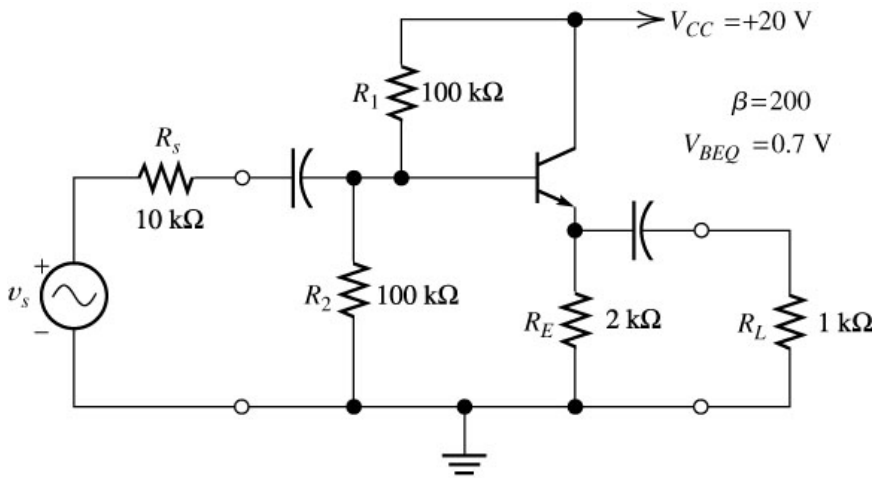
$$Z_{ot} = \frac{R_s^{'} + r_\pi}{(1+\beta)} \tag{4.66}$$

If $R_s' \approx 0$ $\quad Z_{ot} \approx \dfrac{r_\pi}{(1+\beta)} \approx \dfrac{1}{g_m}$

For small power BJT $g_m \sim 10^2..10^3$mS. Thus the range of Z_{ot} is Ohms or tens of Ohms.

Example 4.10 Calculation of Emitter Follower Performance. Compute the voltage gain, input impedance, current gain, power gain, and output impedance of the emitter-follower amplifier displayed in Figure 4.37a.

The dc analysis gives the following quiescent point: $I_{CQ} = 4.12\text{mA}$ and $V_{CE} = 11.7\text{V}$.



(a) Complete circuit

Figure 4.37 Emitter follower of Example 4.10.

Solution

$$r_\pi = \frac{\beta V_T}{I_{CQ}} = \frac{200 \times 0.026}{4.12 \times 10^3} = 1260\Omega$$

$$R_B = \frac{1}{1/R_1 + 1/R_2} = \frac{1}{1/\left(100\times10^3\right) + 1/\left(100\times10^3\right)} = 50\text{k}\Omega$$

$$R_L' = \frac{1}{1/R_L + 1/R_E} = \frac{1}{1/\left(1\times10^3\right) + 1/\left(2\times10^3\right)} = 667\ \Omega$$

$$A_v = \frac{(1+\beta)R_L'}{r_\pi + (1+\beta)R_L'} = \frac{(1+200)\times 667}{1260 + (1+200)\times 667} = 0.991$$

$$Z_{it} = r_\pi + (1+\beta)R_L' = 1260 + (1+200)\times 667 = 135\ k\Omega$$

$$Z_i = \frac{1}{1/R_B + 1/Z_{it}} = \frac{1}{1/\left(50\times10^3\right) + 1/\left(135\times10^3\right)} = 36.5\ k\Omega$$

$$R_s' = \frac{1}{1/R_s + 1/R_1 + 1/R_2}$$

$$= \frac{1}{1/\left(10\times10^3\right) + 1/\left(100\times10^3\right) + 1/\left(100\times10^3\right)} = 8.33\ k\Omega$$

$$Z_o = \frac{1}{(1+\beta)/(R_s' + r_\pi) + (1/R_E)}$$

$$= \frac{1}{(1+200)/\left(8.33\times10^3 + 1260\right) + 1/\left(2\times10^3\right)} = 46.6\ \Omega$$

$$A_i = A_v \frac{Z_i}{R_L} = 0.991\frac{36.5\times10^3}{1\times10^3} = 36.2;\ G = A_v A_i = 38.8$$

4.9 The BJT as a Digital Logic Switch

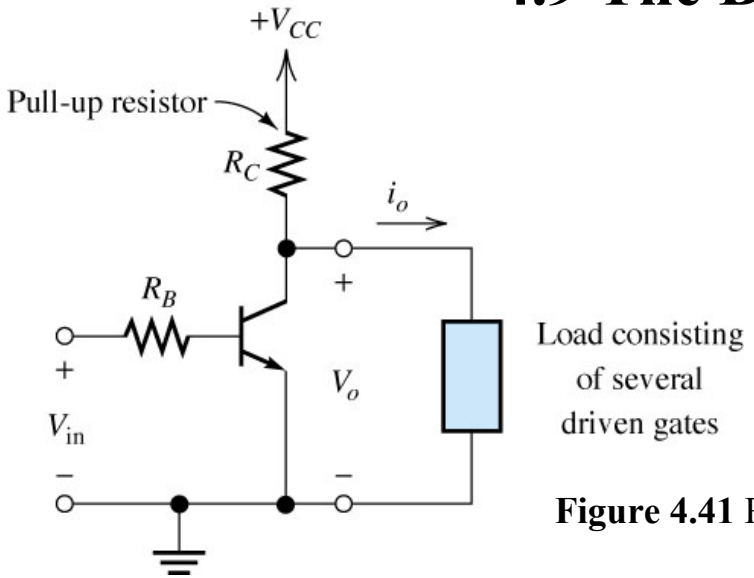


Figure 4.41 RTL inverter.

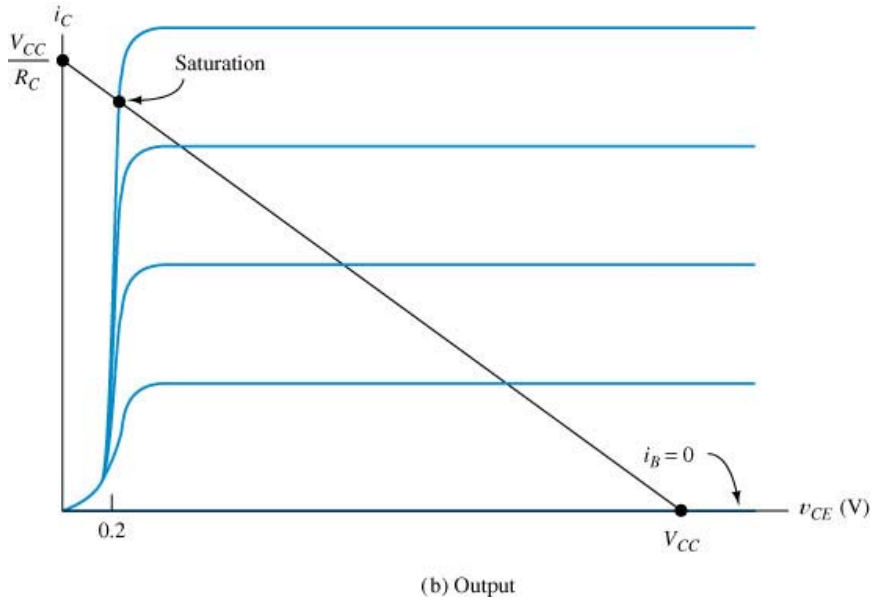


Figure 4.42b Load-line analysis of RTL inverter under no-load conditions.

The circuit in Fig. 4.41 is a modification of common-emitter amplifier intended for operation in saturation and in cut-off region only.

<u>*Cut-off state*</u>: $V_{\text{in}} < 0.5$ (**logical zero**). BJT is in cut-off and $I_C = 0$. There is no voltage drop across R_C and $V_o = +V_{CC}$ (**logical one**).

<u>*Saturation state*</u>: V_{in} is high (**logical one**), usually $V_{in} \approx +V_{CC}$.

$$i_B = \frac{V_{in} - 0.7}{R_B}$$

In saturation $V_{CE} < 0.2\text{V}$. This $V_o = V_{CE} < 0.2\text{V}$ (**logical zero**).

$$i_C = \frac{V_{CC} - 0.7}{R_C}$$

To have saturation region, R_B and R_C must be designed in such a way that $\boldsymbol{\beta i_B > i_C}$.

The output has logically opposite voltage to the input (zero-one; one-zero). The circuit is called **logical inverter**.

RTL NOR Gate

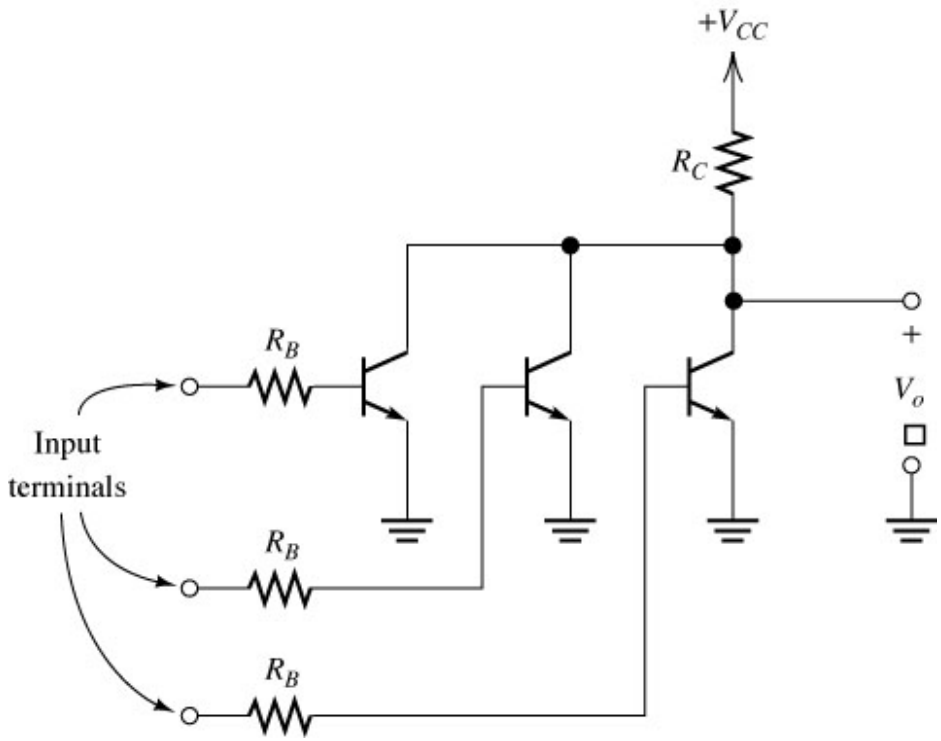


Figure 4.45 Three-input RTL NOR gate.

When at the three inputs are applied low voltages (logical zeros) all BJT are in cutoff, no current flows through R_C and $V_o = +V_{CC}$ (logical one).

When a high voltage is presenting at one or more of the inputs (logical ones at these inputs) the corresponding BJTs are in saturation and $V_o <$ 0.2V (logical zero).