ĐẠI HỌC QUỐC GIA THÀNH PHỐ HỒ CHÍ MINH
TRƯỜNG KHOA HỌC TỰ NHIÊN

VẬT LÝ LINH KIỆN ĐIỆN TỬ

Chap 3:

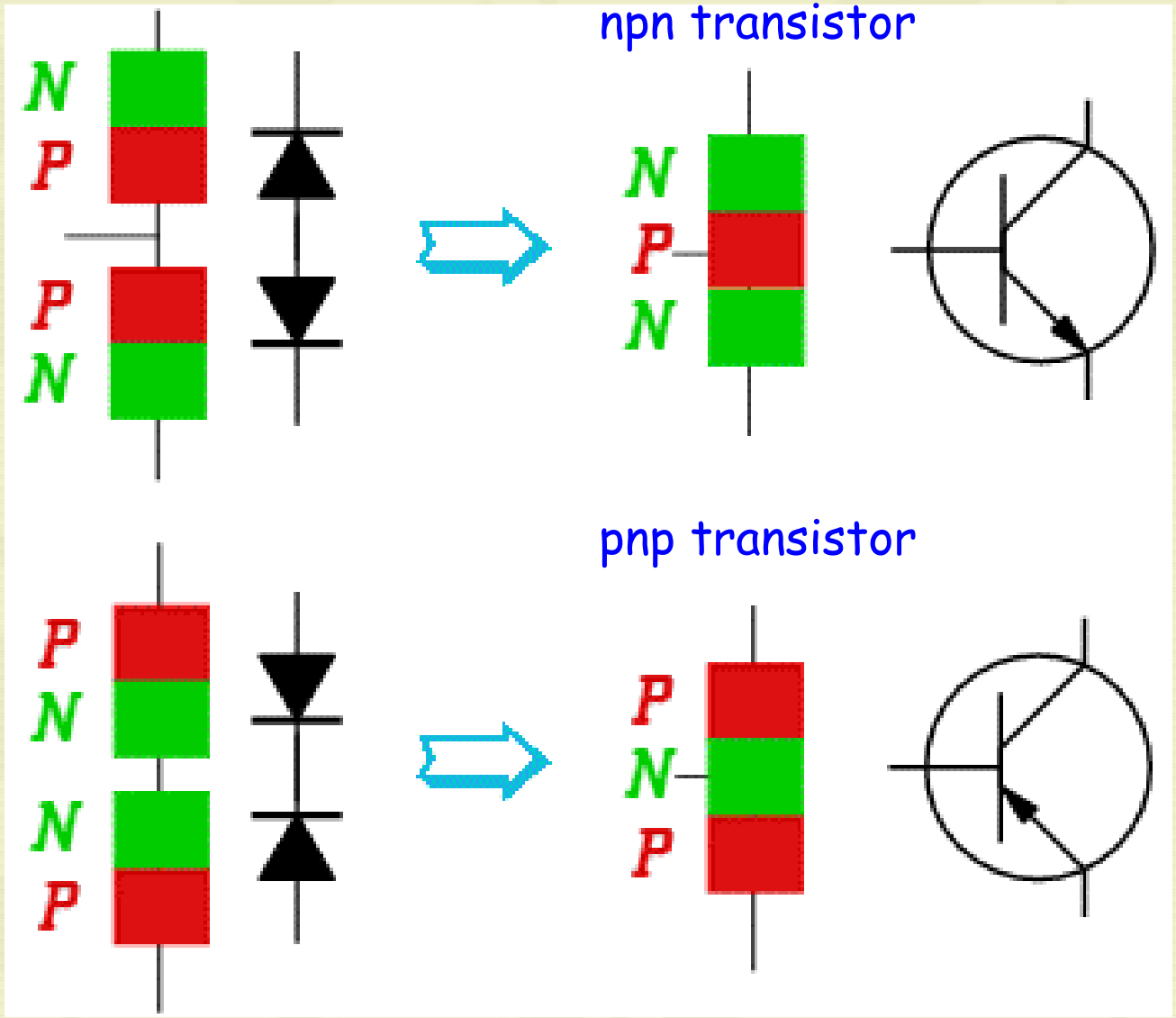
BJT – BIPOLAR JUCNTION TRANSISTOR

Trình bày: NGUYỄN THỊ THIÊN TRANG

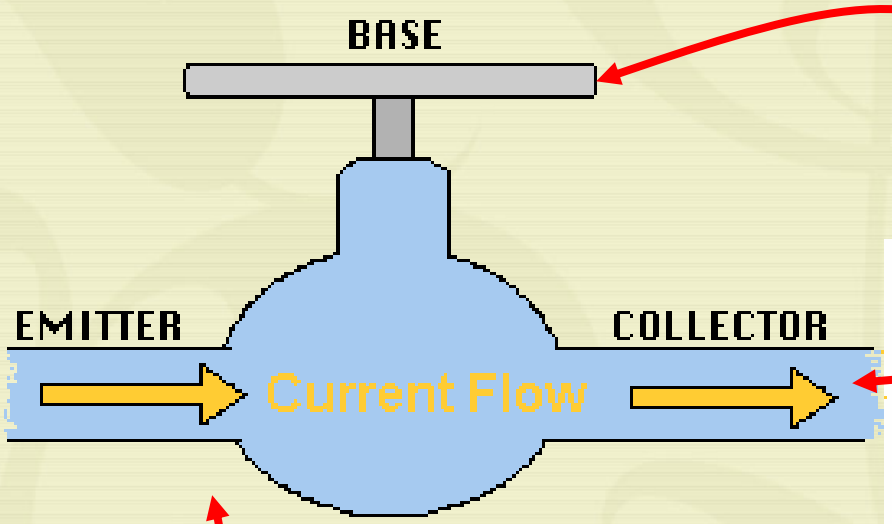
GIỚI THIỆU CHUNG

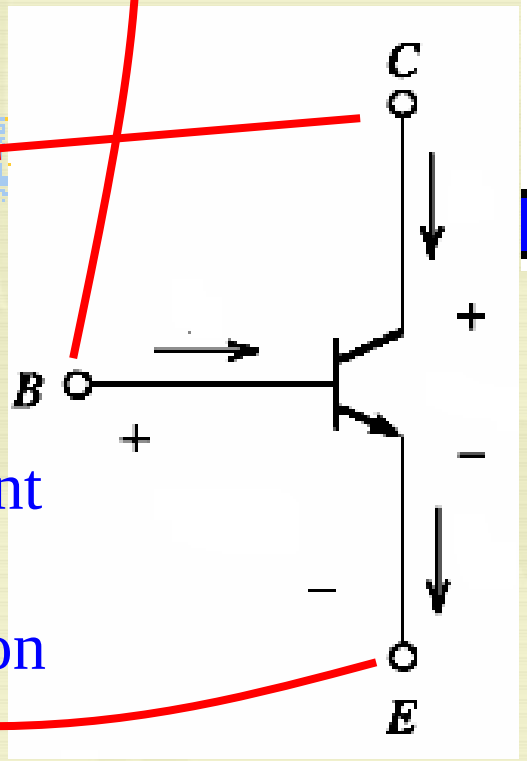
- Cấu tạo & nguyên lý hoạt động BJT
- Các cách mắc mạch & các dạng đặc tuyến tương ứng
- Phân cực cho BJT
- Các mô hình tương đương của BJT
- Phân loại BJT
- Một số ứng dụng BJT
- Giản đồ năng lượng BJT
- Quy trình chế tạo BJT

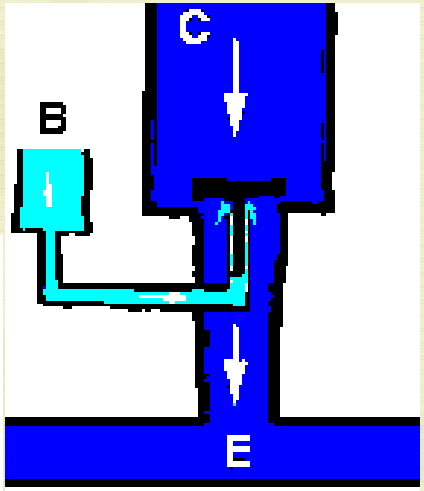
CẤU TẠO TRANSISTOR



CẤU TẠO TRANSISTOR







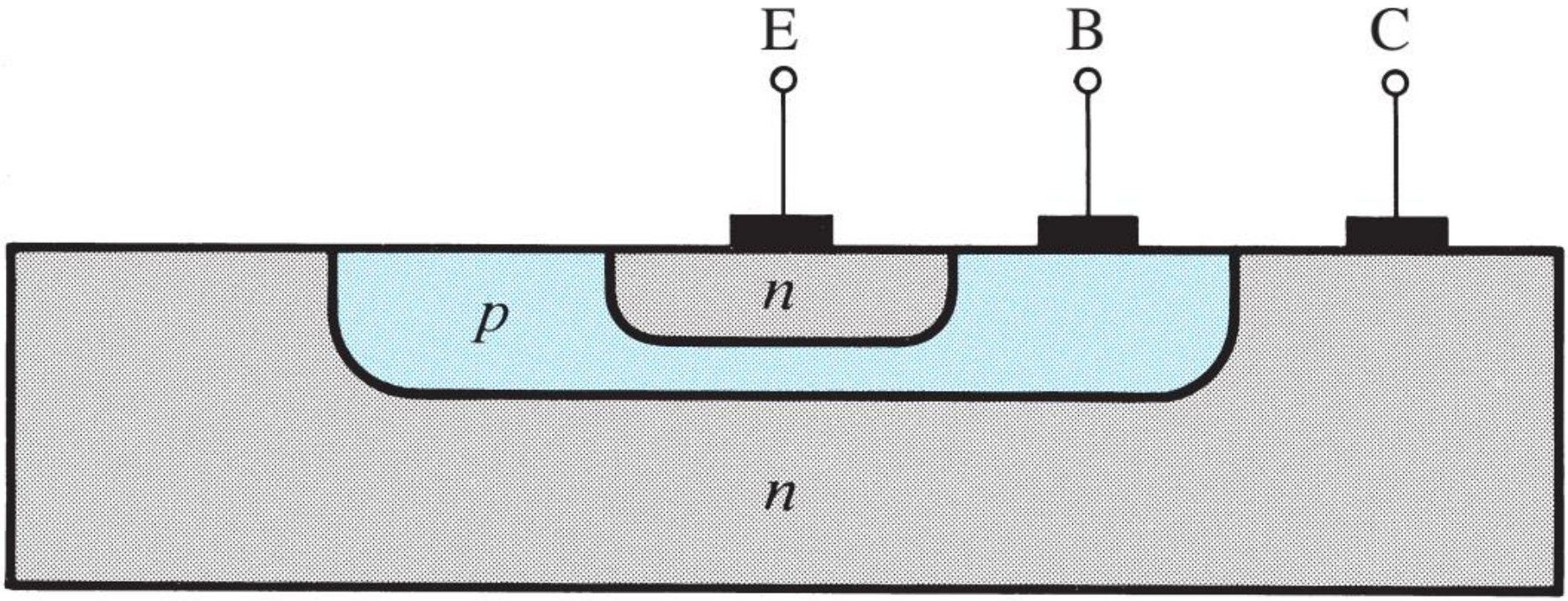
force – voltage/current

water flow – current

- amplification

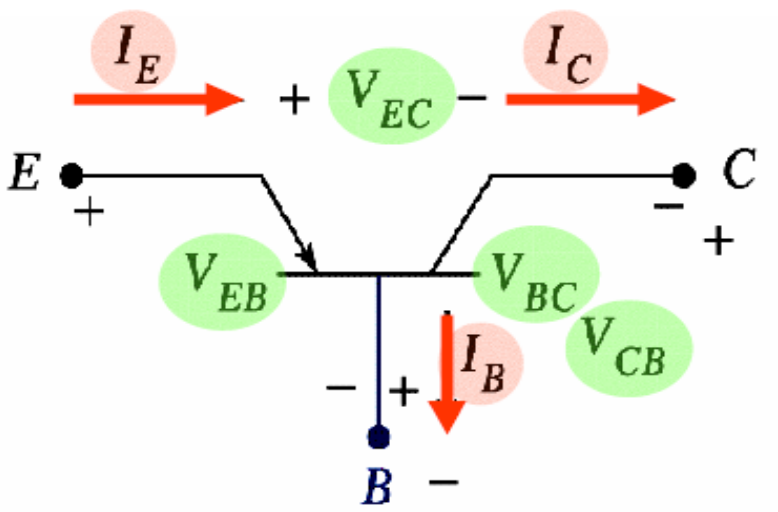
Understanding of BJT

CẤU TẠO TRANSISTOR

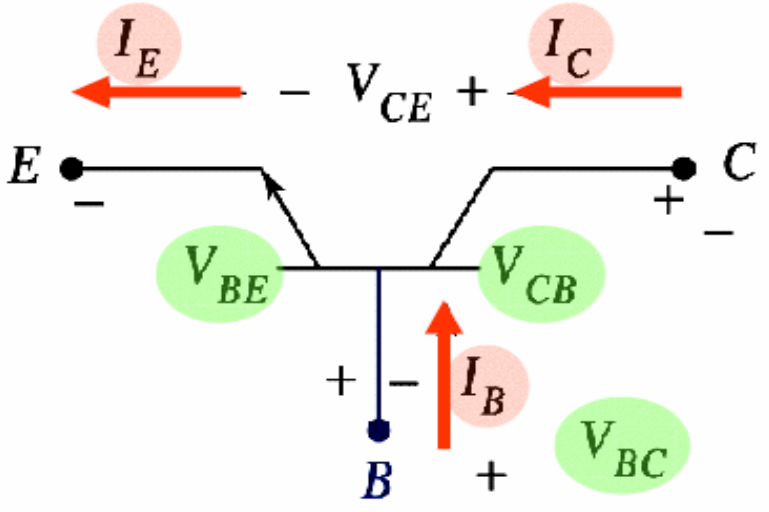


Cấu tạo mặt cắt ngang của transistor NPN

CẤU TẠO TRANSISTOR



pnp



npn

Two of the currents and two of the voltages are independent.
If two of the currents or voltages are known, third terminal current or voltage is determined.

$$I_E = I_B + I_C$$
$$V_{EB} + V_{BC} + V_{CE} = 0$$

Current flowing into a device
= current flowing out of device

$(V_{CE} = - V_{EC})$

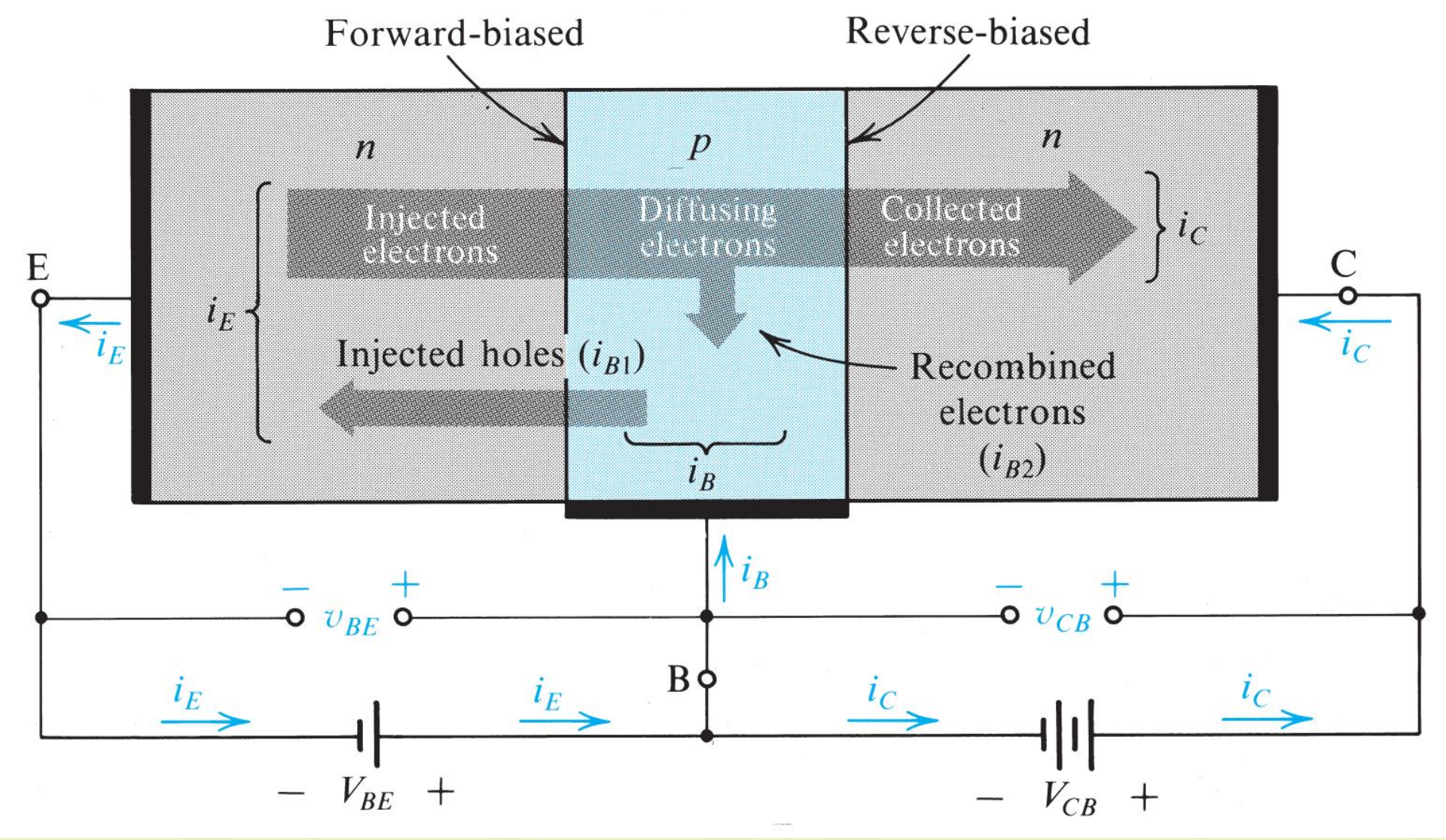
CẤU TẠO TRANSISTOR

- Vùng phát E pha đậm,
- Vùng nền rất hẹp và pha lợt (nhẹ)
- Vùng thu C lớn nhất và pha trung gian giữa vùng phát pha đậm và vùng nền pha lợt

→ Tên gọi nhằm ám chỉ:

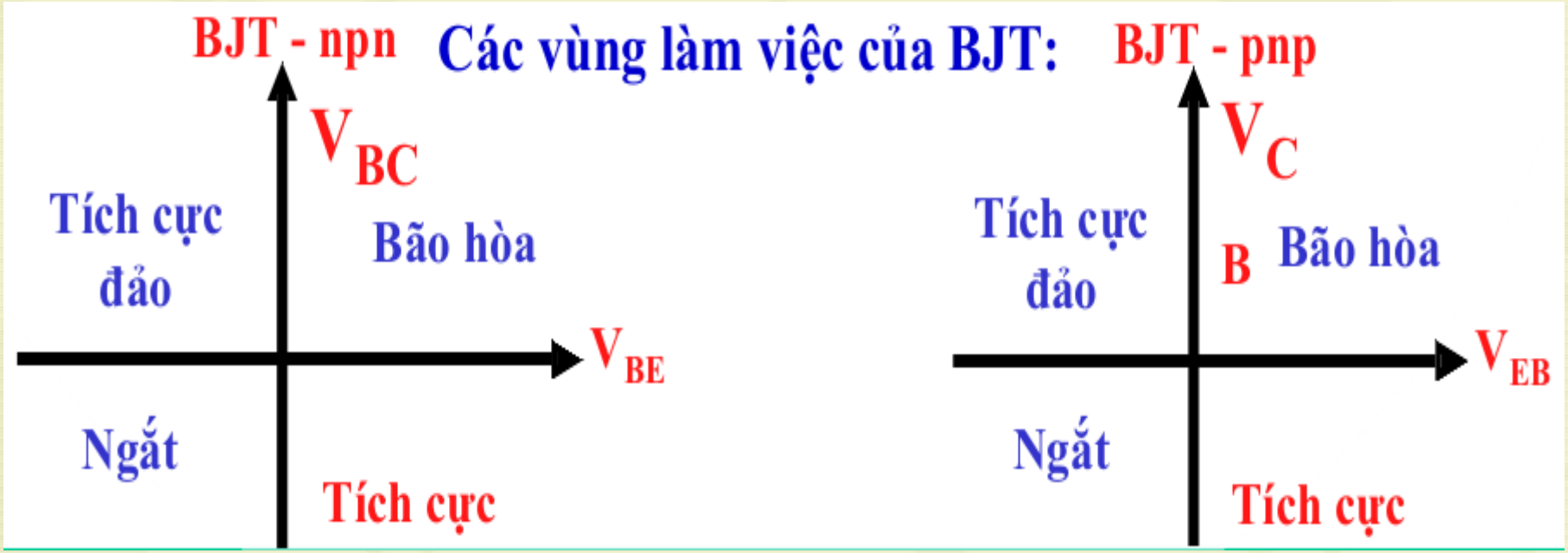
Cực phát (Emitter) phát các hạt tải đến cực thu (collector) và dòng hạt tải này được điều khiển bởi cực nền (base)

NGUYÊN LÝ HOẠT ĐỘNG

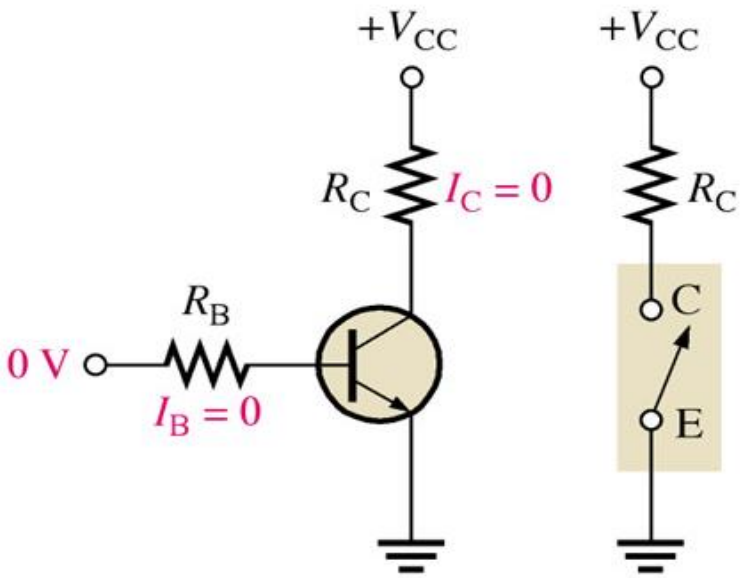


NGUYÊN LÝ HOẠT ĐỘNG

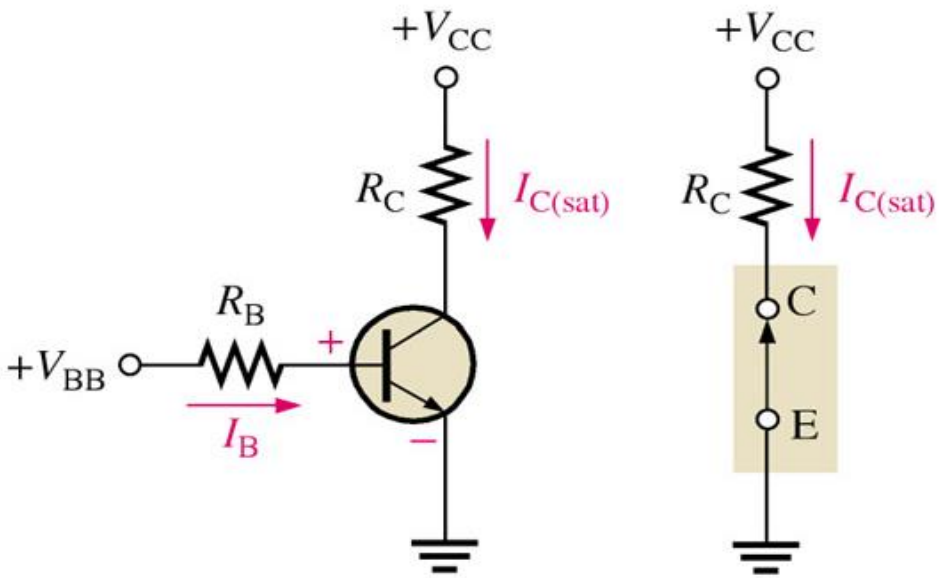
+ Chế độ đảo (tích cực đảo): Tiếp giáp BE phân cực ngược, tiếp giáp BC phân cực thuận, đây là chế độ không mong muốn



NGUYÊN LÝ HOẠT ĐỘNG



(a) Cutoff — open switch

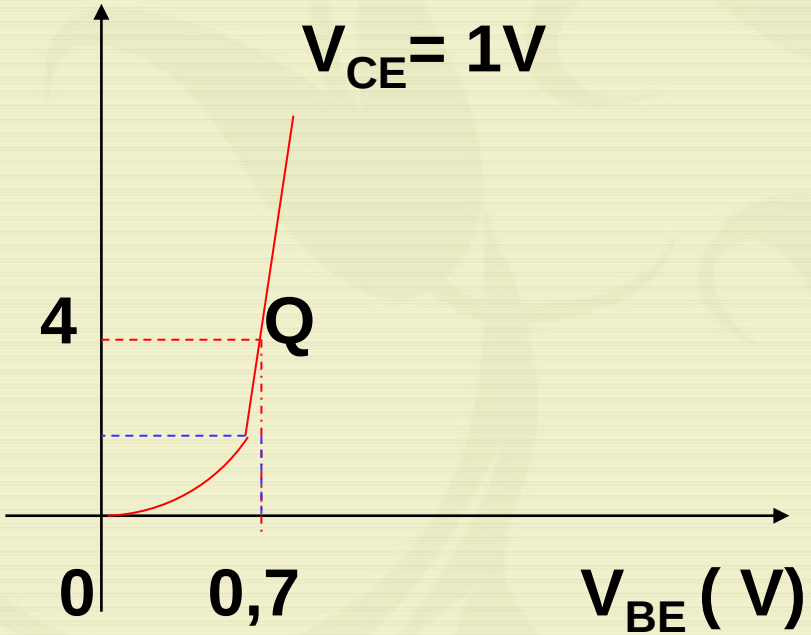


(b) Saturation — closed switch

BJT RÁP CE – ĐẶC TUYẾN

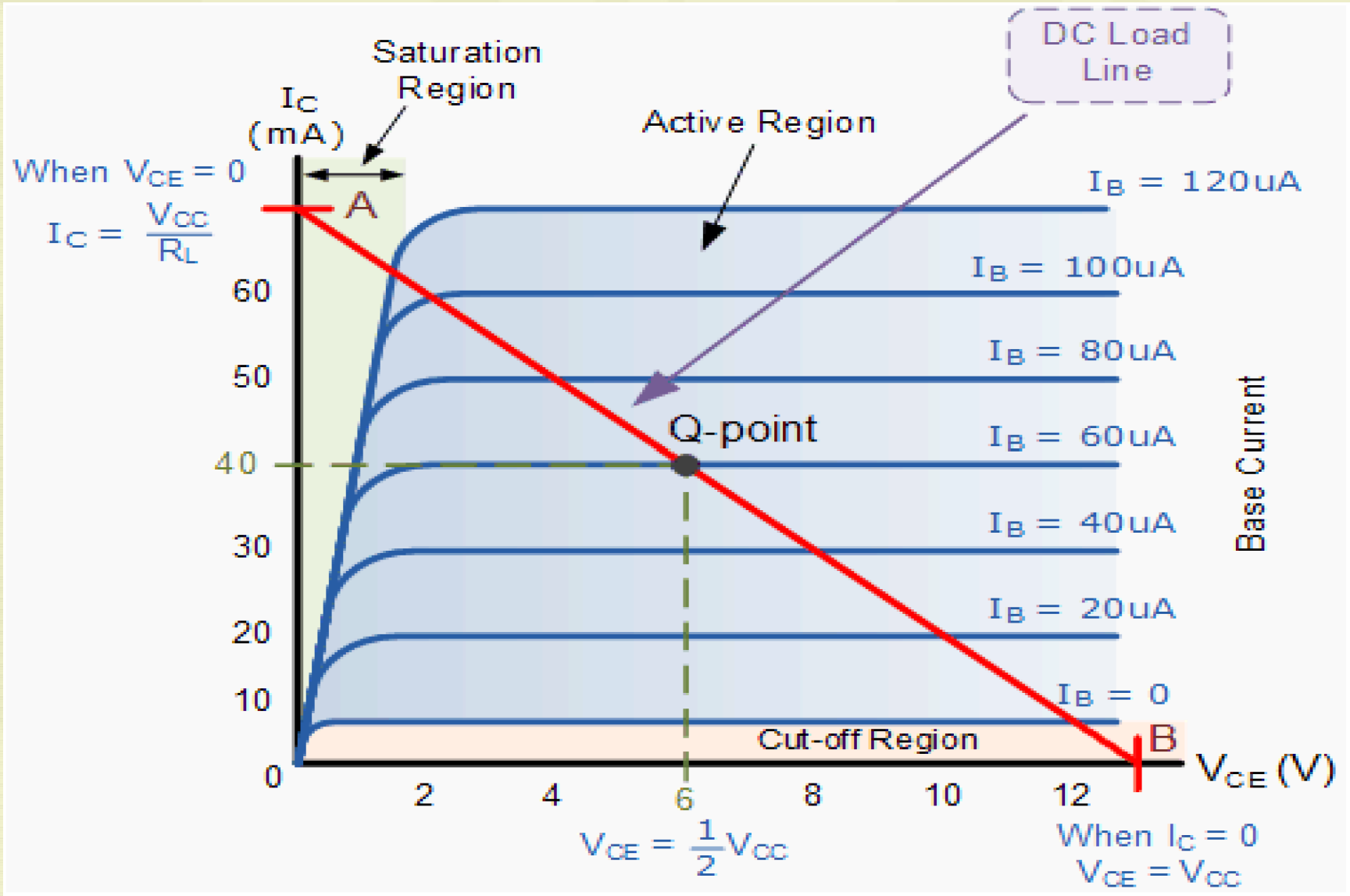
- Gồm có 3 đặc tuyến thông dụng sau:

a. Đặc tuyến vào $I_B = f(V_{BE})$ $V_{CE} = Cte$



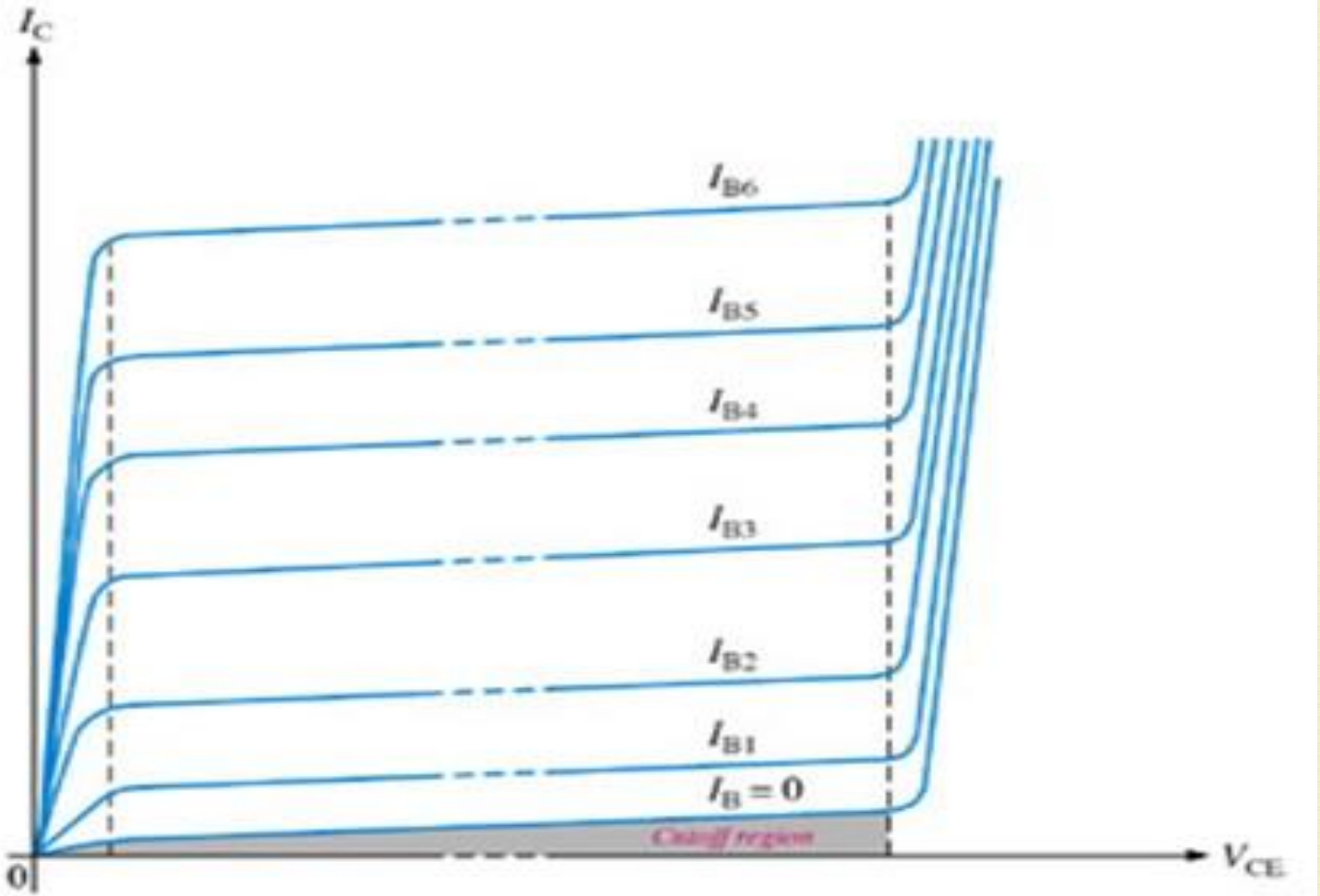
BJT RÁP CE – ĐẶC TUYẾN

b. Đặc tuyến ra $I_C = f(V_{CE})$ I_B =Cte



BJT RÁP CE – ĐẶC TUYẾN

b. Đặc tuyến ra $I_C = f(V_{CE})$ I_B =Cte

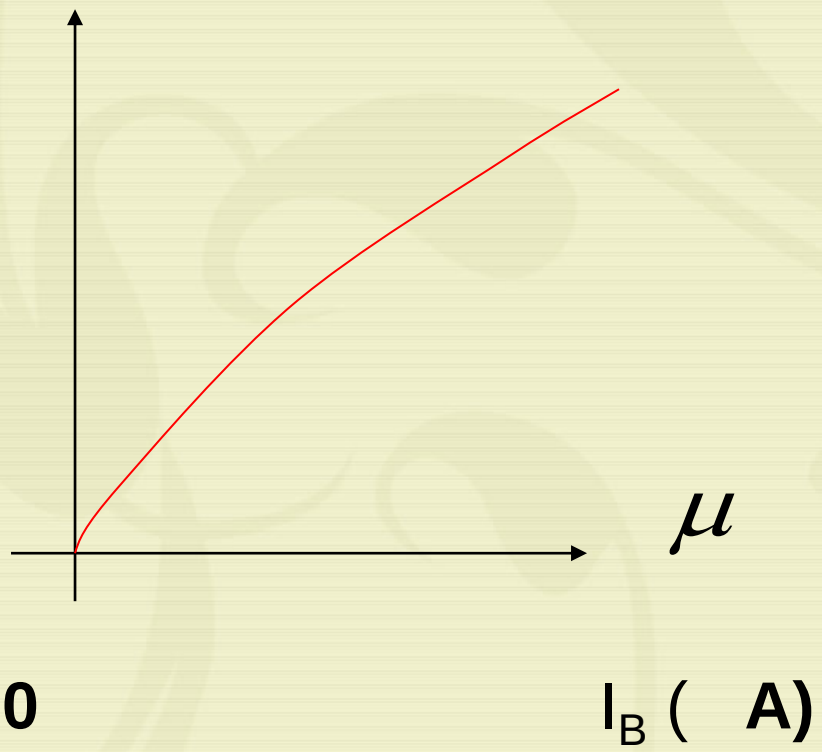


(c) Family of I_C versus V_{CE} curves for several values of I_B ($I_{B1} < I_{B2} < I_{B3}$, etc.)

BJT RÁP CE – ĐẶC TUYẾN

c. Đặc tuyến truyền IC = f (IB) V_{CE} = Cte

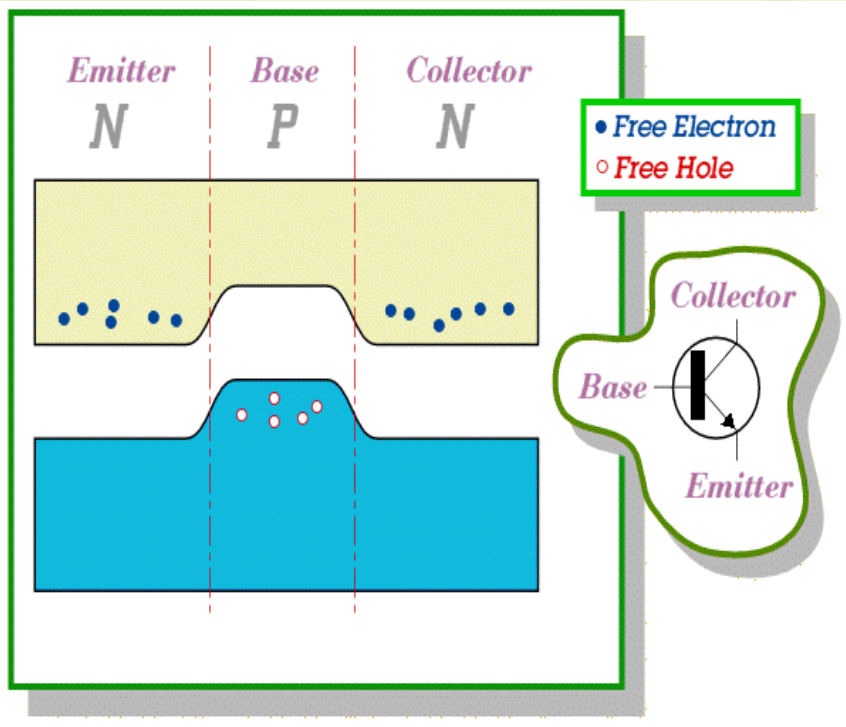
- **Trong dải thay đổi nhỏ của I_B, I_C thay đổi tuyến tính.**
- **Khi dòng I_B lớn , I_C không còn tuyến tính**



Characteristic	Common Base	Common Emitter	Common Collector
Input Impedance	Low	Medium	High
Output Impedance	Very High	High	Low
Phase Angle	0^{o}	180^{o}	0^{o}
Voltage Gain	High	Medium	Low
Current Gain	Low	Medium	High
Power Gain	Low	Very High	Medium

BJT GIẢN ĐỒ NĂNG LƯỢNG

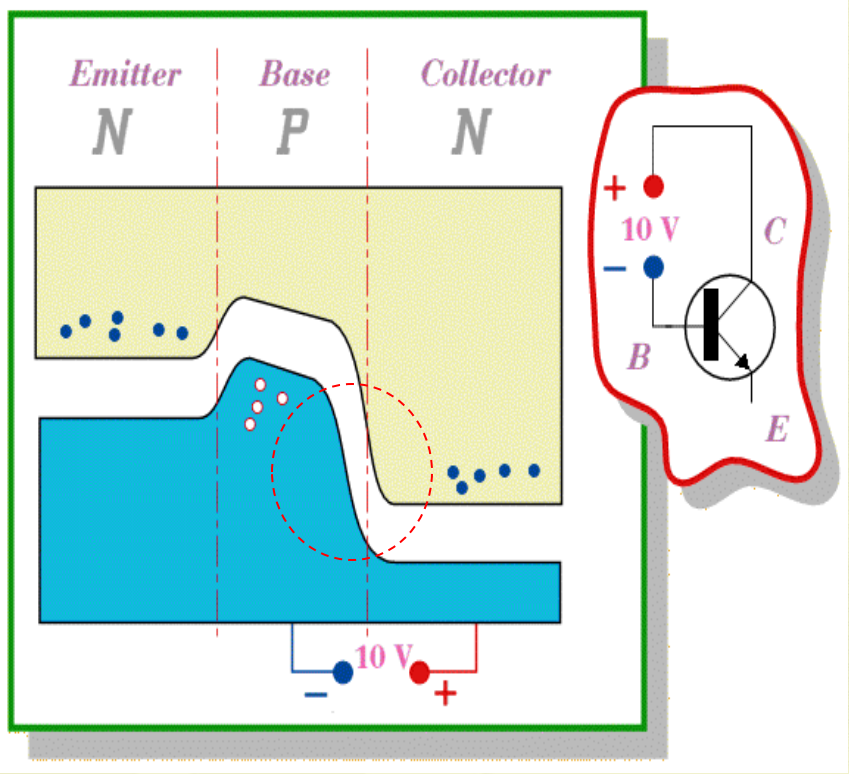
How the BJT works



NPN Bipolar Transistor

- Figure shows the energy levels in an NPN transistor under no externally applying voltages.
- In each of the N-type layers conduction can take place by the free movement of electrons in the conduction band.
- In the P-type (filling) layer conduction can take place by the movement of the free holes in the valence band.
- However, in the absence of any externally applied electric field, we find that depletion zones form at both PN-Junctions, so no charge wants to move from one layer to another.

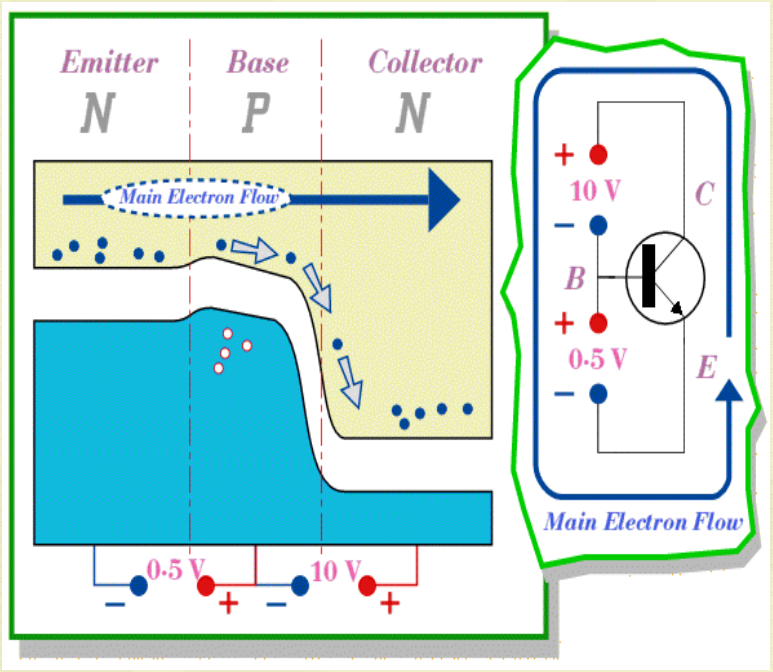
How the BJT works



Apply a Collector-Base voltage

- What happens when we apply a moderate voltage between the collector and base parts.
- The polarity of the applied voltage is chosen to increase the force pulling the N-type electrons and P-type holes apart.
- This widens the depletion zone between the collector and base and so no current will flow.
- In effect we have reverse-biassed the Base-Collector diode junction.

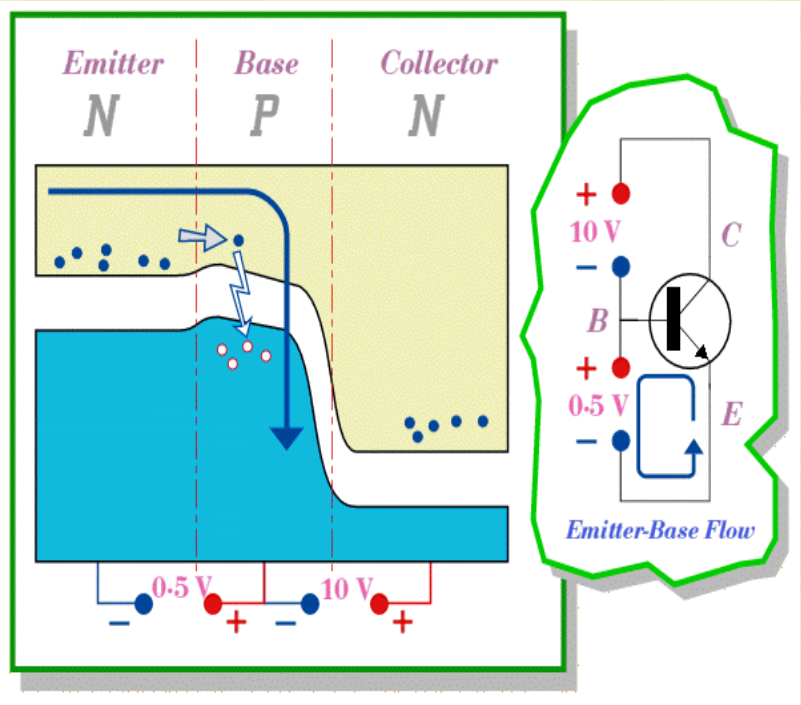
Charge Flow



Apply an Emitter-Base voltage

- What happens when we apply a relatively small Emitter-Base voltage whose polarity is designed to forward-bias the Emitter-Base junction.
- This 'pushes' electrons from the Emitter into the Base region and sets up a current flow across the Emitter-Base boundary.
- Once the electrons have managed to get into the Base region they can respond to the attractive force from the positively-biassed Collector region.
- As a result the electrons which get into the Base move swiftly towards the Collector and cross into the Collector region.
- Hence a Emitter-Collector current magnitude is set by the chosen Emitter-Base voltage applied.
- Hence an external current flowing in the circuit.

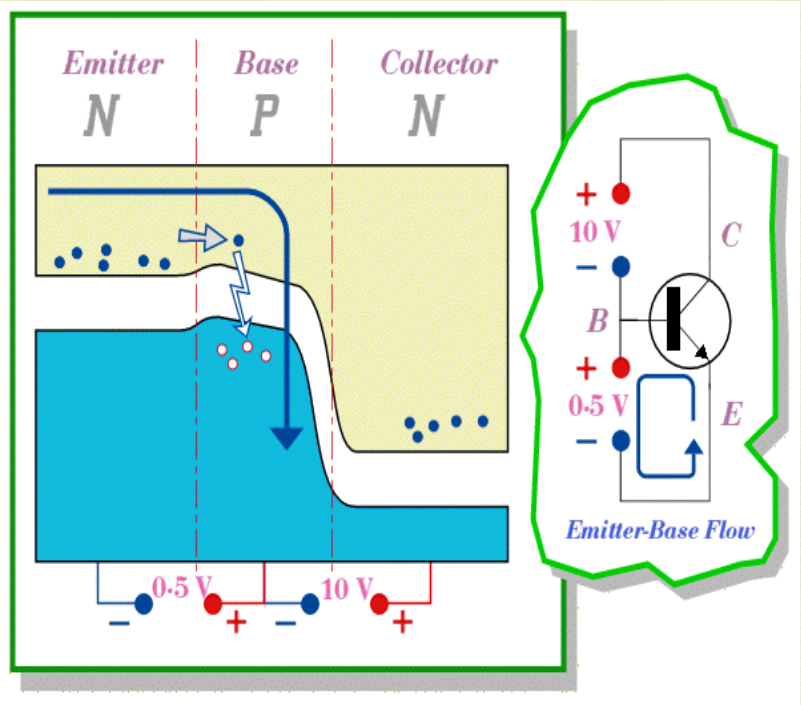
Charge Flow



Some electron fall into a hole

- Some of free electrons crossing the Base encounter a hole and 'drop into it'.
- As a result, the Base region loses one of its positive charges (holes).
- The Base potential would become more negative (because of the removal of the holes) until it was negative enough to repel any more electrons from crossing the Emitter-Base junction.
- The current flow would then stop.

Charge Flow

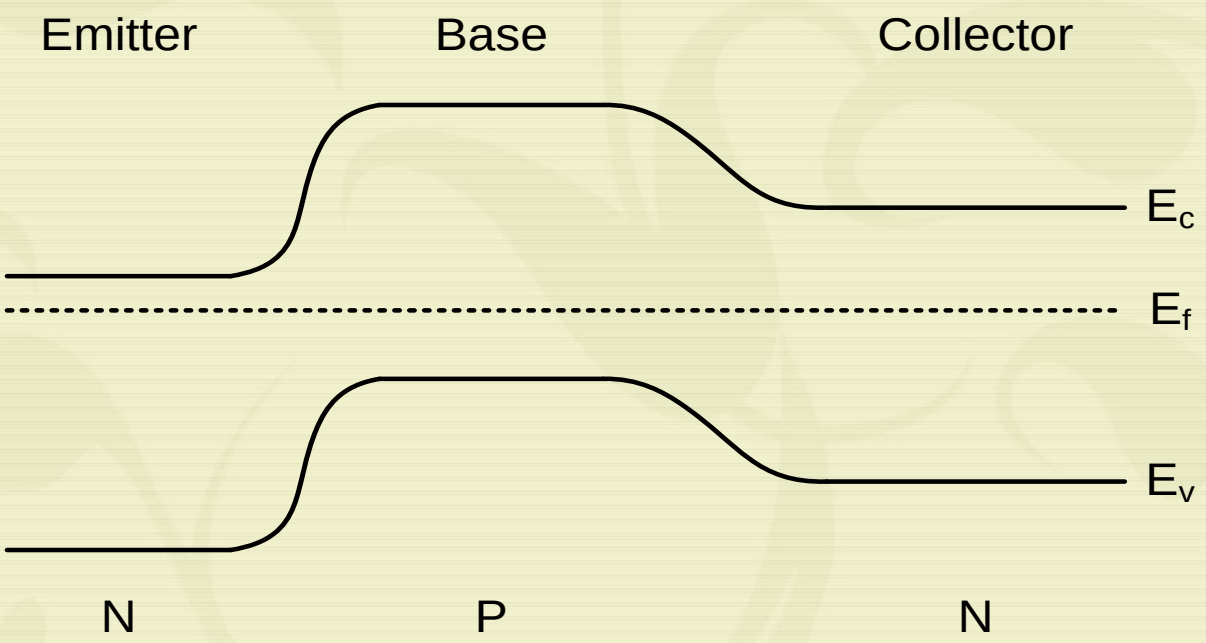


Some electron fall into a hole

- To prevent this happening we use the applied E-B voltage to remove the captured electrons from the base and maintain the number of holes.
- The effect, some of the electrons which enter the transistor via the Emitter emerging again from the Base rather than the Collector.
- For most practical BJT only about 1% of the free electrons which try to cross Base region get caught in this way.
- Hence a Base current, I_B, which is typically around one hundred times smaller than the Emitter current, I_E.

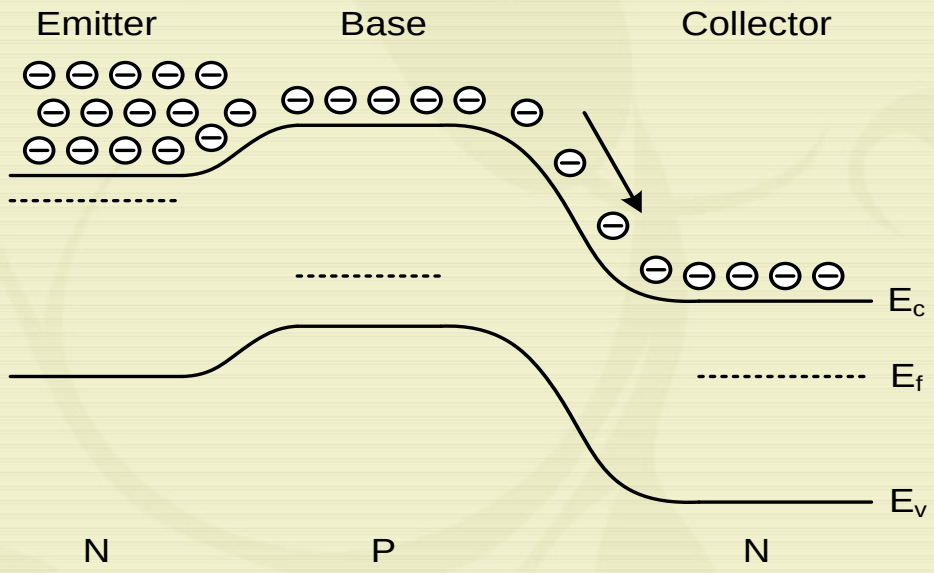
GIẢN ĐỒ NĂNG LƯỢNG

Trạng thái cân bằng - không có dòng chuyển dời của hoạt mang điện



GIẢN ĐỒ NĂNG LƯỢNG

- EB phân cực thuận
  - Rào thế giản và các electron khuếch tán dần sang cực B
  - Các electron quét qua cực B để đến C
- CB phân cực nghịch
  - Electron dịch chuyển xuống từ E sang C

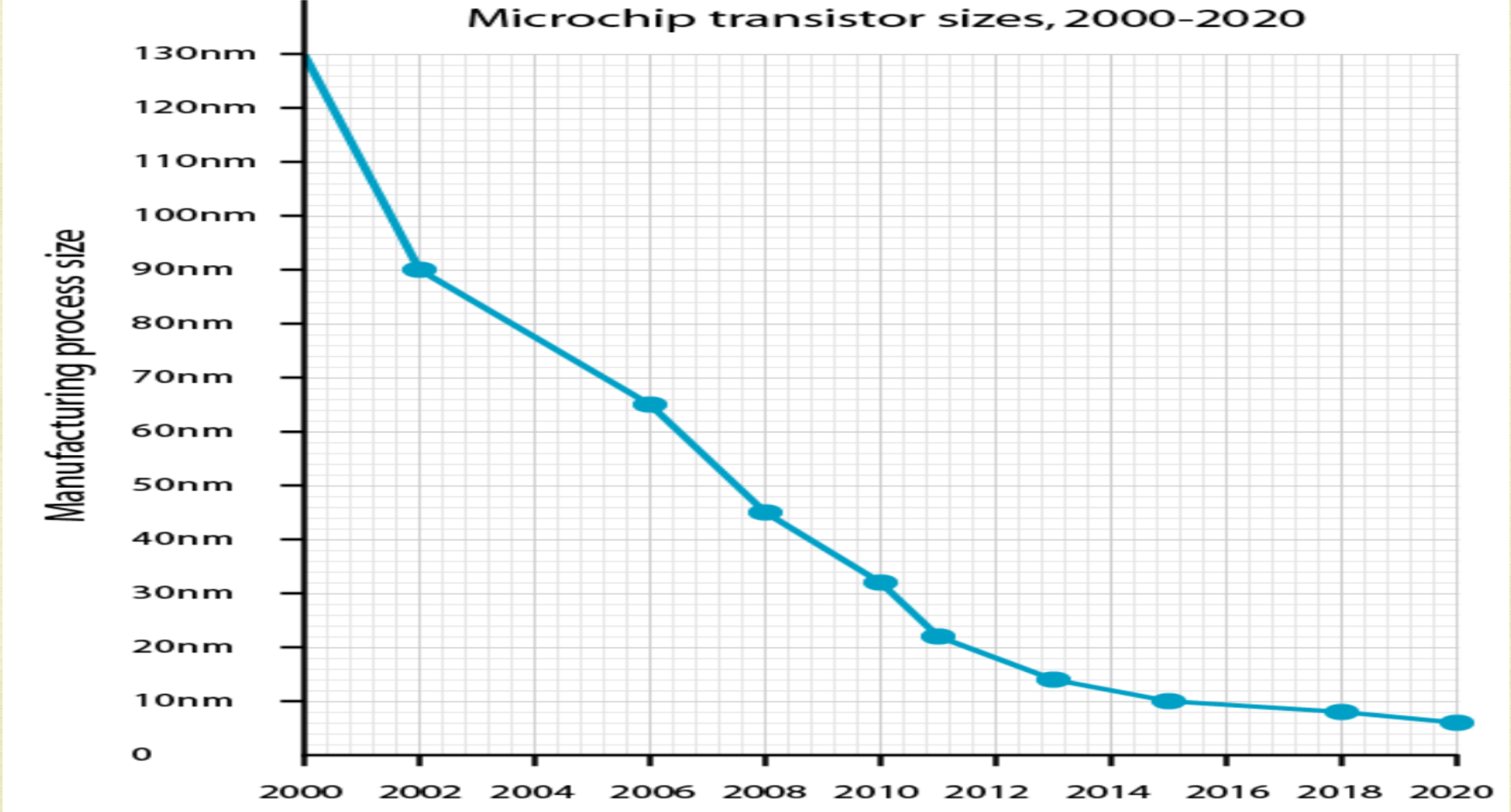


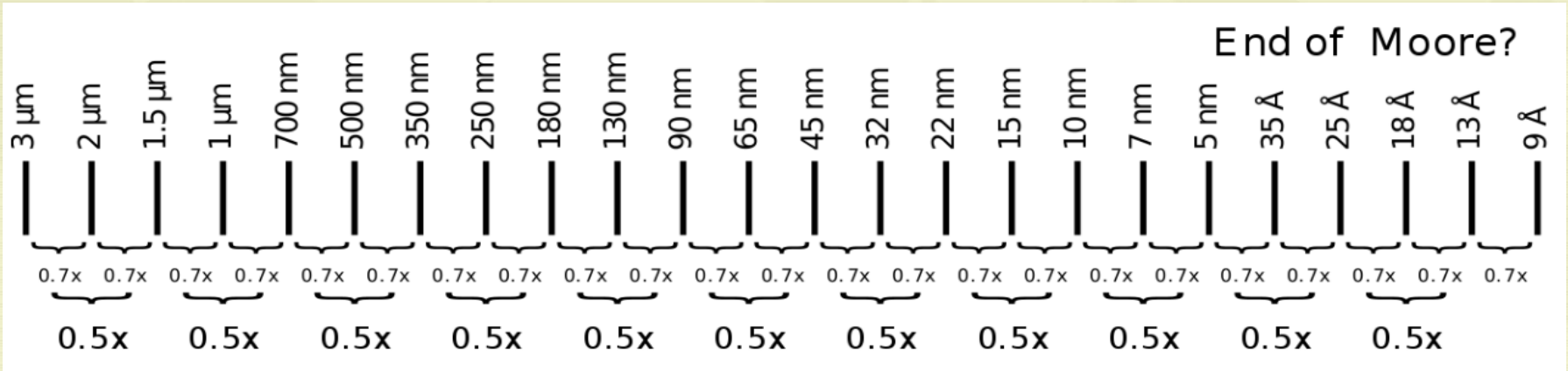
FABRICATION PROCESS

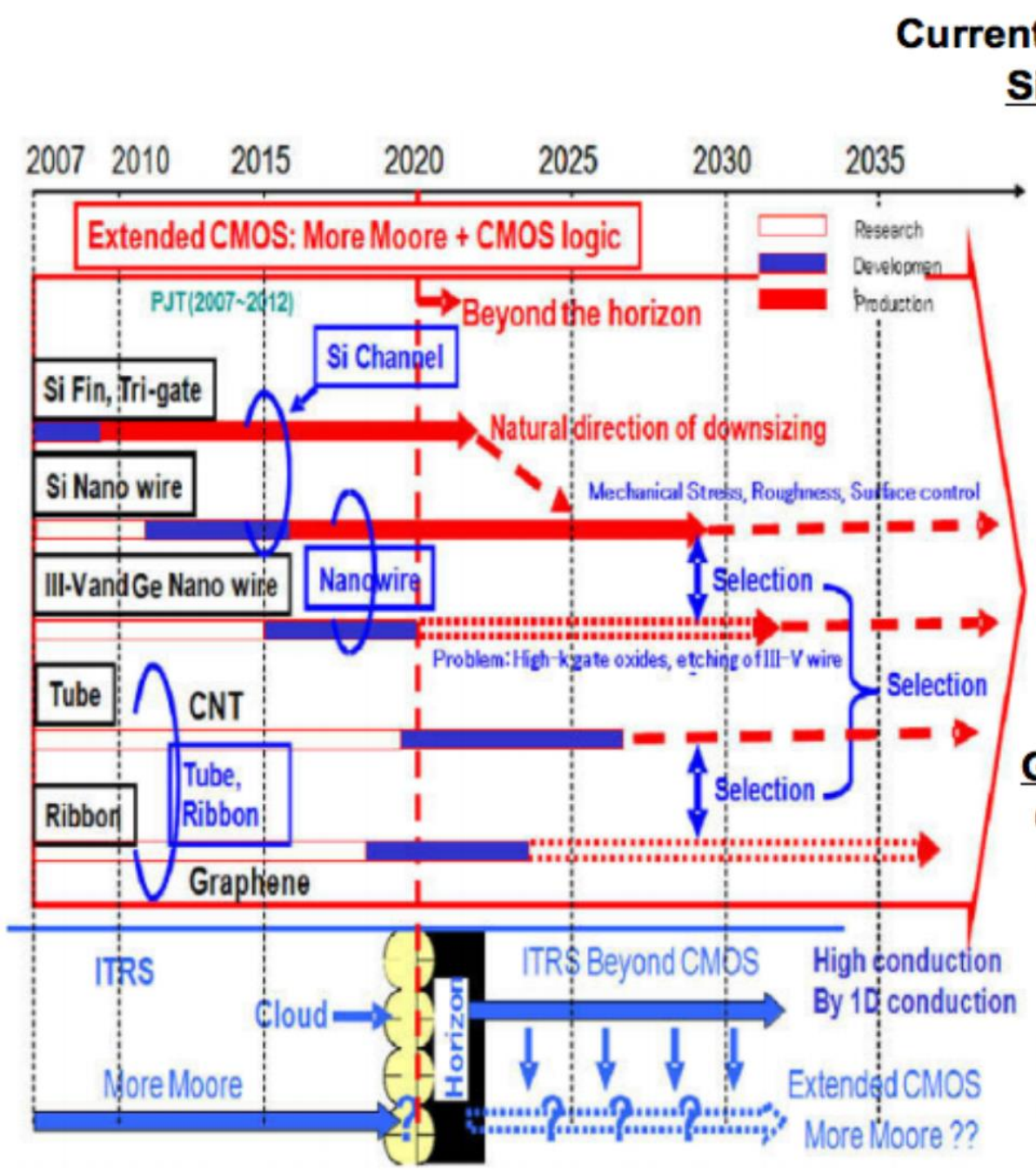
https://www.youtube.com/watch?v=fwNkg1fsqBY

MINIMUM FEATURE SIZE

Year	Processor	Speed	Transistors	Process
1982	i286	6 - 25 MHz	~134,000	1.5 μm
1986	i386	16 – 40 MHz	~270,000	1 μm
1989	i486	16 - 133 MHz	~1 million	.8 μm
1993	Pentium	60 - 300 MHz	~3 million	.6 μm
1995	Pentium Pro	150 - 200 MHz	~4 million	.5 μm
1997	Pentium II	233 - 450 MHz	~5 million	.35 μm
1999	Pentium III	450 – 1400 MHz	~10 million	.25 μm
2000	Pentium 4	1.3 – 3.8 GHz	~50 million	.18 μm
2005	Pentium D	2 cores/package	~200 million	.09 μm
2006	Core 2	2 cores/die	~300 million	.065 μm
2008	Core i7	4 cores/die	~800 million	.040 μm
2010	“Sandy Bridge”	8 cores/die	??	.032 μm


Microchip transistor sizes, 2000-2020
Manufacturing process size
130nm
120nm
110nm
100nm
90nm
80nm
70nm
60nm
50nm
40nm
30nm
20nm
10nm
0
2000
2002
2004
2006
2008
2010
2012
2014
2016
2018
2020


End of Moore?
3 µm
2 µm
1.5 µm
1 µm
700 nm
500 nm
350 nm
250 nm
180 nm
130 nm
90 nm
65 nm
45 nm
32 nm
22 nm
15 nm
10 nm
7 nm
5 nm
35 Å
25 Å
18 Å
13 Å
9 Å
0.7x
0.5x



Current Issues

Si Nanowire

Control of wire surface property

Source Drain contact

Optimization of wire diameter

Compact I-V model

III-V & Ge Nanowire

High-k gate insulator

Wire formation technique

CNT:

Growth and integration of CNT

Width and Chirality control

Chirality determines conduction types: metal or semiconductor

Graphene:

Graphene formation technique

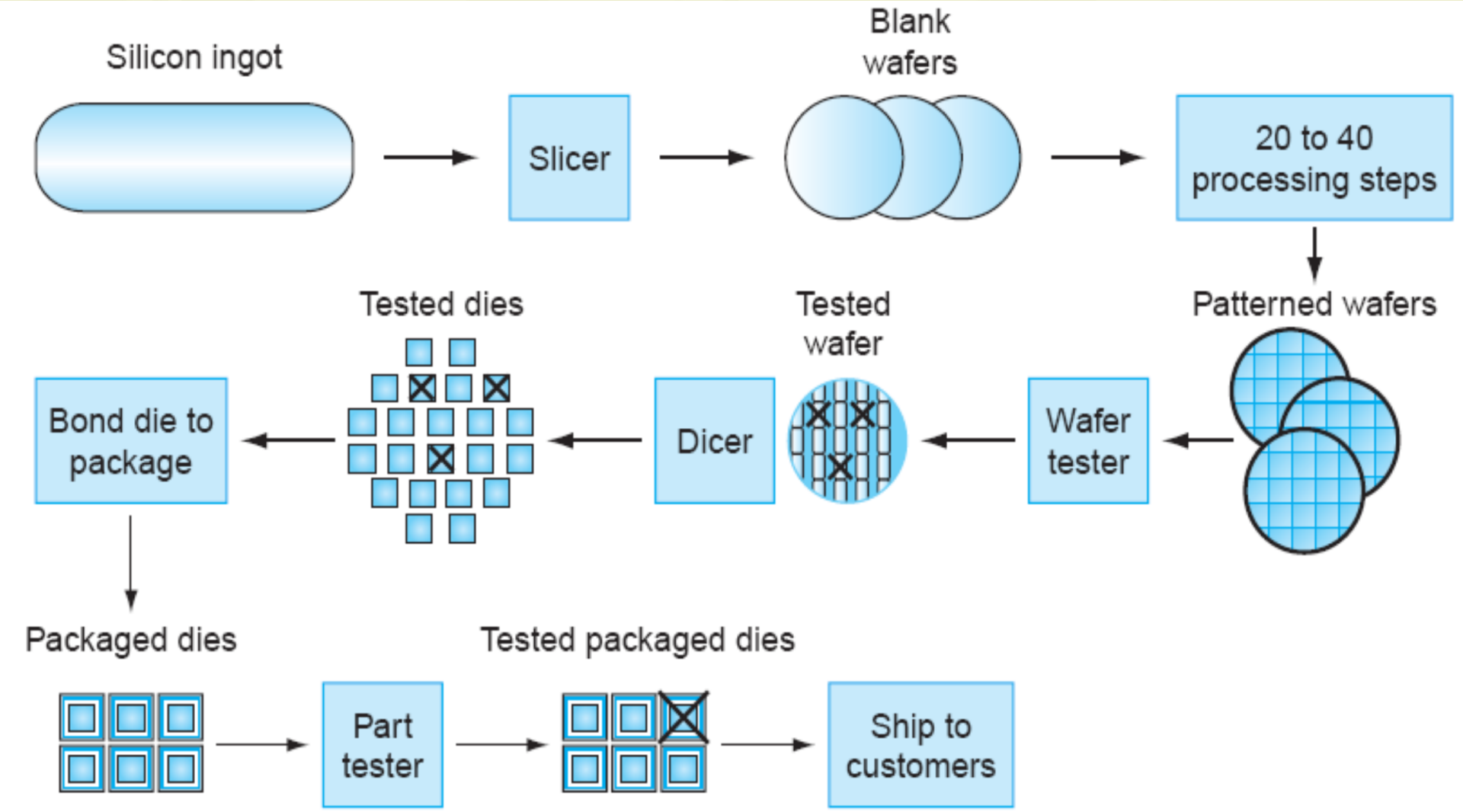
Suppression of off-current

Very small bandgap or no bandgap (semi-metal)

Control of ribbon edge structure which affects bandgap

Fig. 19. Long range roadmap for logic CMOS transistors for next 30 years.

IC MANUFACTURING

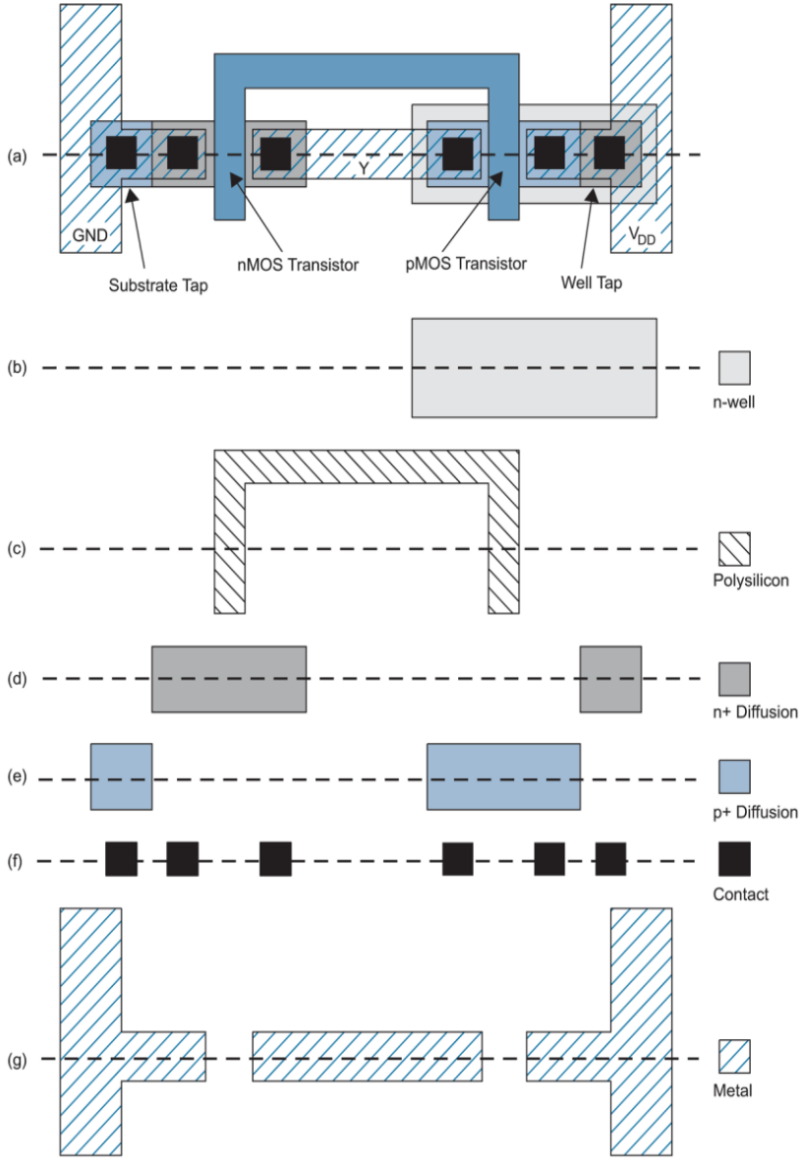


IC FABRICATION

- Chips are fabricated using set of masks
  - Photolithography

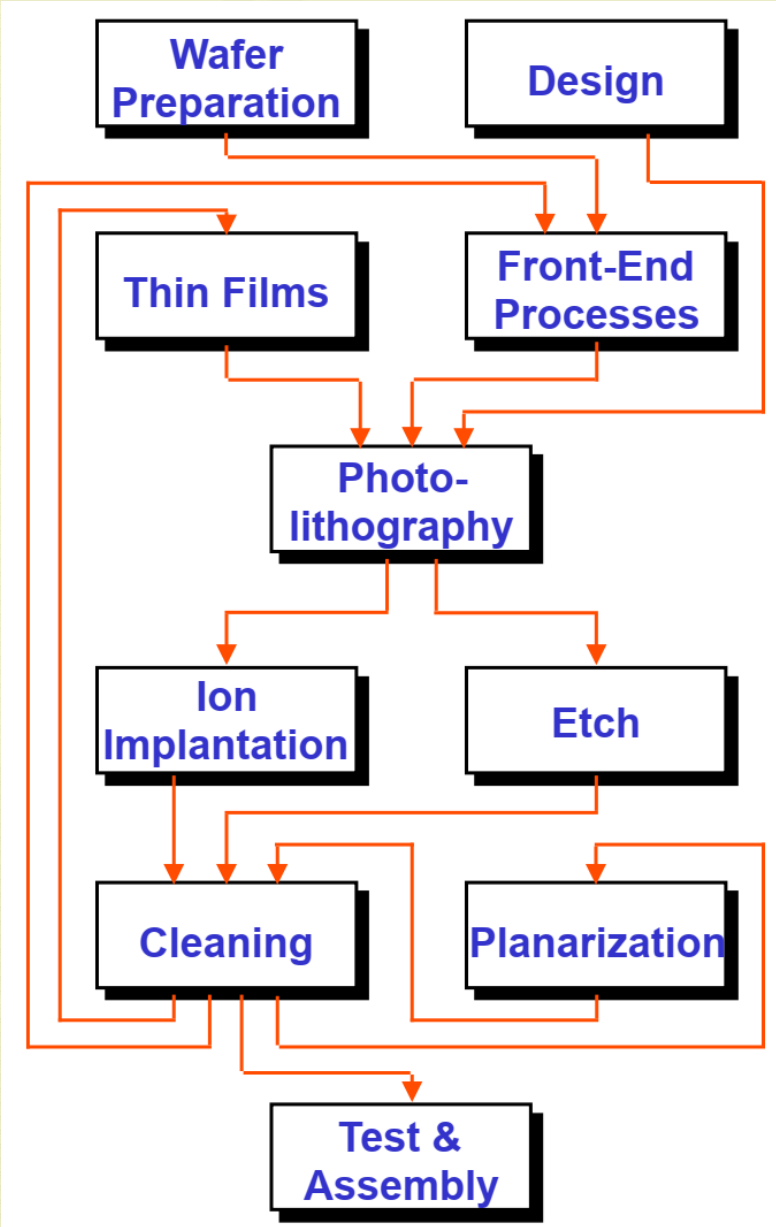
- Basic steps
  - oxidize
  - apply photoresist
  - remove photoresist with mask
  - HF acid eats oxide but not photoresist
  - pirana acid eats photoresist

  - ion implantation (diffusion, wells)
  - vapor deposition (poly)
  - plasma etching (metal)



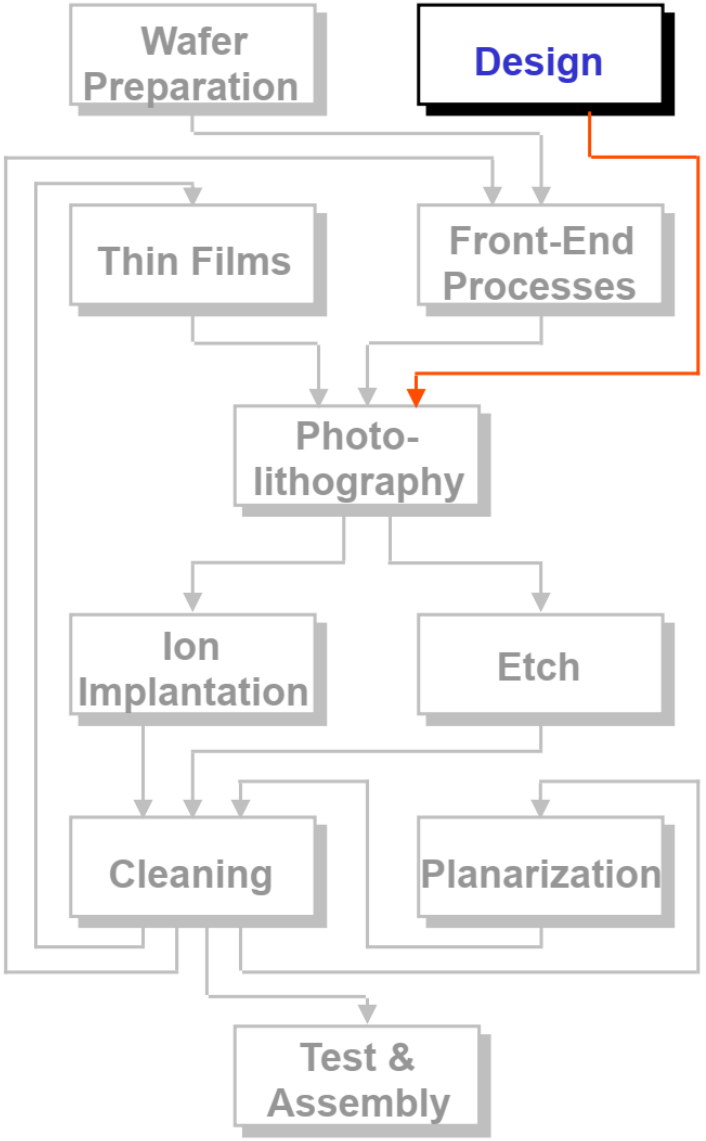
SEMICONDUCTOR MANUFACTURING PROCESSES

- Design
- Wafer Preparation
- Front-end Processes
- Photolithography
- Etch
- Cleaning
- Thin Films
- Ion Implantation
- Planarization
- Test and Assembly

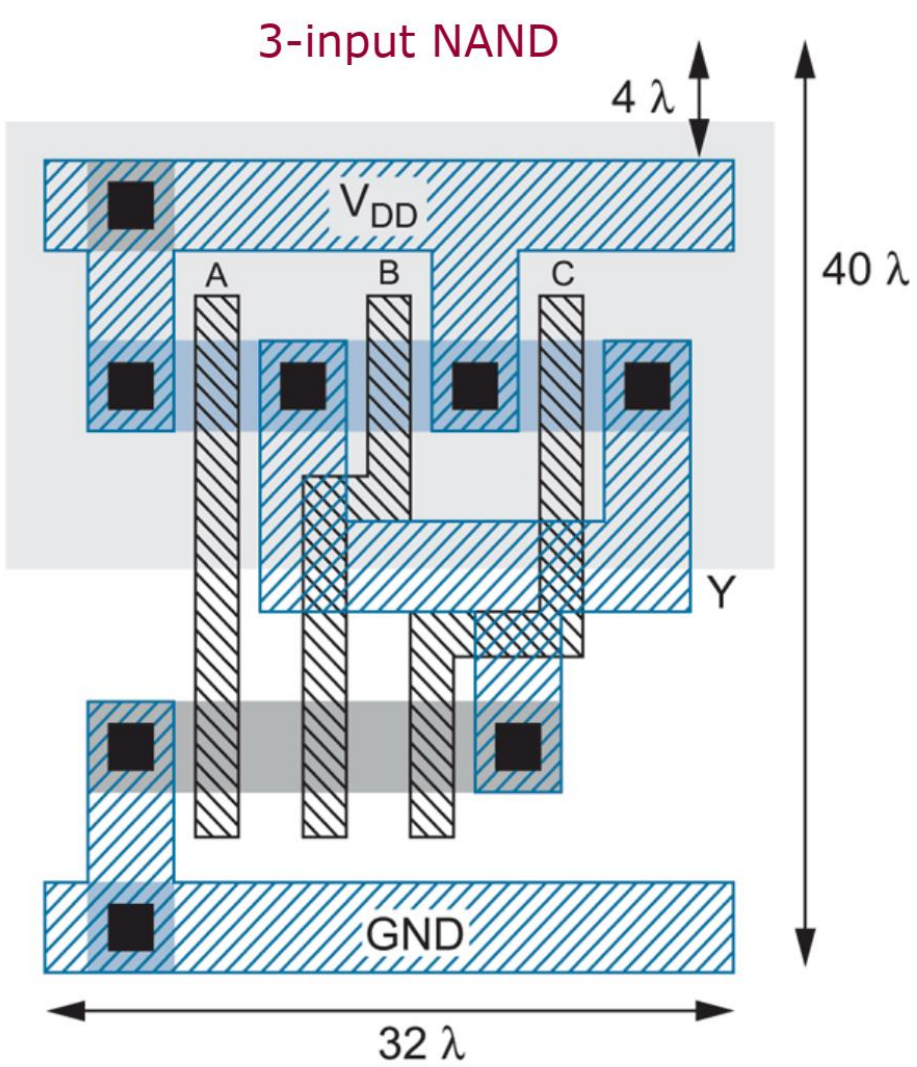


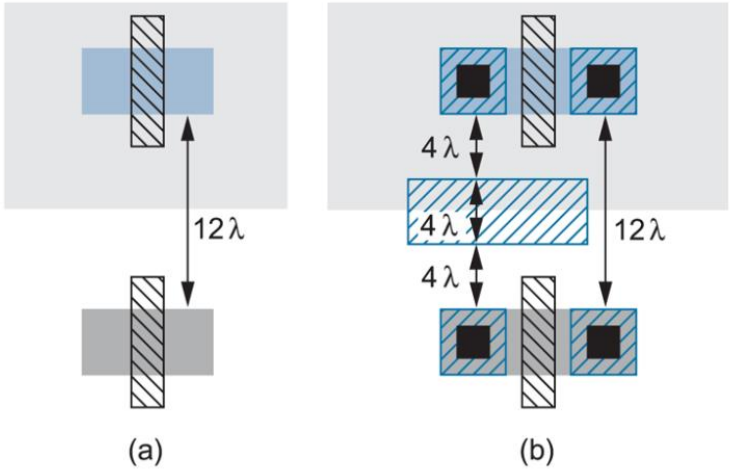
DESIGN

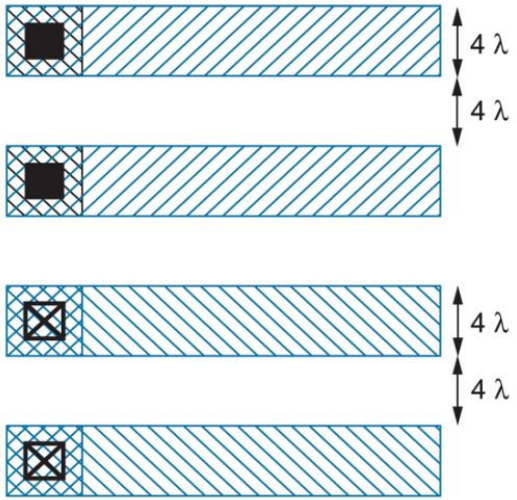
- Establish Design Rules
- Circuit Element Design
- Interconnect Routing
- Device Simulation
- Pattern Preparation



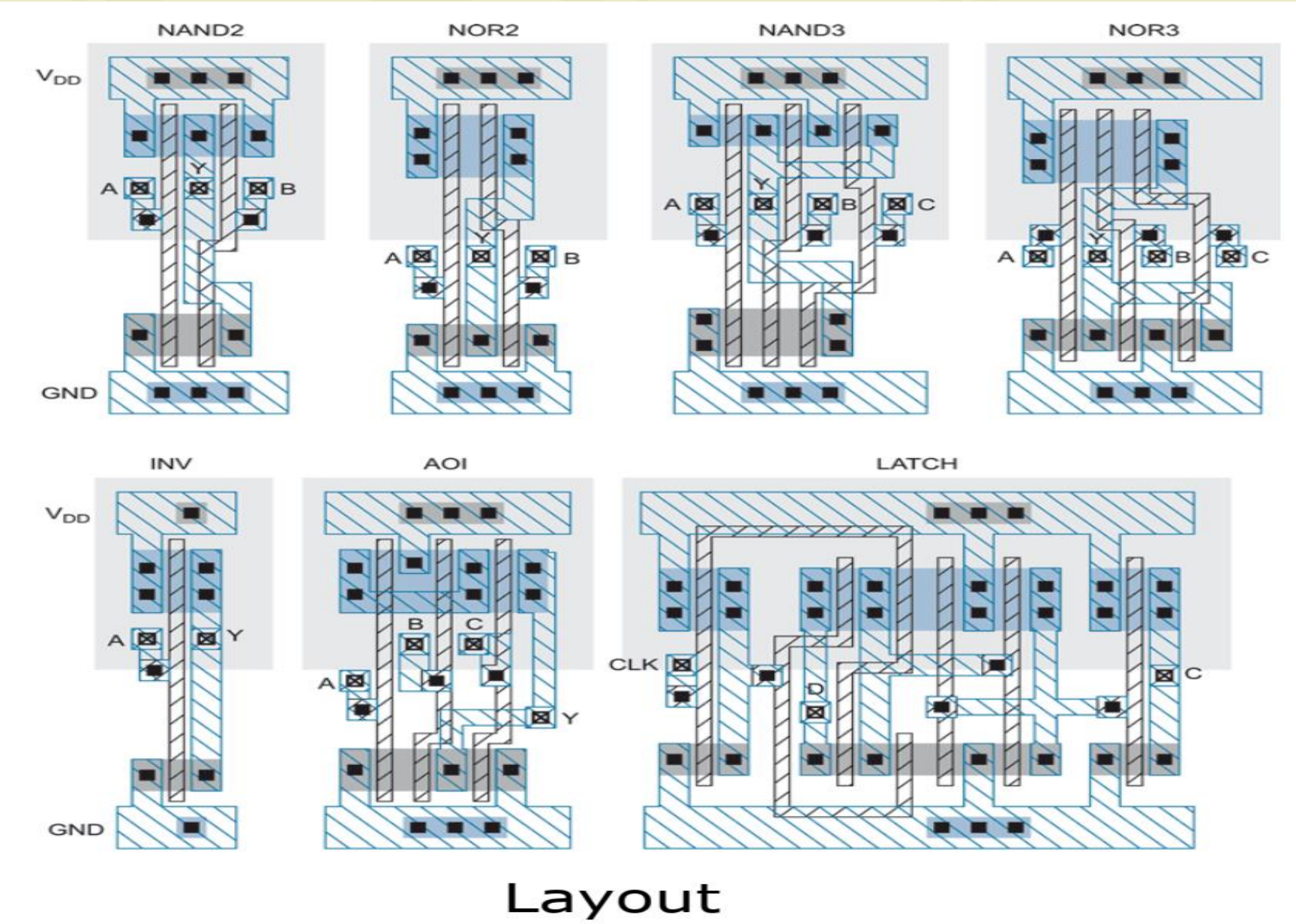
DESIGN - LAYOUT







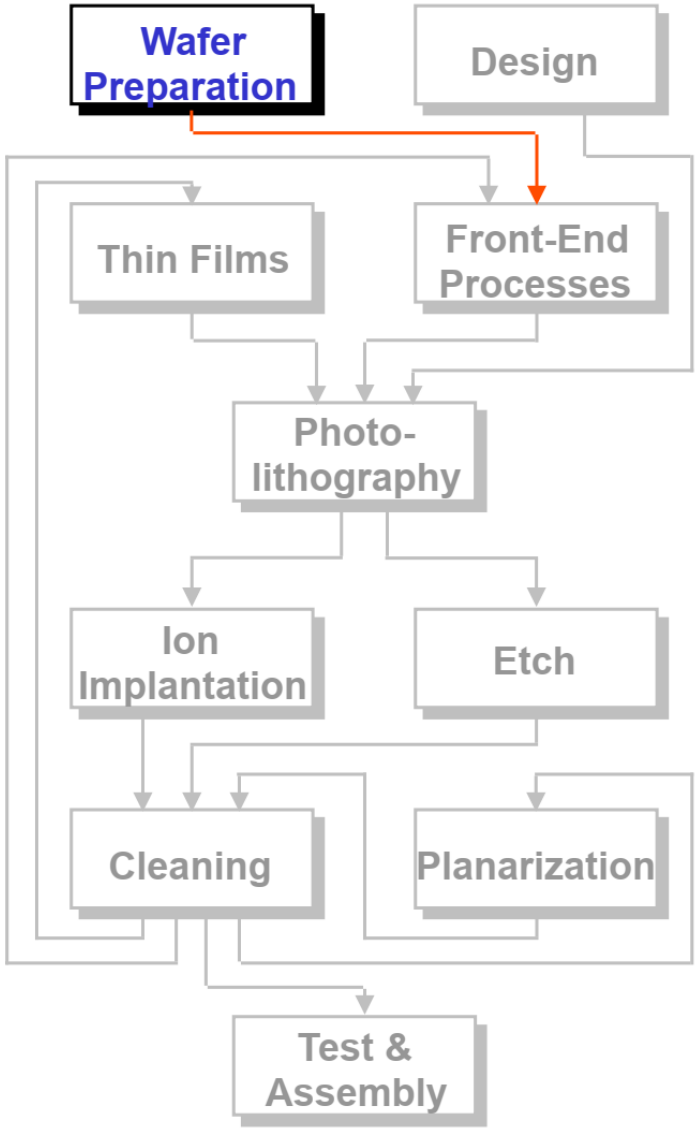
DESIGN – ELEMENT CELL LIBRARY



Layout

WAFER PREPARATION

- Polysilicon Refining
- Crystal Pulling
- Wafer Slicing & Polishing
- Epitaxial Silicon Deposition



WAFER PREPARATION – SAND/INGOT

Sand

With about 25% (mass) Silicon is – after Oxygen – the second most frequent chemical element in the earth's crust. Sand – especially Quartz - has high percentages of Silicon in the form of Silicon dioxide (SiO_2) and is the base ingredient for semiconductor manufacturing.

Melted Silicon –

scale: wafer level (~300mm / 12 inch)

Silicon is purified in multiple steps to finally reach semiconductor manufacturing quality which is called Electronic Grade Silicon. Electronic Grade Silicon may only have one alien atom every one billion Silicon atoms. In this picture you can see how one big crystal is grown from the purified silicon melt. The resulting mono crystal is called Ingot.

Mono-crystal Silicon Ingot –

scale: wafer level (~300mm / 12 inch)

An ingot has been produced from Electronic Grade Silicon. One ingot weights about 100 kilograms (=220 pounds) and has a Silicon purity of 99.9999%.

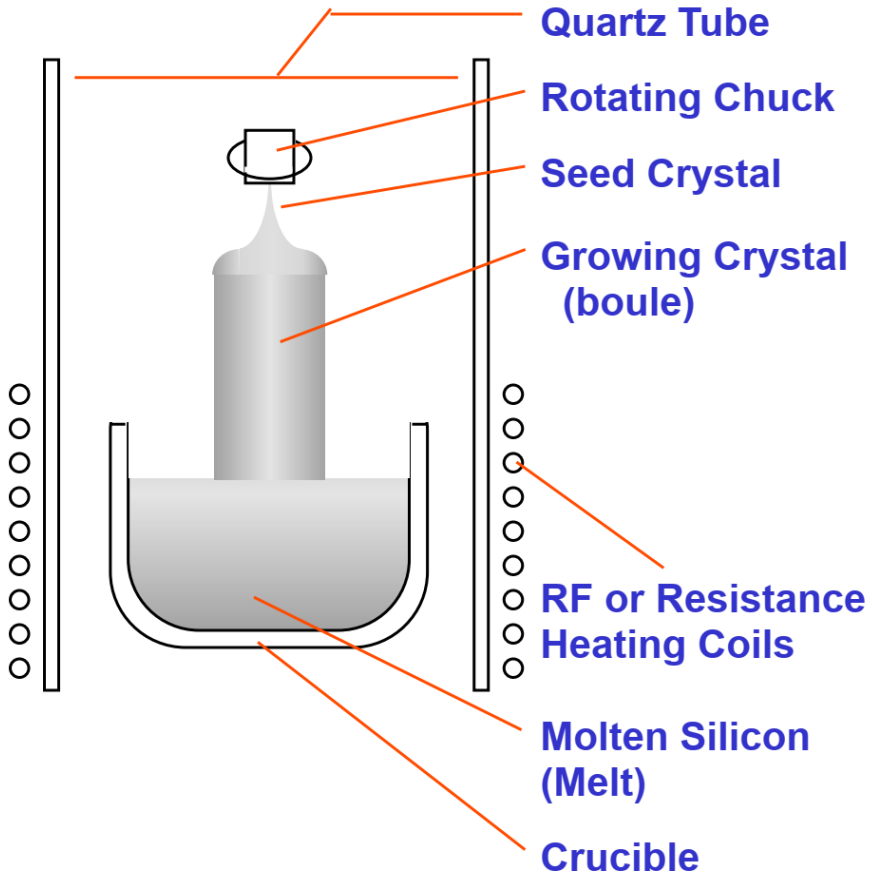
WAFER PREPARATION – CRYSTAL PULLING

Process Conditions

Flow Rate: 20 to 50 liters/min
Time: 18 to 24 hours
Temperature: >1,300 degrees C
Pressure: 20 Torr

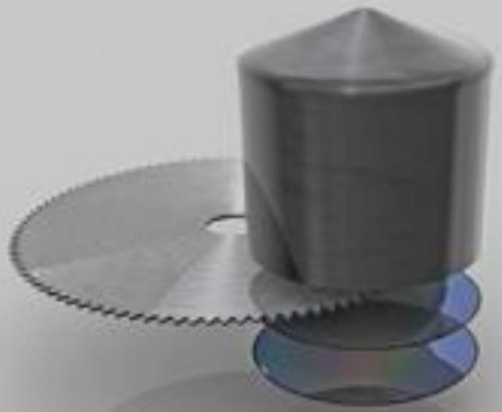
Materials

Polysilicon Nodules *
Ar *
H_2



* High proportion of the total product use

WAFER PREPARATION –INGOT/WAFER



Ingot Slicing –

scale: wafer level (~300mm / 12 inch)

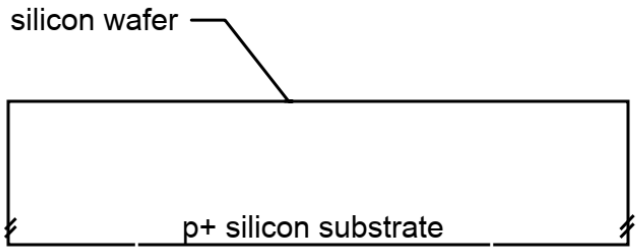
The Ingot is cut into individual silicon discs called wafers.

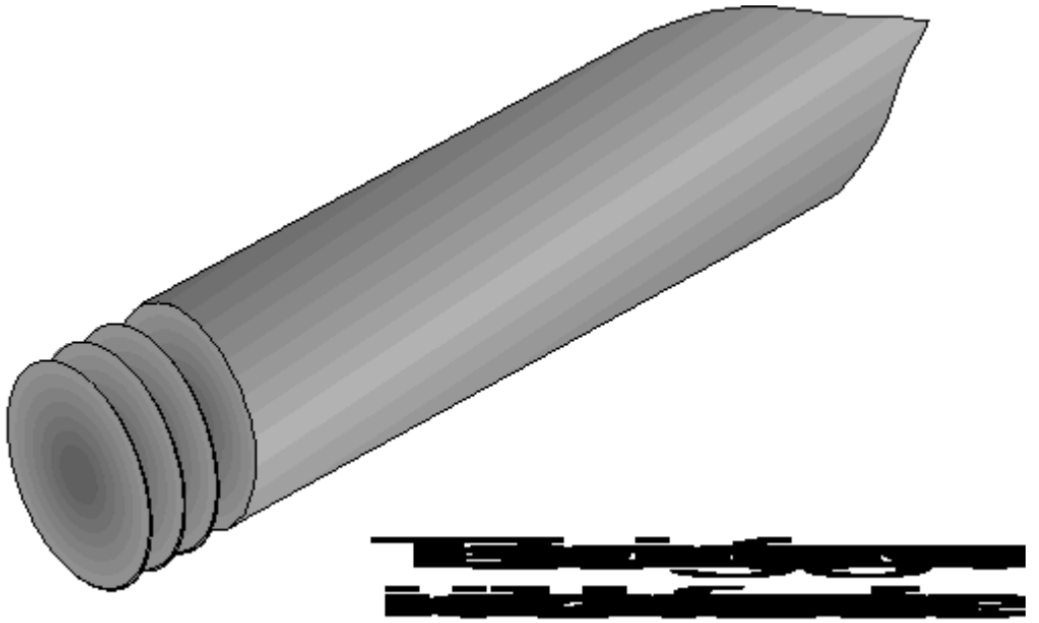
Wafer –

scale: wafer level (~300mm / *12 inch*)

The wafers are polished until they have flawless, mirror-smooth surfaces. Intel buys those manufacturing ready wafers from third party companies. Intel's highly advanced 45nm High-K/Metal Gate process uses wafers with a diameter of 300 millimeter (~12 inches). When Intel first began making chips, the company printed circuits on 2-inch (50mm) wafers. Now the company uses 300mm wafers, resulting in decreased costs per chip.

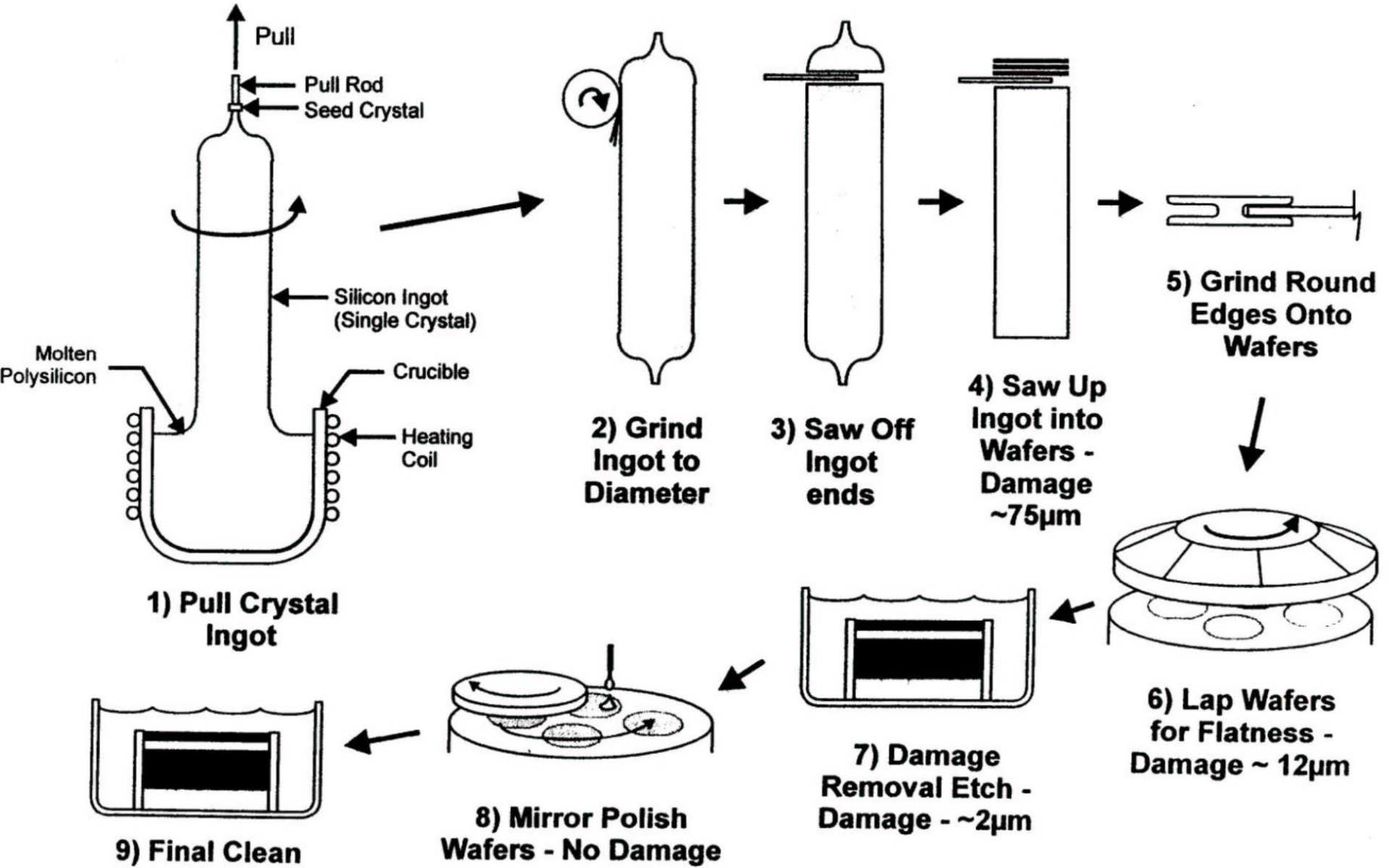
WAFER PREPARATION – Wafer Slicing & Polishing





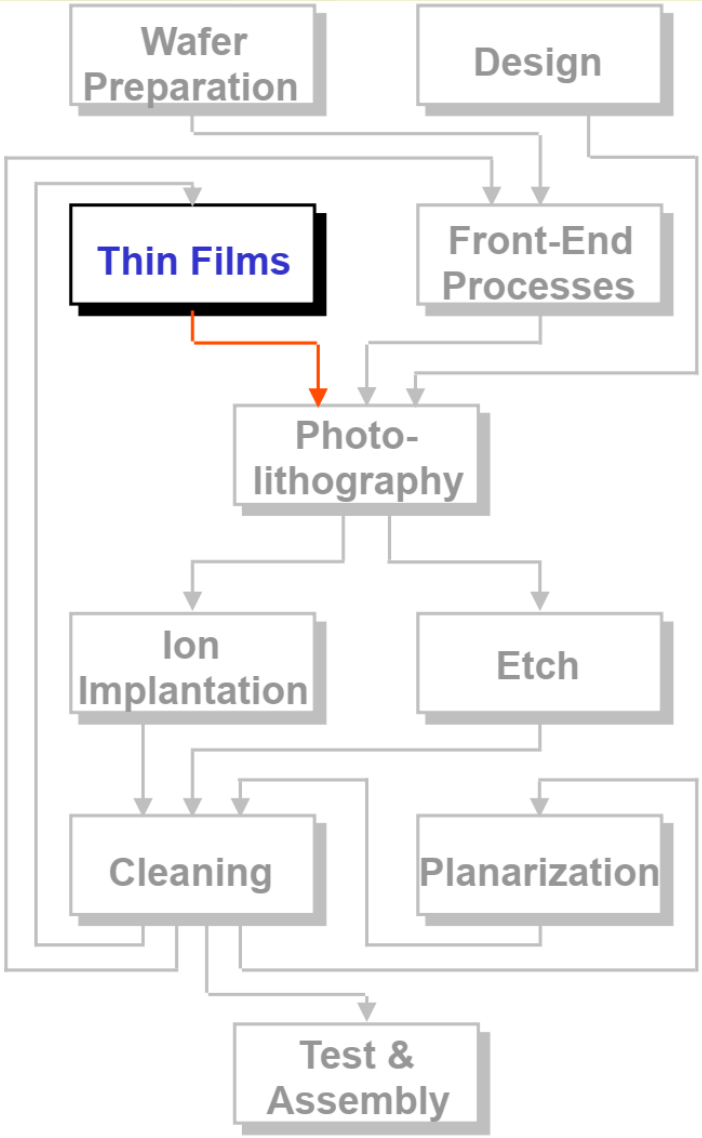
The silicon ingot is sliced into individual wafers, polished, and cleaned.

WAFER PREPARATION – Wafer Manufacturing Process Overview



THIN FILMS

- Chemical Vapor Deposition (CVD) Dielectric
- CVD Tungsten
- Physical Vapor Deposition (PVD)
- Chamber Cleaning



THIN FILMS - CVD

- Chemical Vapor Deposition (CVD) thermally reacts gases to deposit films.
- CVD can be performed over a variety of temperatures from around 400°C on the low end to over 1,200°C on the high end.
- CVD films can be deposited over a variety of different material layers.
- Compared to oxidation, CVD films can be deposited at lower temperatures, can be deposited over material layers other than silicon and do not consume any of the underlying substrate material the way oxidation does.
- CVD can deposit a wide variety of Insulating, Conducting and Semiconducting films.

THIN FILMS – CVD DIELECTRIC

Chemical Reactions

$Si(OC_2H_5)_4 + 9\ O_3 \rightarrow SiO_2 + 5\ CO + 3\ CO_2 + 10\ H_2O$

Process Conditions (ILD)

Flow Rate: 100 to 300 sccm

Pressure: 50 Torr to Atmospheric

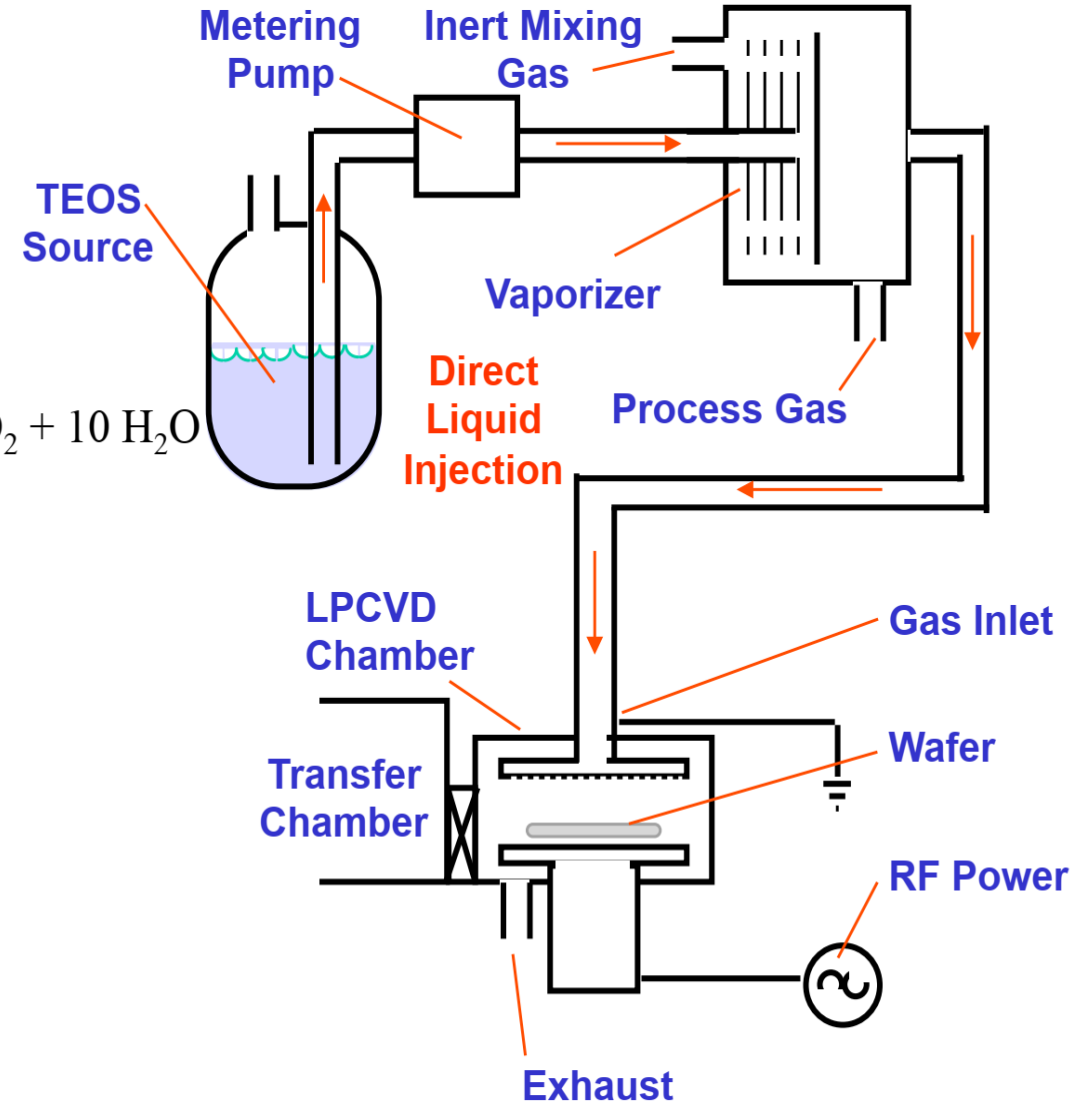
CVD Dielectric

O_2

O_3

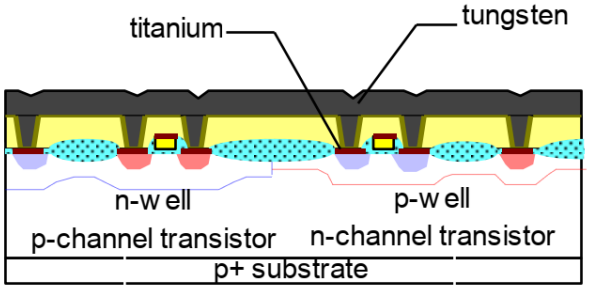
TEOS *

TMP *



* High proportion of the total product use

THIN FILMS – CVD TUNGSTEN



Chemical Reactions

$WF_6 + 3\ H_2 \rightarrow W + 6\ HF$

Process Conditions

Flow Rate: 100 to 300 sccm

Pressure: 100 mTorr

Temperature: 400 degrees C.

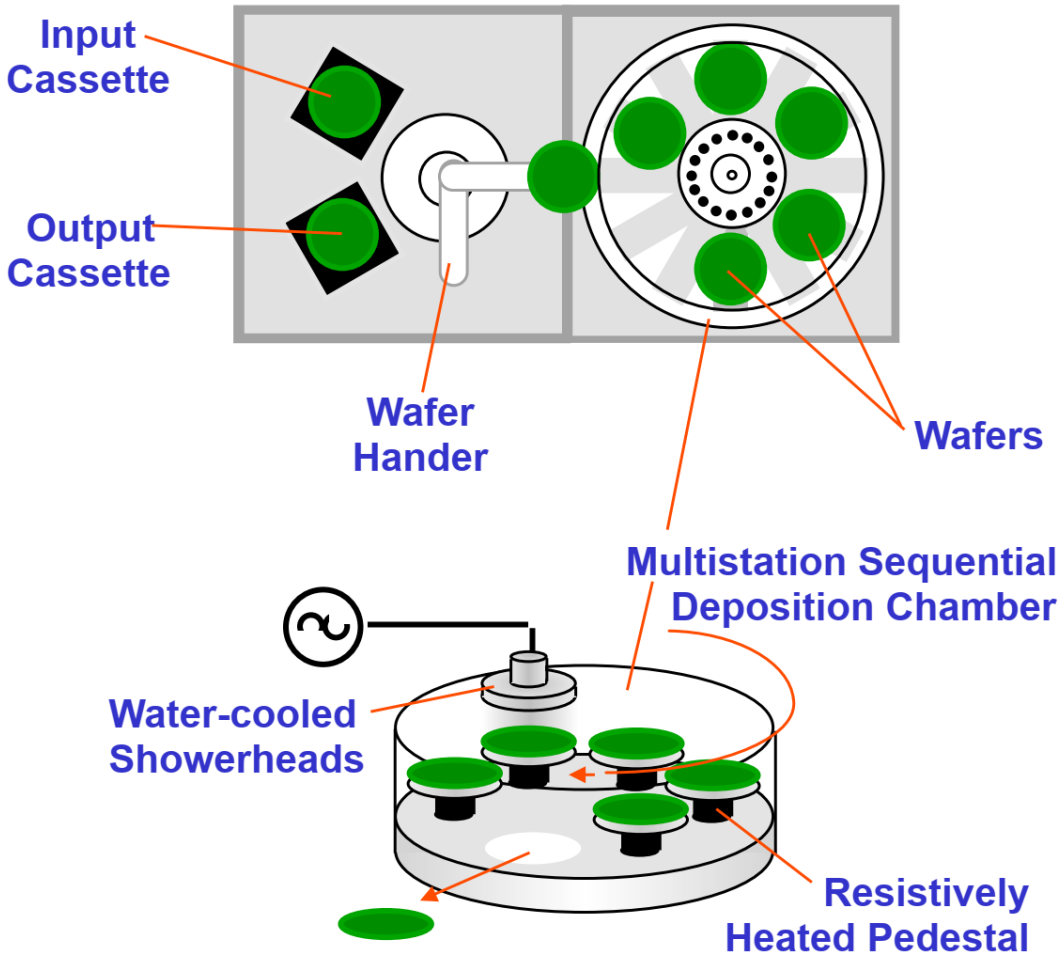
CVD Dielectric

WF_6 *

Ar

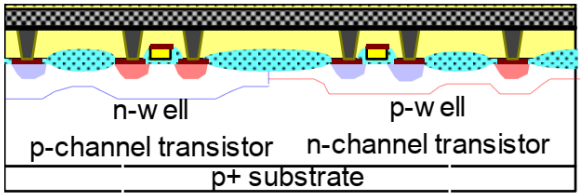
H_2

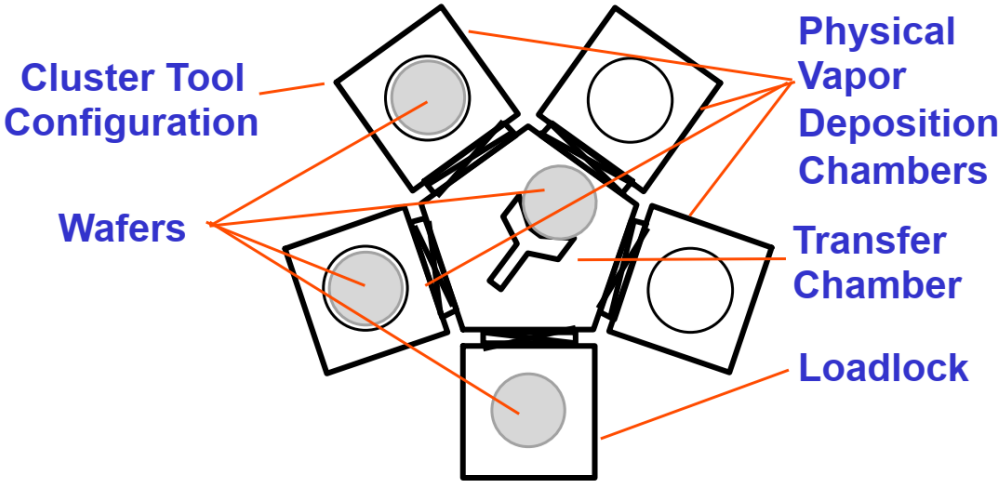
N_2



* High proportion of the total product use

THIN FILMS – PVD





Process Conditions

Pressure: < 5 mTorr

Temperature: 200 degrees C.

RF Power:

Barrier Metals

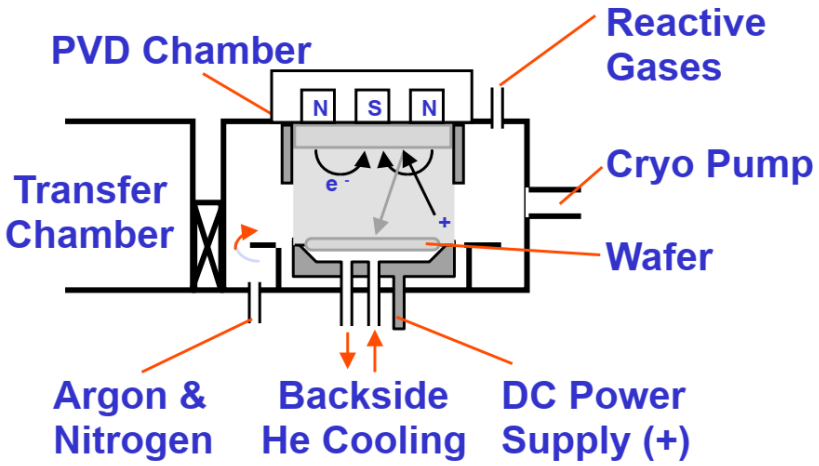
SiH_4

Ar

N_2

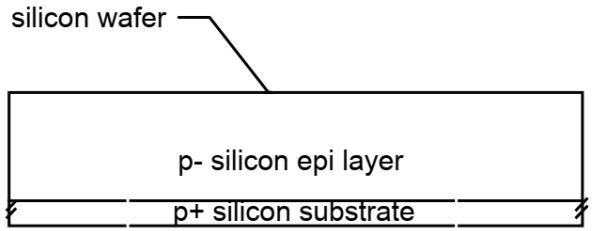
N_2

Ti PVD Targets *



* High proportion of the total product use

THIN FILMS – EPITAXIAL SILICON DEPOSITION



Chemical Reactions

Silicon Deposition: $HSiCl_3 + H_2 \rightarrow Si + 3\ HCl$

Process Conditions

Flow Rates: 5 to 50 liters/min

Temperature: 900 to 1,100 degrees C.

Pressure: 100 Torr to Atmospheric

Silicon Sources

SiH_4

H_2SiCl_2

$HSiCl_3$ *

$SiCl_4$ *

Dopants

AsH_3

B_2H_6

PH_3

Etchant

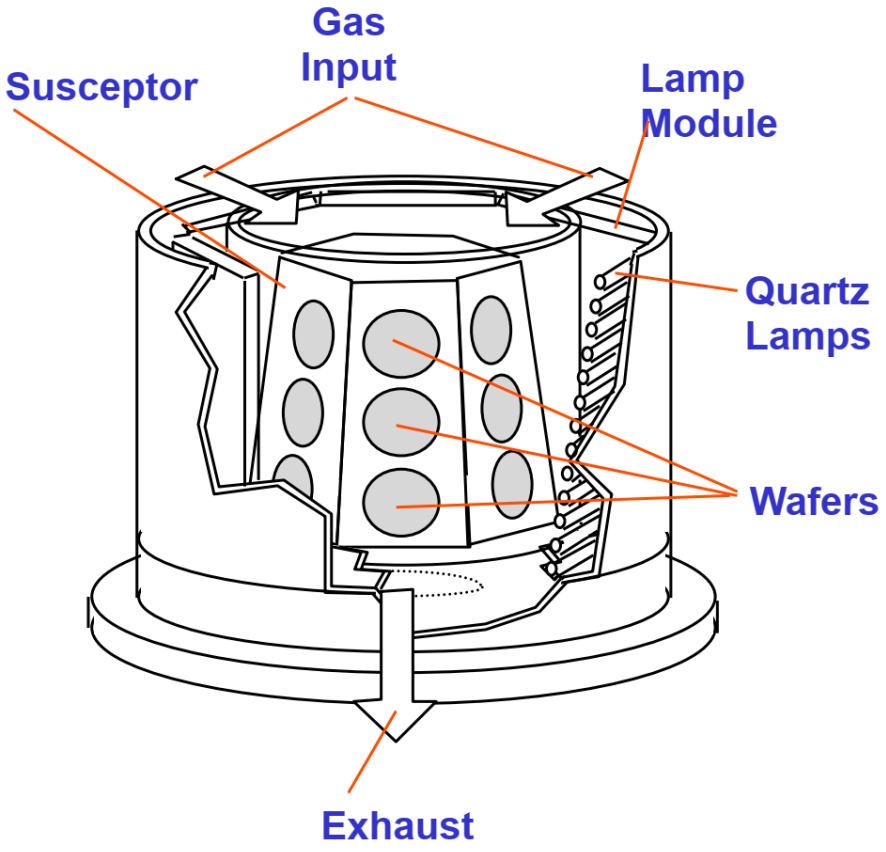
HCl

Carriers

Ar

H_2 *

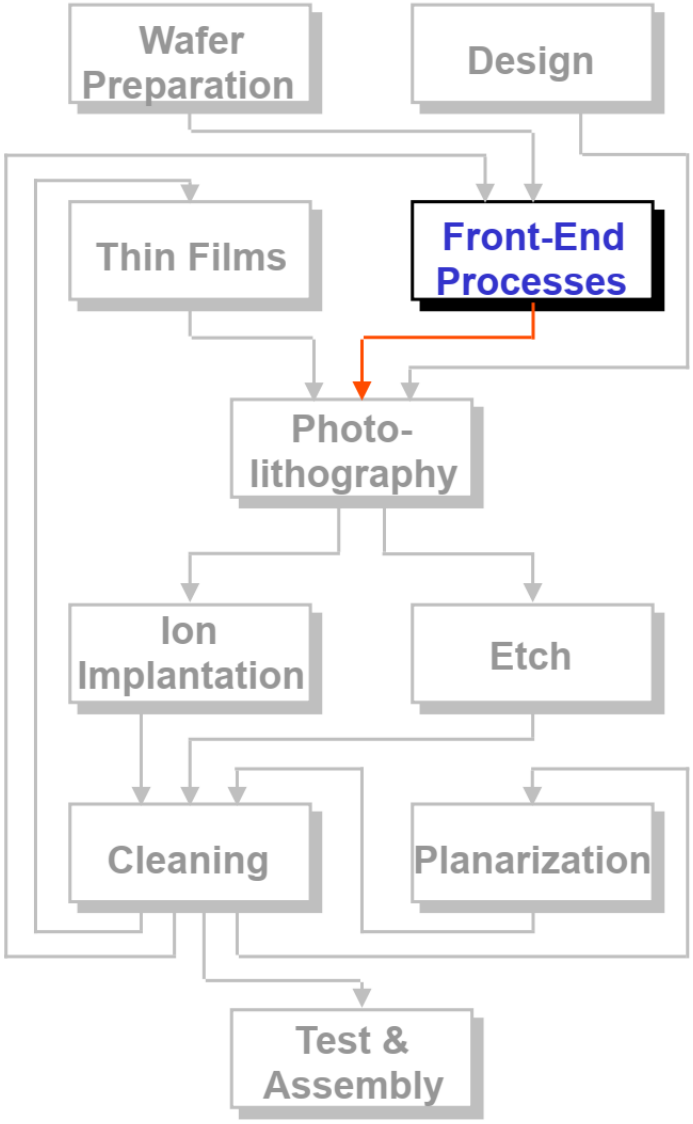
N_2



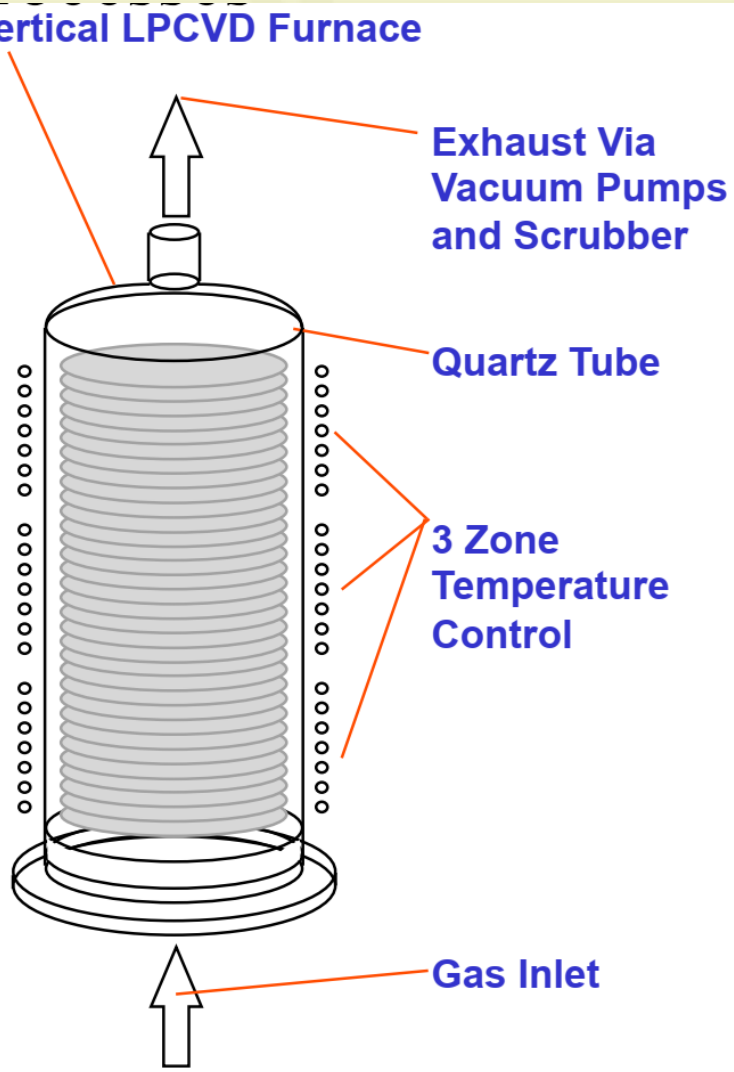
* High proportion of the total product use

FRONT-END PROCESSES

- Thermal Oxidation
- Silicon Nitride Deposition
  - Low Pressure Chemical Vapor Deposition (LPCVD)
- Polysilicon Deposition
  - Low Pressure Chemical Vapor Deposition (LPCVD)
- Annealing



FRONT-END PROCESSES



Chemical Reactions

Thermal Oxidation: $Si + O_2 \rightarrow SiO_2$

Nitride Deposition: $3\ SiH_4 + 4\ NH_3 \rightarrow Si_3N_4 + 12\ H_2$

Polysilicon Deposition: $SiH_4 \rightarrow Si + 2\ H_2$

Process Conditions (Silicon Nitride LPCVD)

Flow Rates: 10 - 300 sccm

Temperature: 600 degrees C.

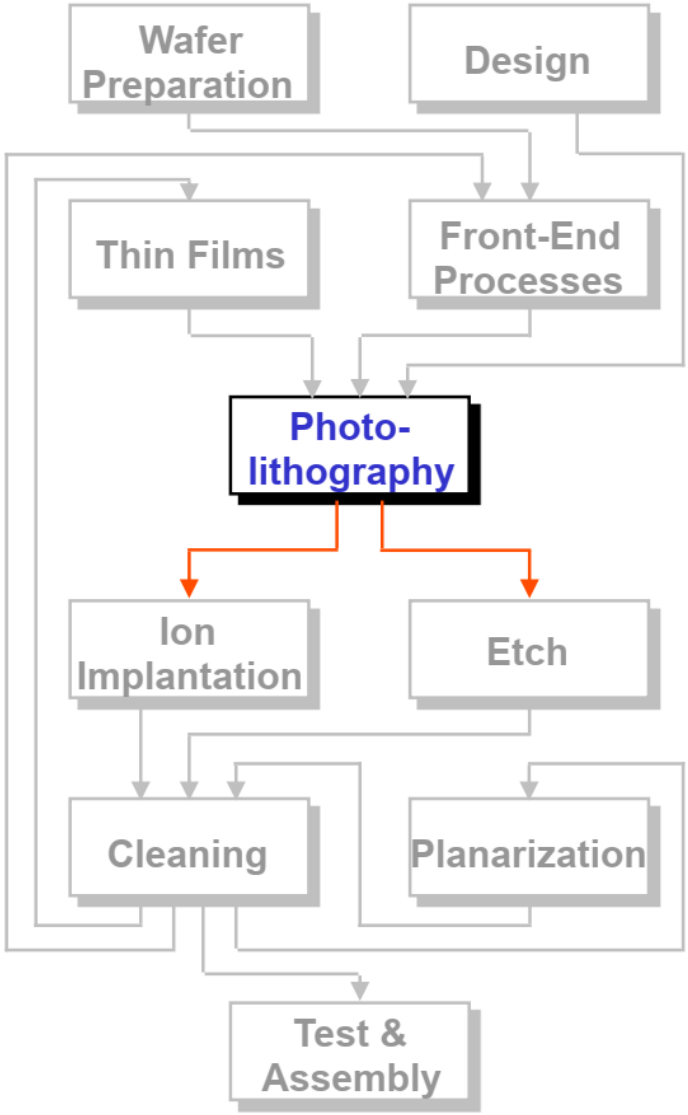
Pressure: 100 mTorr

Oxidation	Polysilicon	Nitride	Annealing
Ar	H_2	NH_3 *	Ar
N_2	N_2	H_2SiCl_2 *	He
H_2O	SiH_4 *	N_2	H_2
Cl_2	AsH_3	SiH_4 *	N_2
H_2	B_2H_6	$SiCl_4$	
HCl *	PH_3		
O_2 *			
Dichloroethene *			

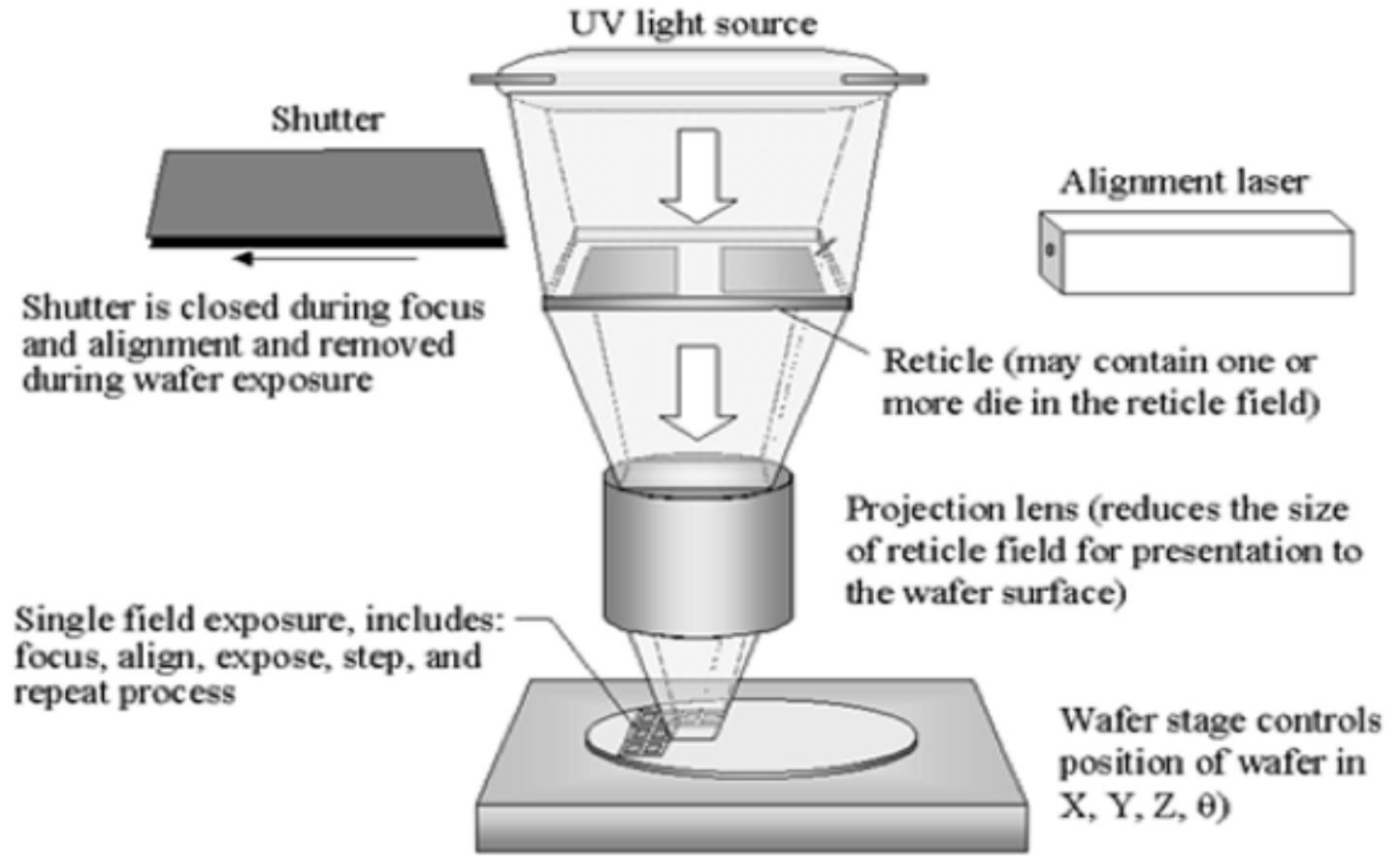
* High proportion of the total product use

PHOTOLITHOGRAPHY

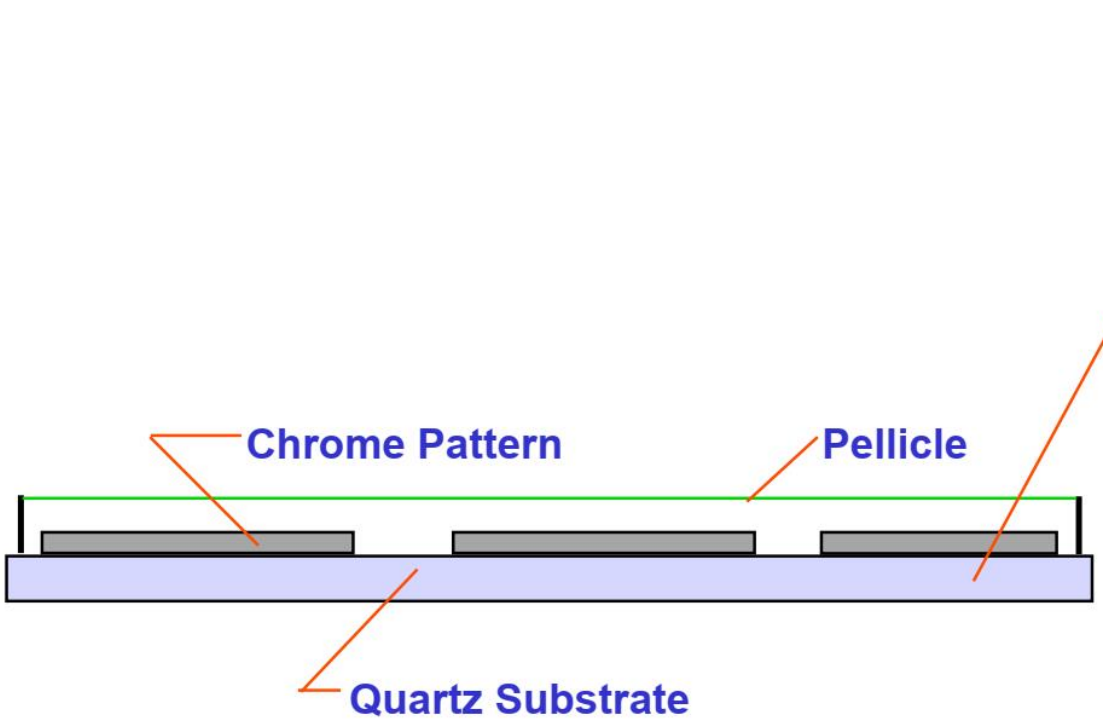
- Photoresist Coating Processes
- Exposure Processes

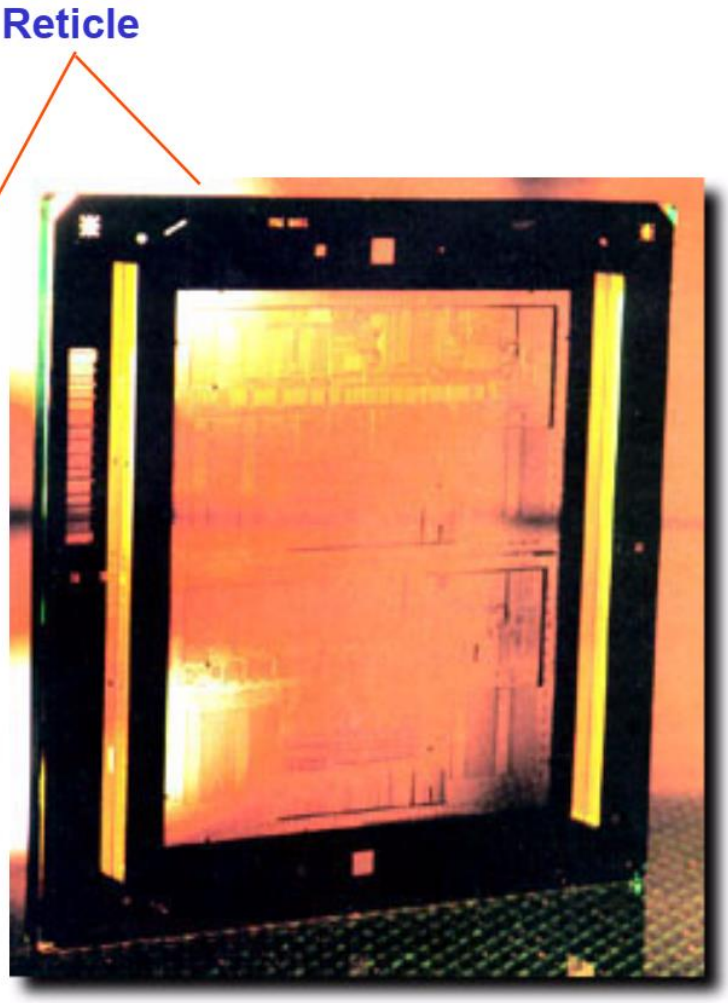


PHOTOLITHOGRAPHY – ALIGNMENT & EXPOSURE

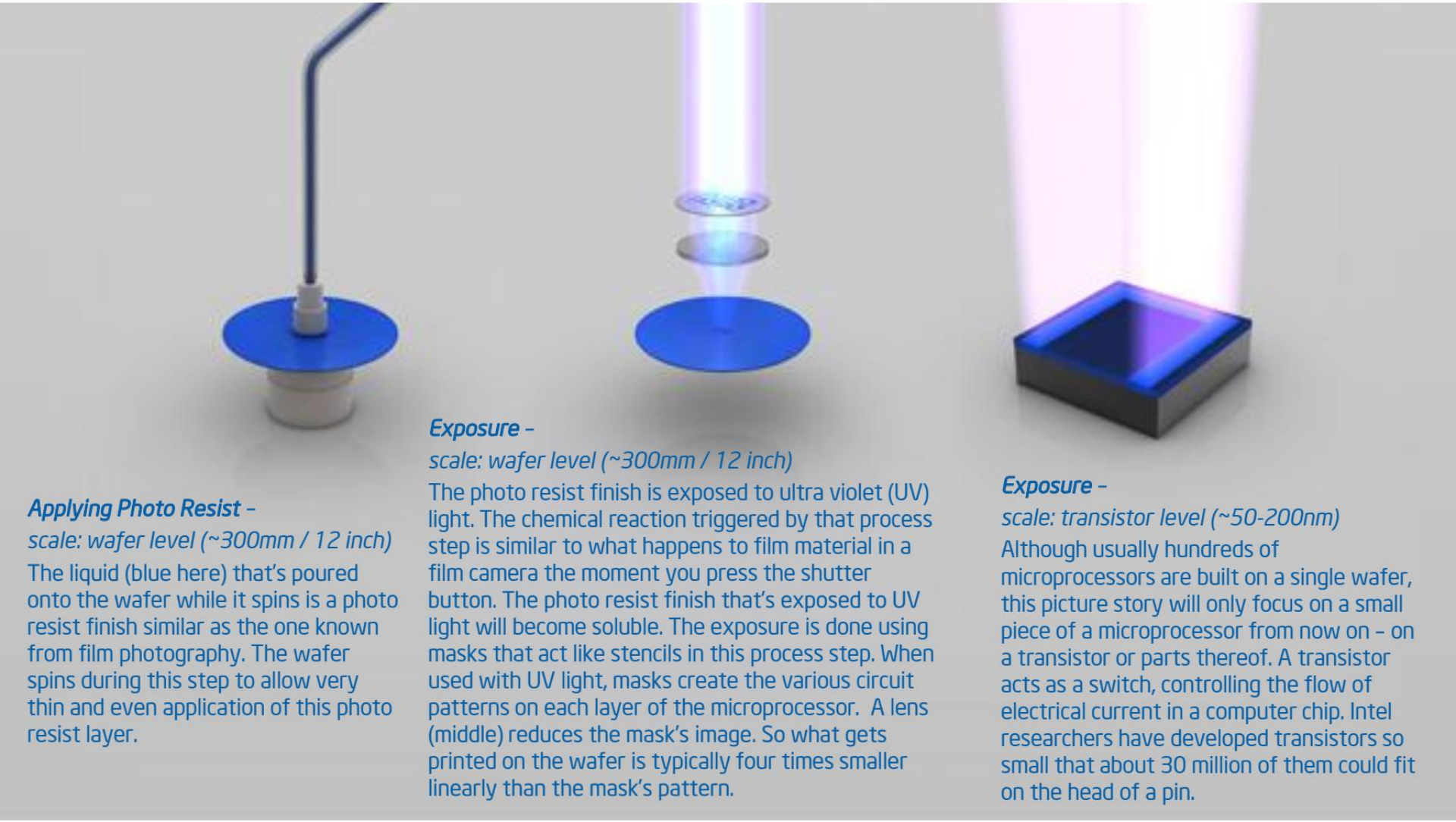


PHOTOLITHOGRAPHY – Lithography
Pattern Preparation





PHOTOLITHOGRAPHY



Applying Photo Resist –

scale: wafer level (~300mm / 12 inch)

The liquid (blue here) that's poured onto the wafer while it spins is a photo resist finish similar as the one known from film photography. The wafer spins during this step to allow very thin and even application of this photo resist layer.

Exposure –

scale: wafer level (~300mm / 12 inch)

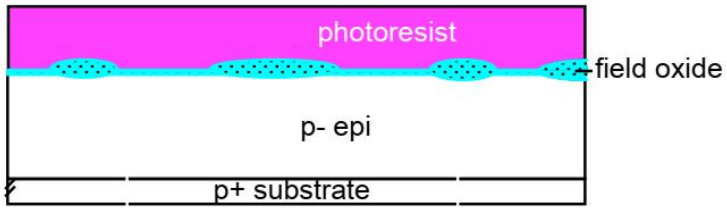
The photo resist finish is exposed to ultra violet (UV) light. The chemical reaction triggered by that process step is similar to what happens to film material in a film camera the moment you press the shutter button. The photo resist finish that's exposed to UV light will become soluble. The exposure is done using masks that act like stencils in this process step. When used with UV light, masks create the various circuit patterns on each layer of the microprocessor. A lens (middle) reduces the mask's image. So what gets printed on the wafer is typically four times smaller linearly than the mask's pattern.

Exposure –

scale: transistor level (~50-200nm)

Although usually hundreds of microprocessors are built on a single wafer, this picture story will only focus on a small piece of a microprocessor from now on – on a transistor or parts thereof. A transistor acts as a switch, controlling the flow of electrical current in a computer chip. Intel researchers have developed transistors so small that about 30 million of them could fit on the head of a pin.

PHOTOLITHOGRAPHY - Photoresist Coating Processes

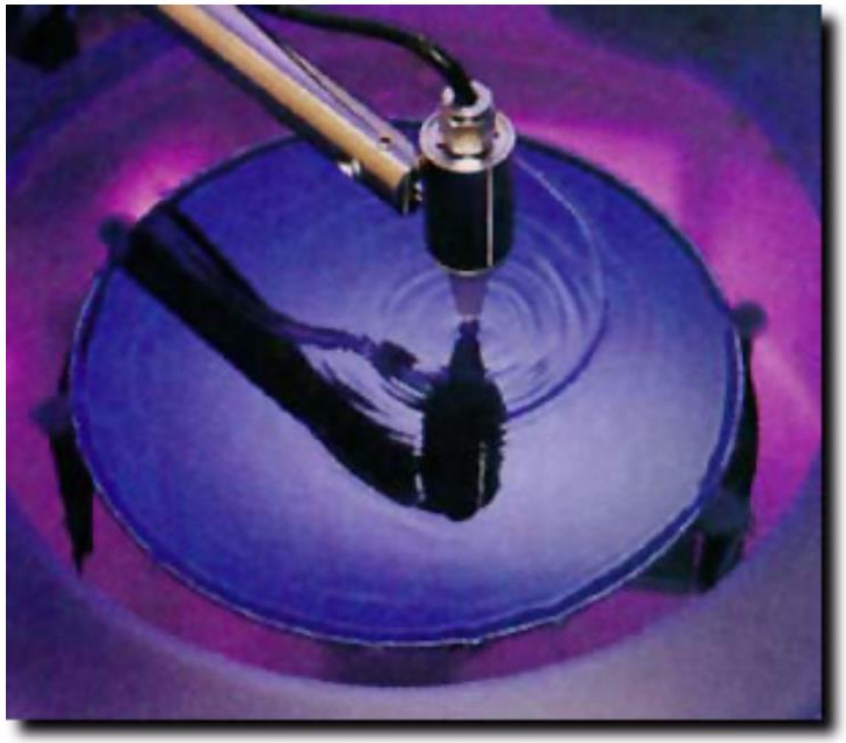


Photoresists
- Negative Photoresist *
- Positive Photoresist *

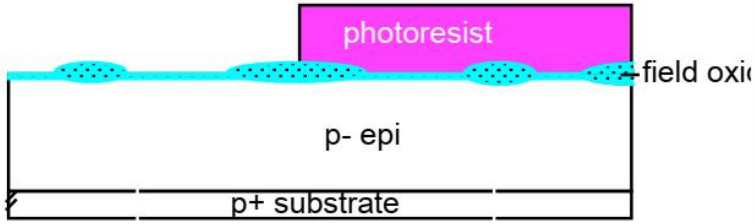
Other Ancillary Materials (Liquids)
- Edge Bead Removers *
- Anti-Reflective Coatings *
- Adhesion Promoters/Primers (HMDS) *
- Rinsers/Thinners/Corrosion Inhibitors *
- Contrast Enhancement Materials *

Developers
- TMAH *
- Specialty Developers *

Inert Gases
- Ar
- N_2



PHOTOLITHOGRAPHY – EXPOSURE PROCESSES

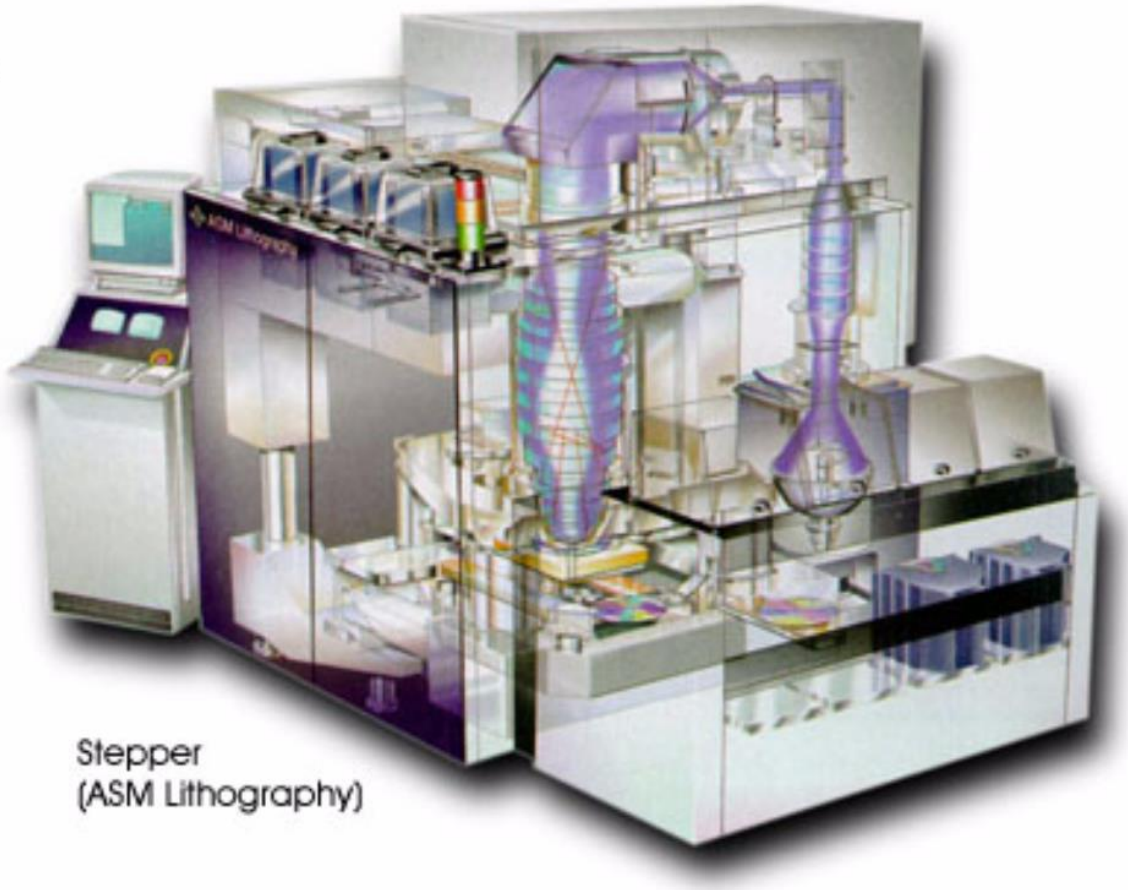


Expose

$Kr + F_2$ (gas) *

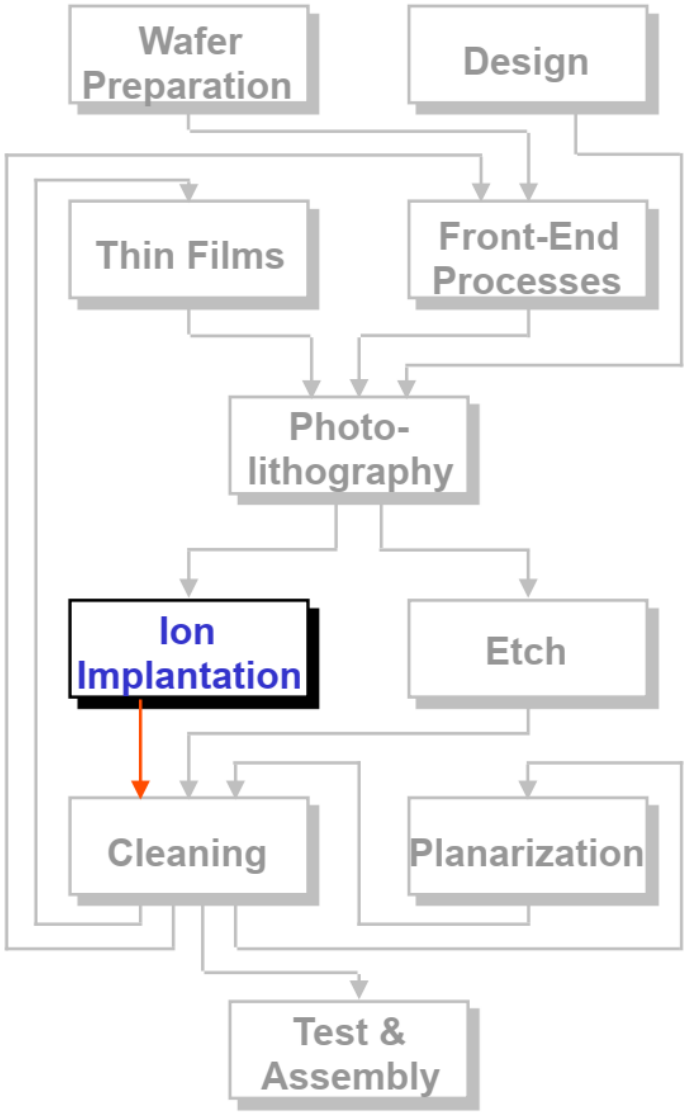
Inert Gases

N_2

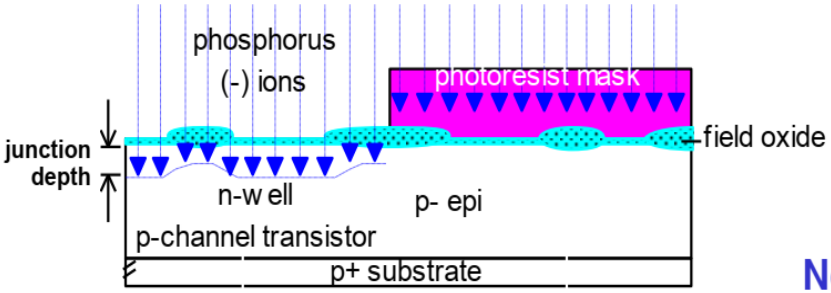


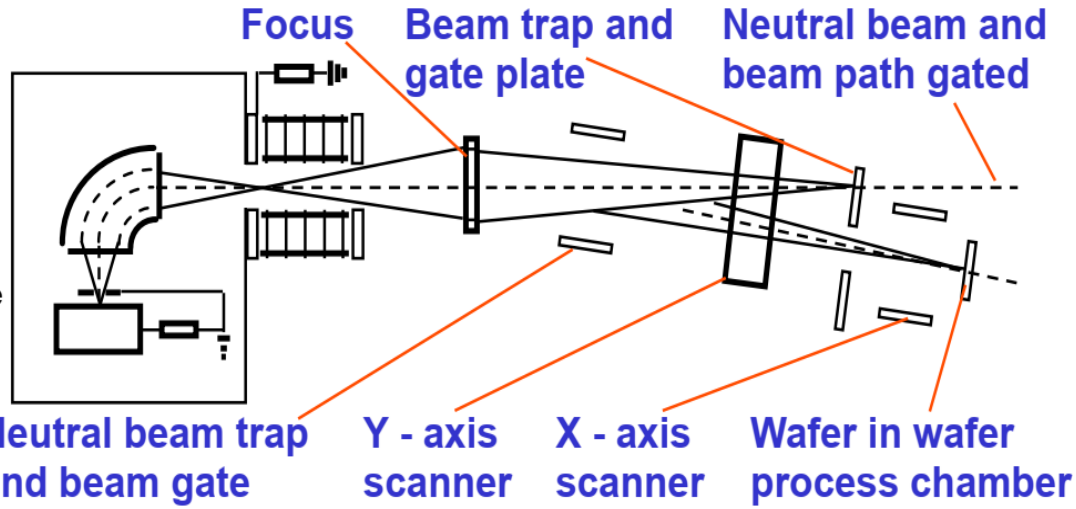
ION IMPLANTATION

- Well Implants
- Channel Implants
- Source/Drain Implants



Ion Implantation





Process Conditions

Flow Rate: 5 sccm

Pressure: 10^{-5} Torr

Accelerating Voltage: 5 to 200 keV

Gases

Ar

AsH_3

$B^{11}F_3$ *

He

N_2

PH_3

SiH_4

SiF_4

GeH_4

Solids

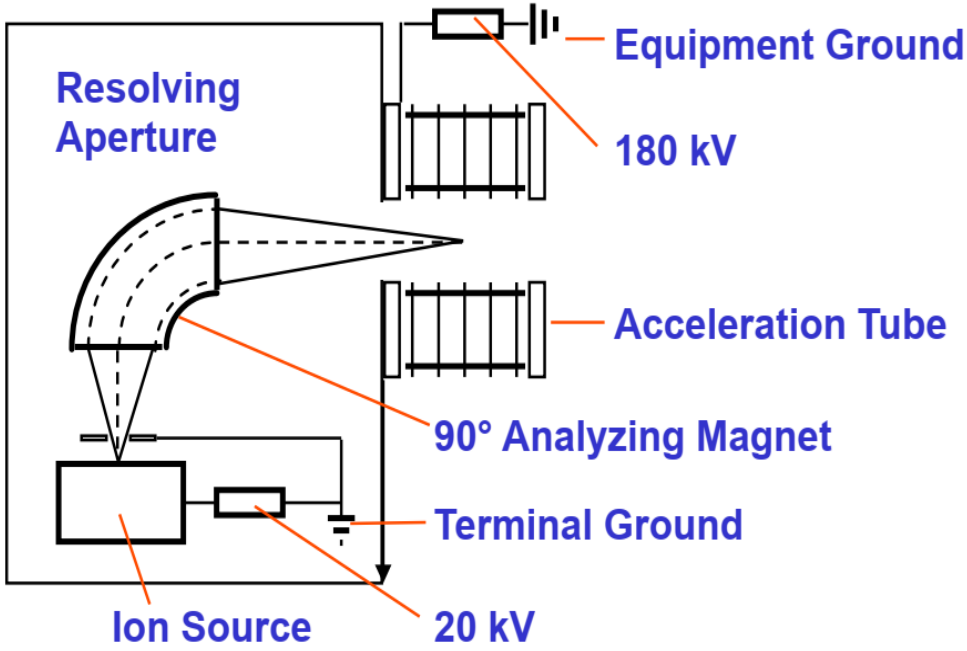
Ga

In

Sb

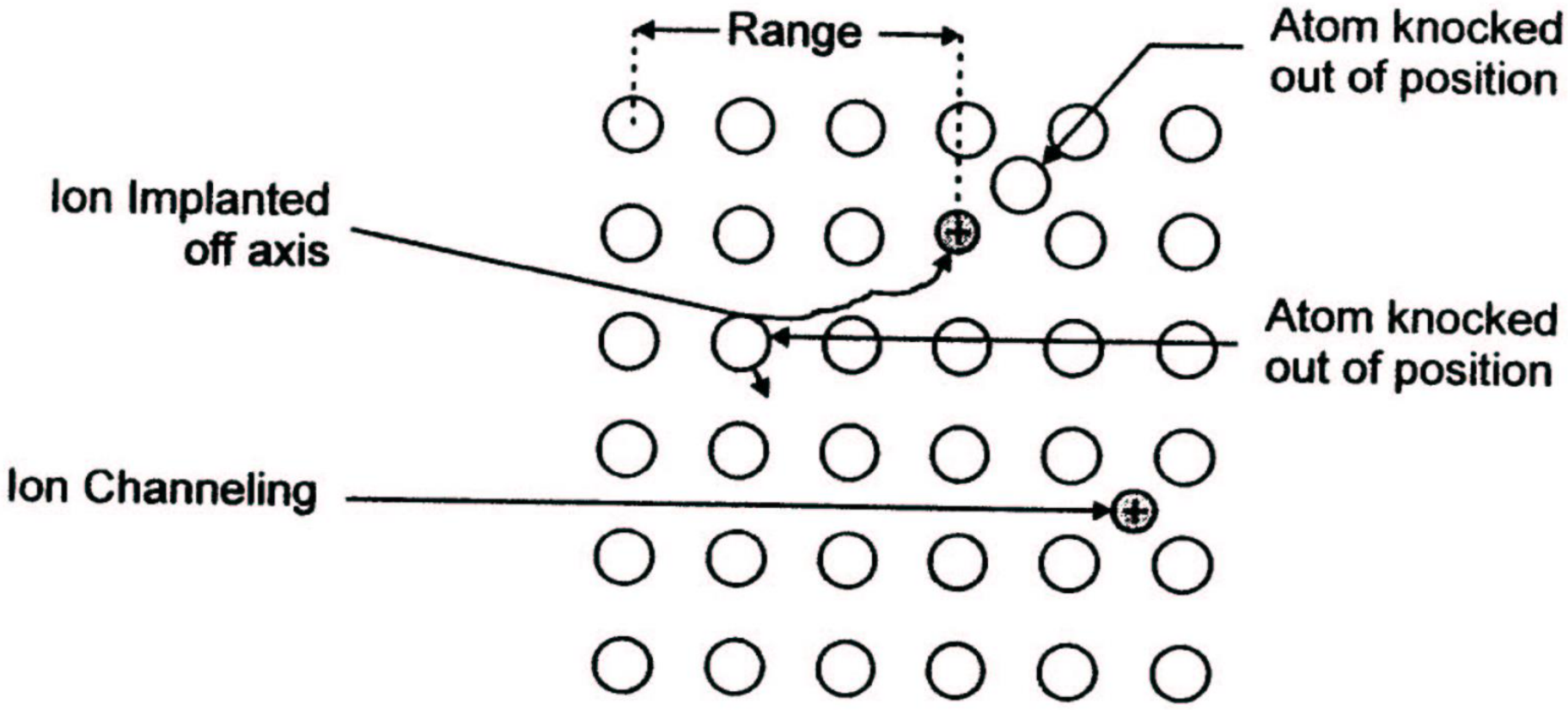
Liquids

$Al(CH_3)_3$



* High proportion of the total product use

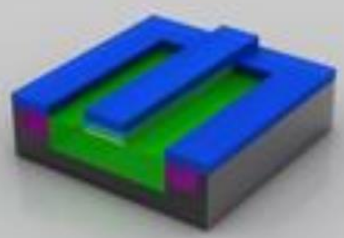
ION IMPLANTATION – Implanted Ion Path



Typical Values

Deep Retrograde Well	=	800-1000 KcV or 1-3 x 10^{13} ions/cm^3
N-Well	=	200 KcV or 1 x 10^{13} ions/cm^3
Source-Drain	=	30 KcV or 3-5 x 10^{15} ions/cm^3
Buried Layer	=	80-100 KcV or 1-5 x 10^{15} ions/cm^3
Resistors	=	50 KcV or .1-10 x 10^{13} ions/cm^3

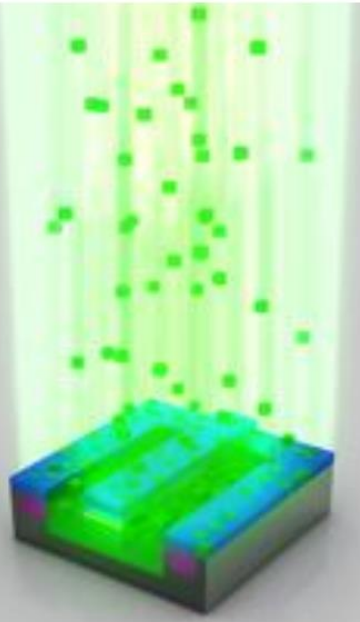
ION IMPLANTATION



Applying Photo Resist *–*

scale: transistor level (~50-200nm)

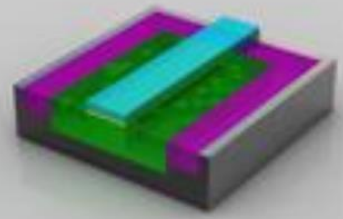
There's photo resist (blue color) applied, exposed and exposed photo resist is being washed off before the next step. The photo resist will protect material that should not get ions implanted.



Ion Implantation *–*

scale: transistor level (~50-200nm)

Through a process called ion implantation (one form of a process called doping), the exposed areas of the silicon wafer are bombarded with various chemical impurities called Ions. Ions are implanted in the silicon wafer to alter the way silicon in these areas conducts electricity. Ions are shot onto the surface of the wafer at very high speed. An electrical field accelerates the ions to a speed of over 300,000 km/h (~185,000 mph)



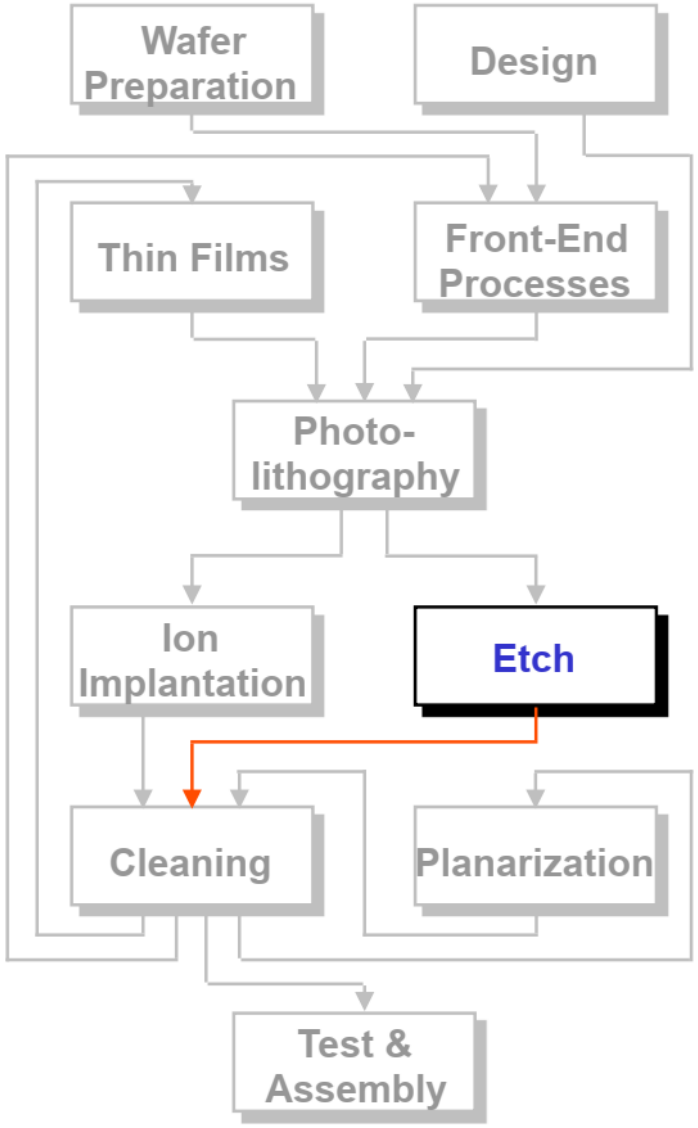
Removing Photo Resist *–*

scale: transistor level (~50-200nm)

After the ion implantation the photo resist will be removed and the material that should have been doped (green) has alien atoms implanted now (notice slight variations in color)

ETCHING

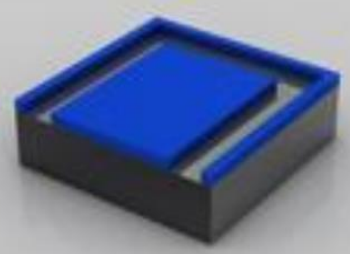
- Conductor Etch
  - Poly Etch and Silicon Trench Etch
  - Metal Etch
- Dielectric Etch



ETCHING – ETCHING TERMINOLOGY

- Isotropic Etching – Etching which is not directional. The etchant etches down and sideways at the same rate. Most wet etches are Isotropic.
- Anisotropic Etching – Etching which proceeds faster in one direction than in other directions, i.e., a directional etch. Some plasma and ion beam etches are directional.
- Selectivity – The relative etch rate for an etchant for one material versus another material. For example, hydrofluoric acid etches oxide but not silicon; hydrofluoric acid, therefore, has a high selectivity for oxide over silicon.

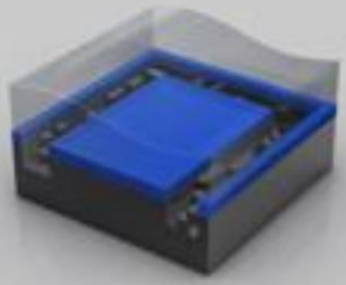
ETCHING



Washing off of Photo Resist –

scale: transistor level (~50-200nm)

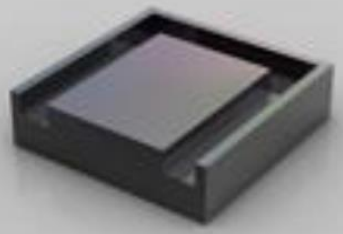
The gooey photo resist is completely dissolved by a solvent. This reveals a pattern of photo resist made by the mask.



Etching –

scale: transistor level (~50-200nm)

The photo resist is protecting material that should not be etched away. Revealed material will be etched away with chemicals.

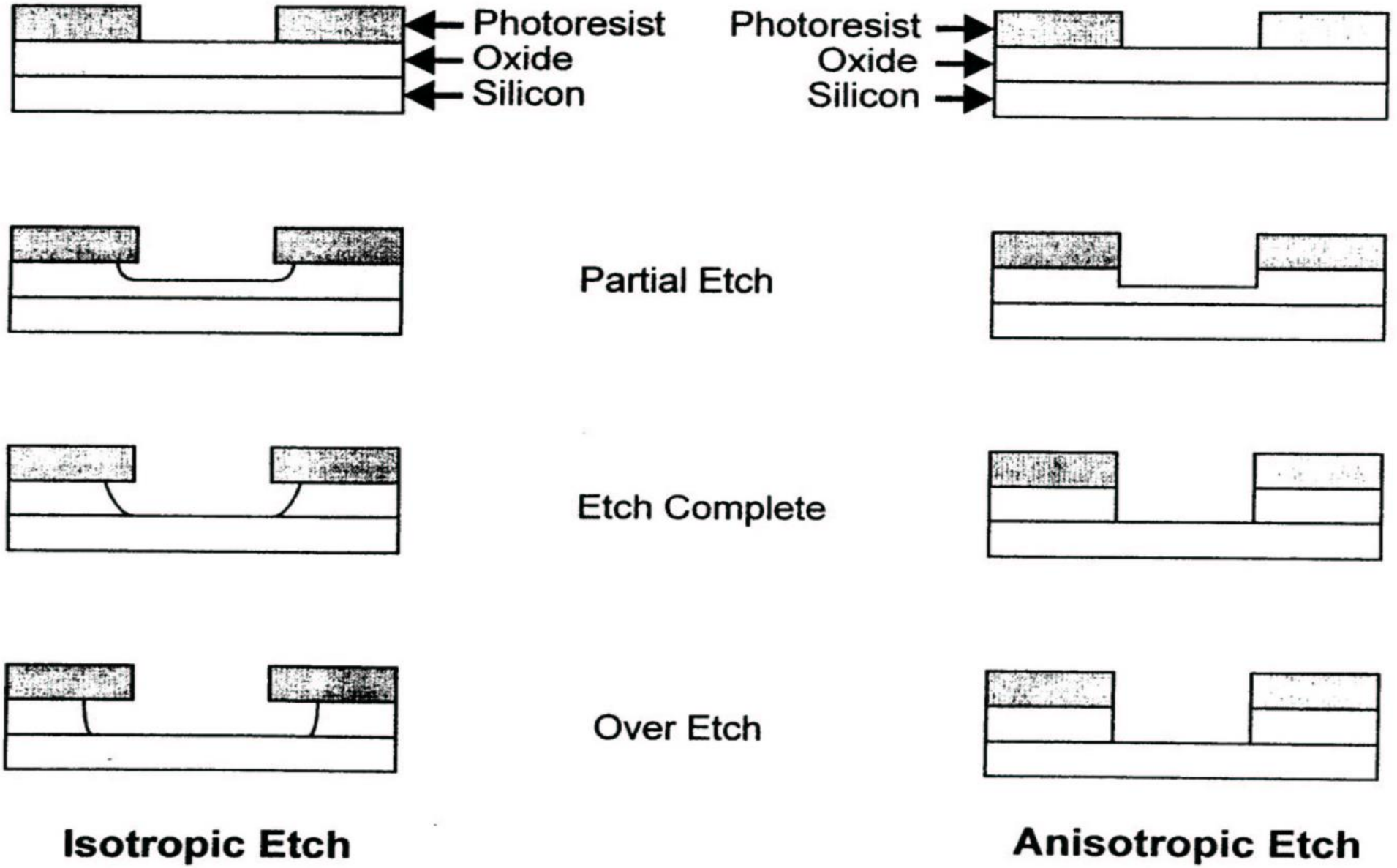


Removing Photo Resist –

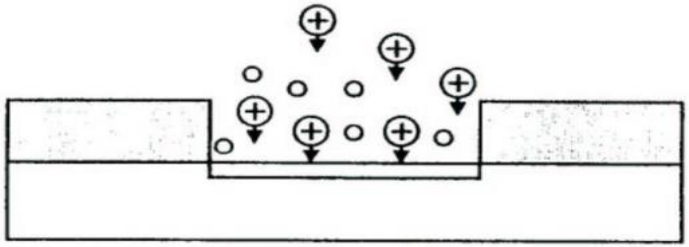
scale: transistor level (~50-200nm)

After the etching the photo resist is removed and the desired shape becomes visible.

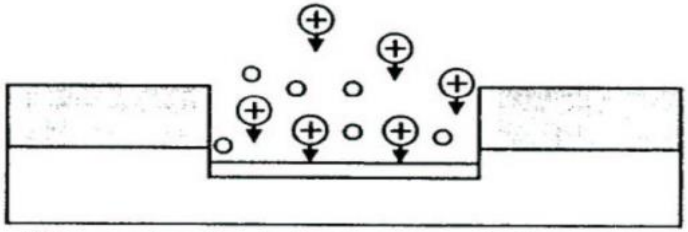
ETCHING – Isotropic Versus Anisotropic Etching



ETCHING – Anisotropic Etch Mechanisms

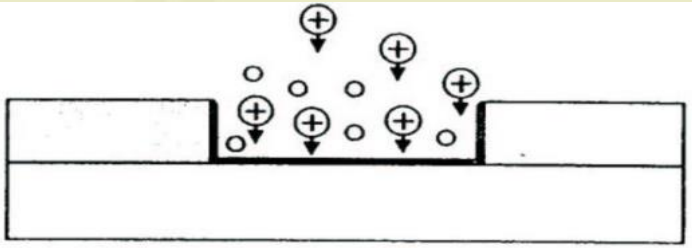


Ion bombardment creates a surface damage layer.

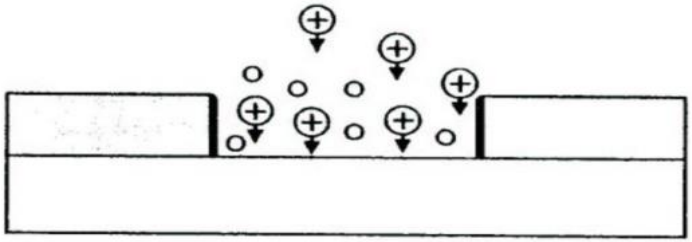


Chemical etchants - etch away the damage layer, ion bombardment creates a new damage layer.

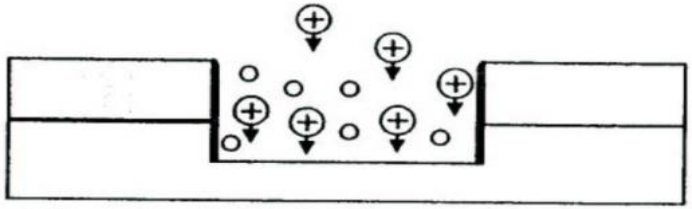
Damage Layer



Inhibitor covers the whole surface inhibiting etching.



Ion bombardment removes the inhibitor from the bottom of the exposed area.

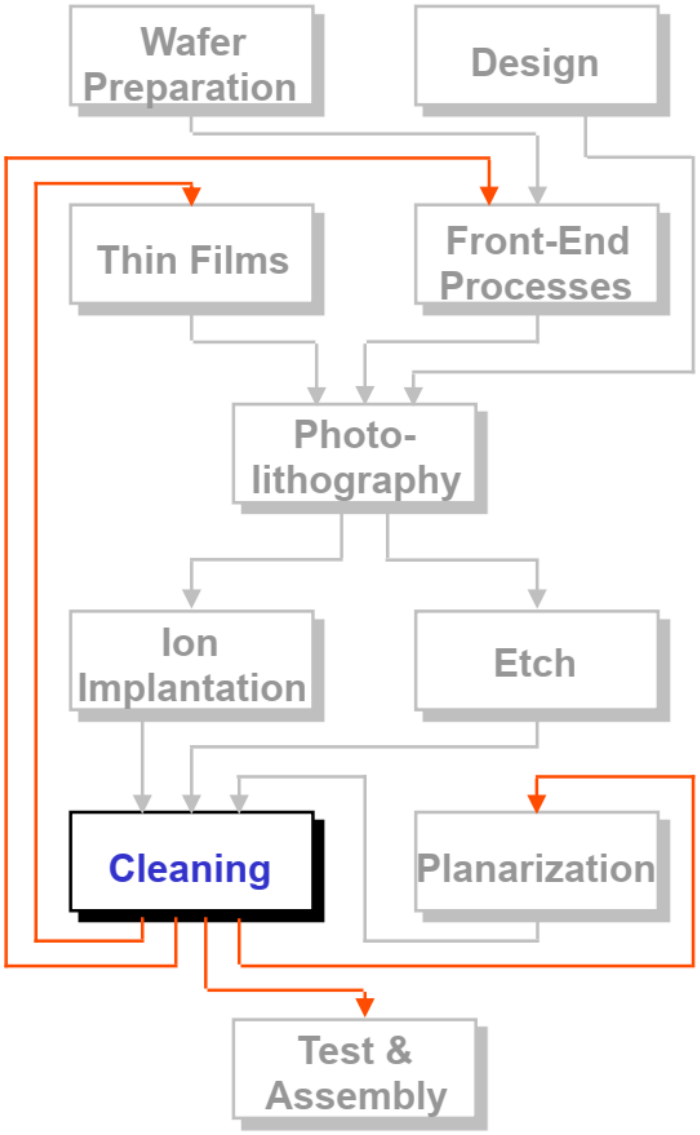


Chemical etchants - etch the area where the inhibitor has been removed by ion bombardment

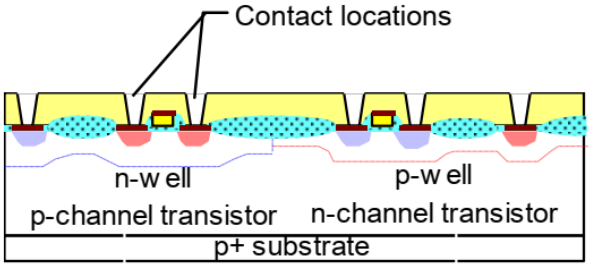
Inhibitor

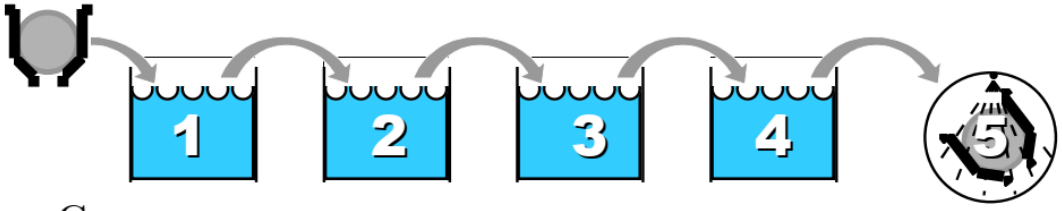
CLEANING

- Critical Cleaning
- Photoresist Strips
- Pre-Deposition Cleans



CRITICAL CLEANING





Process Conditions

Temperature: Piranha Strip is 180 degrees C.

1 Organics	2 Oxides	3 Particles	4 Metals	5 Dry
H_2SO_4 +	HF +	NH_4OH +	HCl +	H_2O or IPA +
H_2O_2	H_2O	H_2O_2 + H_2O	H_2O_2 + H_2O	N_2
H_2O Rinse	H_2O Rinse	H_2O Rinse	H_2O Rinse	

RCA Clean

SC1 Clean (H_2O + NH_4OH + H_2O_2) *

* SC2 Clean (H_2O + HCl + H_2O_2) *

Piranha Strip

* H_2SO_4 + H_2O_2 *

Nitride Strip

H_3PO_4 *

Oxide Strip

HF + H_2O *

Dry Strip

N_2O

O_2

CF_4 + O_2

O_3

Solvent Cleans

NMP

Proprietary Amines (liquid)

Dry Cleans

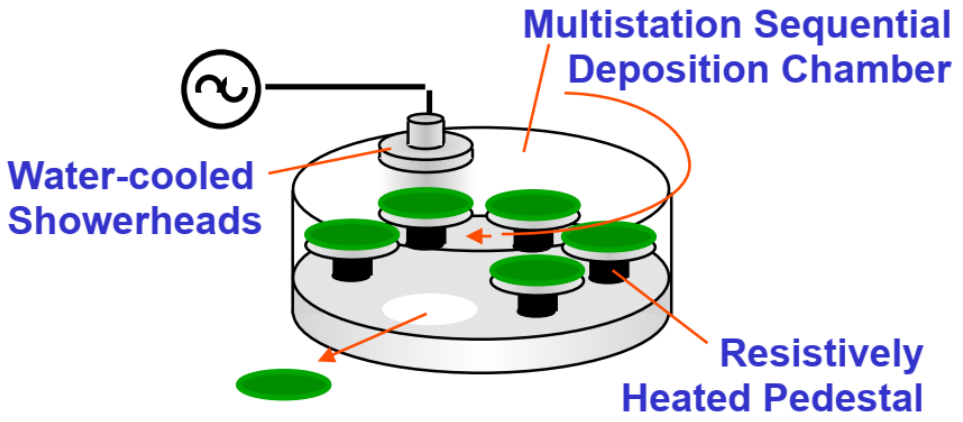
HF

O_2 Plasma

Alcohol + O_3

CLEANING

Chamber Cleaning



Chemical Reactions

Oxide Etch: $SiO_2 + C_2F_6 \rightarrow SiF_4 + CO_2 + CF_4 + 2\ CO$

Process Conditions

Flow Rates: 10 to 300 sccm

Pressure: 10 to 100 mTorr

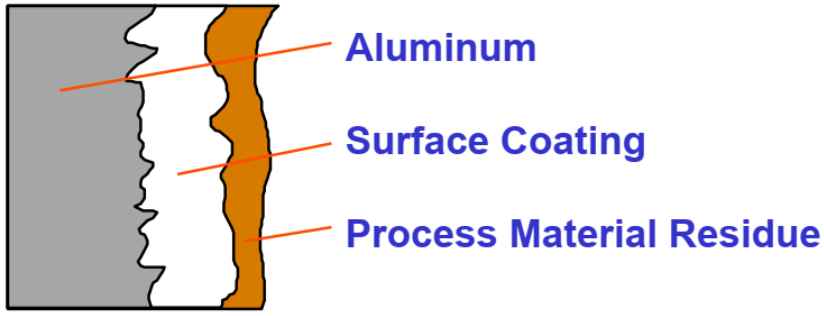
RF Power: 100 to 200 Watts

Chamber Cleaning

C_2F_6 *

NF_3

ClF_3

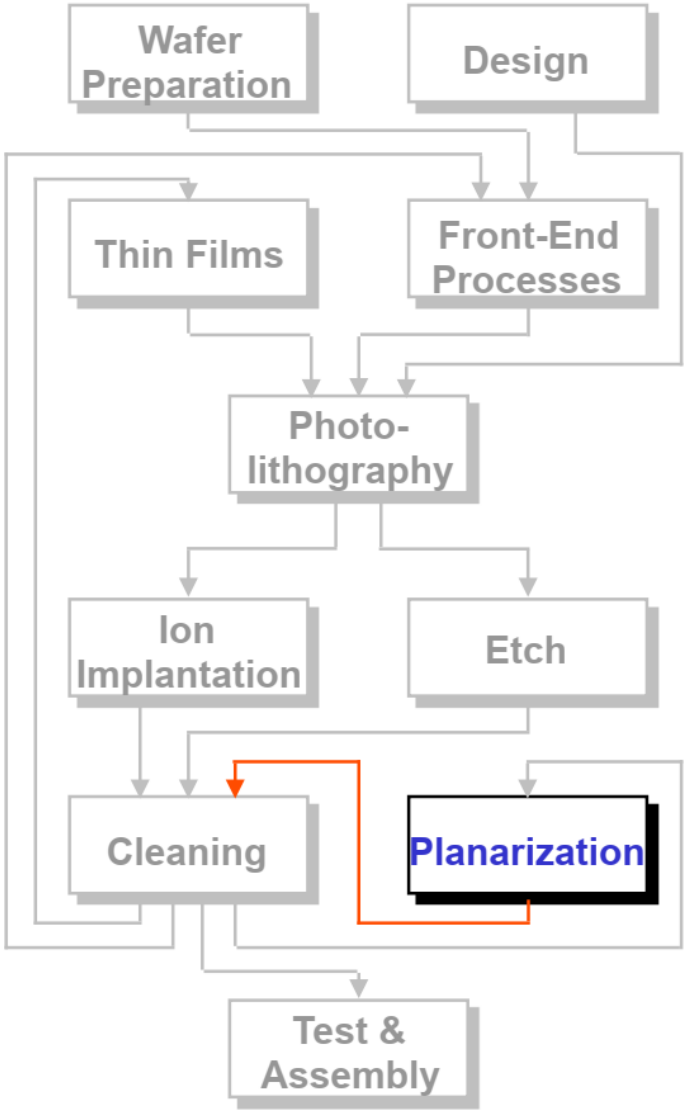


Chamber Wall Cross-Section

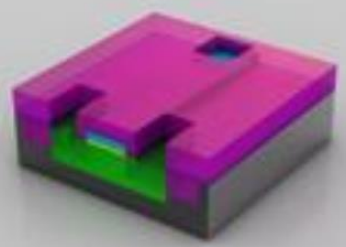
* High proportion of the total product use

PLANARIZATION

- Electroplating
- Oxide planarization
- Metal Planarization



METAL DEPOSITION



Ready Transistor –

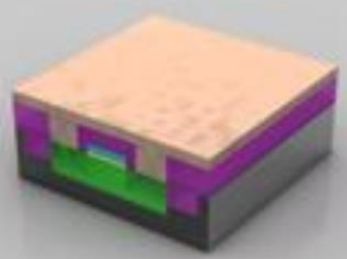
scale: transistor level (~50-200nm)

This transistor is close to being finished. Three holes have been etched into the insulation layer (magenta color) above the transistor. These three holes will be filled with copper which will make up the connections to other transistors.

Electroplating –

scale: transistor level (~50-200nm)

The wafers are put into a copper sulphate solution as this stage. The copper ions are deposited onto the transistor thru a process called electroplating. The copper ions travel from the positive terminal (anode) to the negative terminal (cathode) which is represented by the wafer.

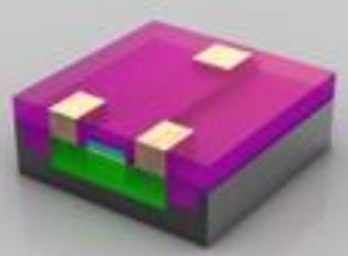


After Electroplating –

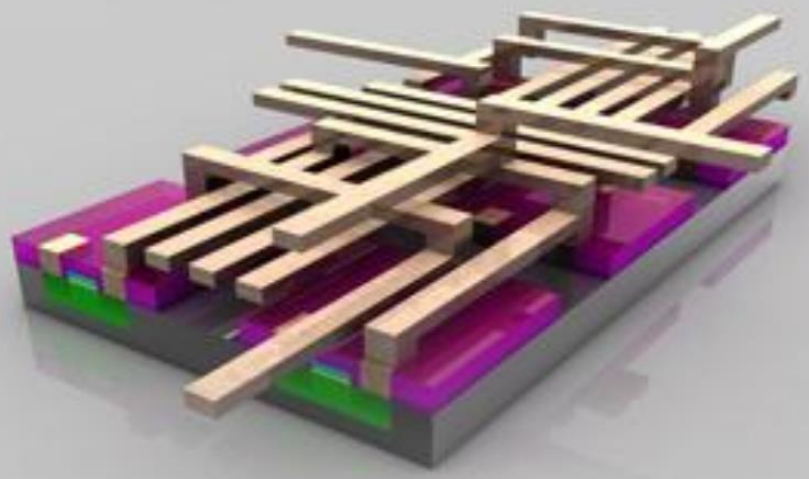
scale: transistor level (~50-200nm)

On the wafer surface the copper ions settle as a thin layer of copper.

METAL LAYERS

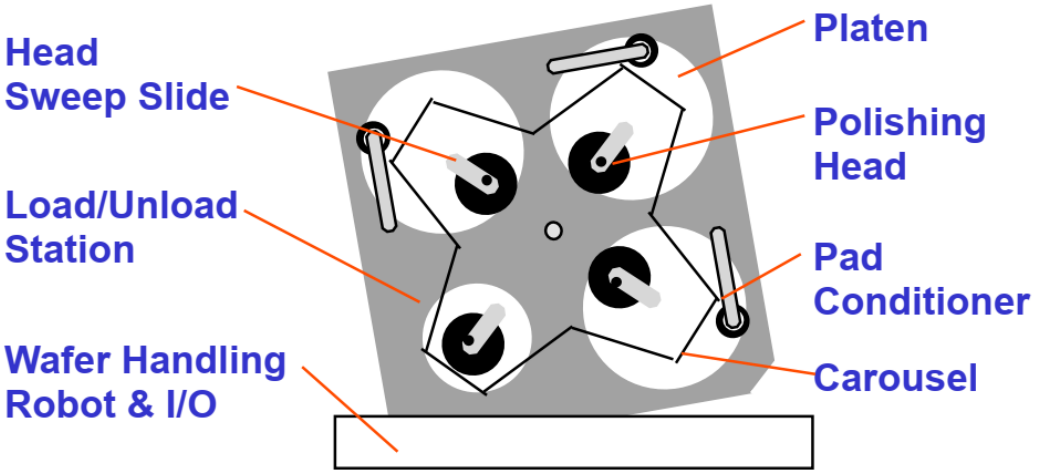


Polishing *–*
scale: transistor level (~50-200nm)
The excess material is polished off.



Metal Layers *– scale: transistor level (six transistors combined ~500nm)*
Multiple metal layers are created to interconnect (think: wires) in between the various transistors. How these connections have to be "wired" is determined by the architecture and design teams that develop the functionality of the respective processor (e.g. Intel® Core™ i7 Processor). While computer chips look extremely flat, they may actually have over 20 layers to form complex circuitry. If you look at a magnified view of a chip, you will see an intricate network of circuit lines and transistors that look like a futuristic, multi-layered highway system.

Chemical Mechanical Planarization (CMP)



Process Conditions (Oxide)

Flow: 250 to 1000 ml/min
Particle Size: 100 to 250 nm
Concentration: 10 to 15%, 10.5 to 11.3 pH

Process Conditions (Metal)

Flow: 50 to 100 ml/min
Particle Size: 180 to 280 nm
Concentration: 3 to 7%, 4.1 - 4.4 pH

Backing (Carrier) Film

Polyurethane

Pad

Polyurethane

Pad Conditioner

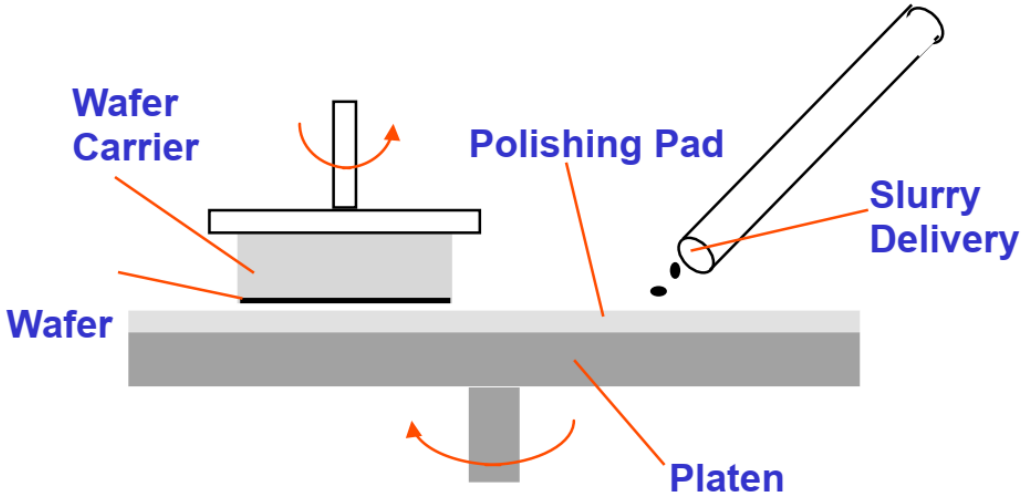
Abrasive

CMP (Oxide)

Silica Slurry *
KOH *
NH_4OH
H_2O

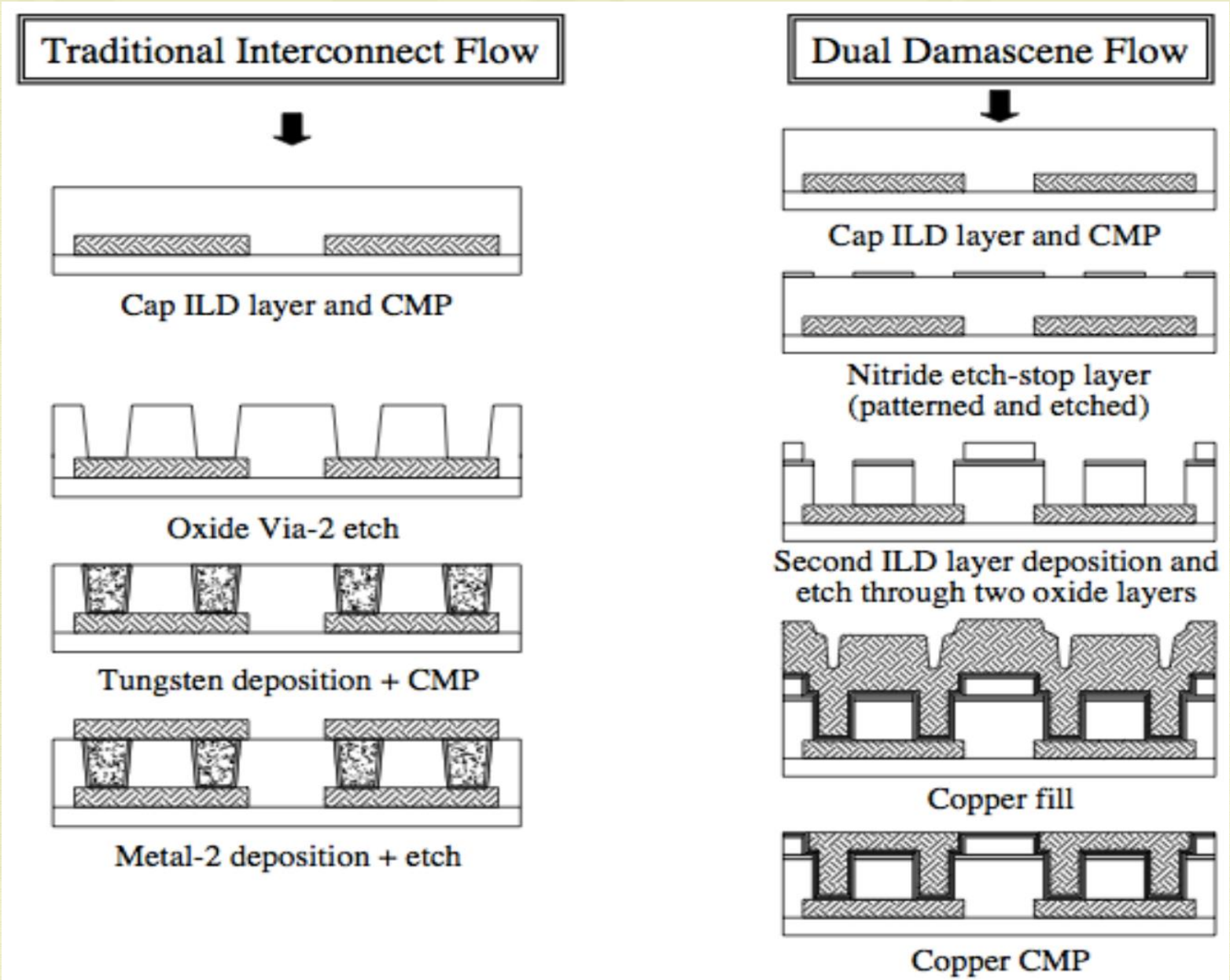
CMP (Metal)

Alumina *
$FeNO_3$



* High proportion of the total product use.

METALLIZATION



Example CMOS process flow