PART III: Fabrication of Nano Systems

1. Deposition

2. Lithography

3. Etching

4. Interconnects

1. Deposition Technology

A. Physical Vapor Deposition (PVD)

- Introduction to Sputtering
- Various Sputtering Techniques

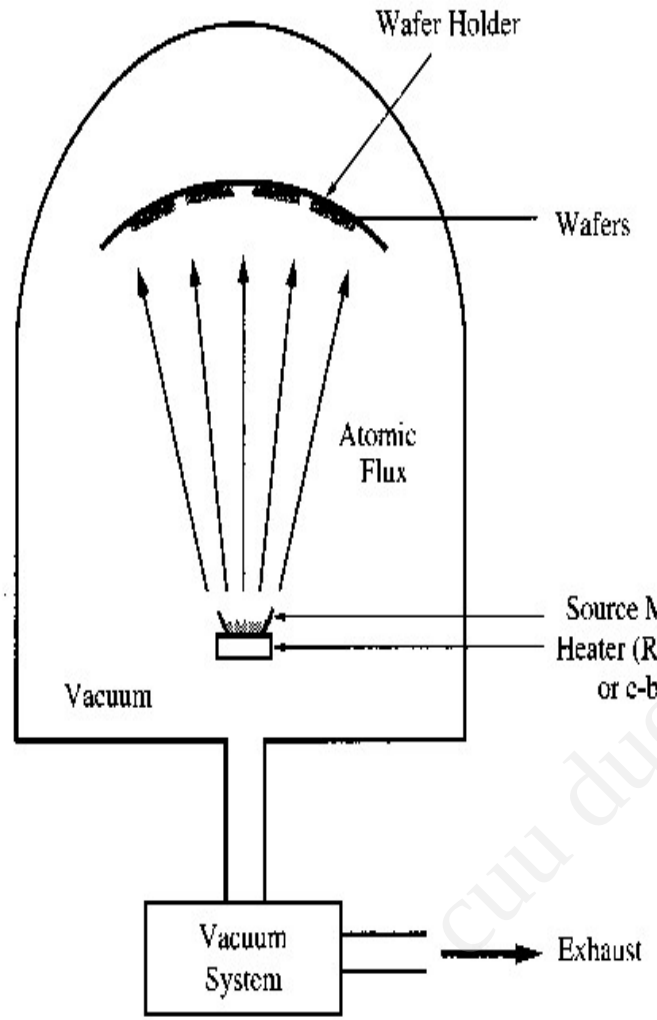
B. Chemical Vapor Deposition (CVD)

- Introduction to CVD
- Various CVD Equipment and Techniques

INTRODUCTION TO PVD

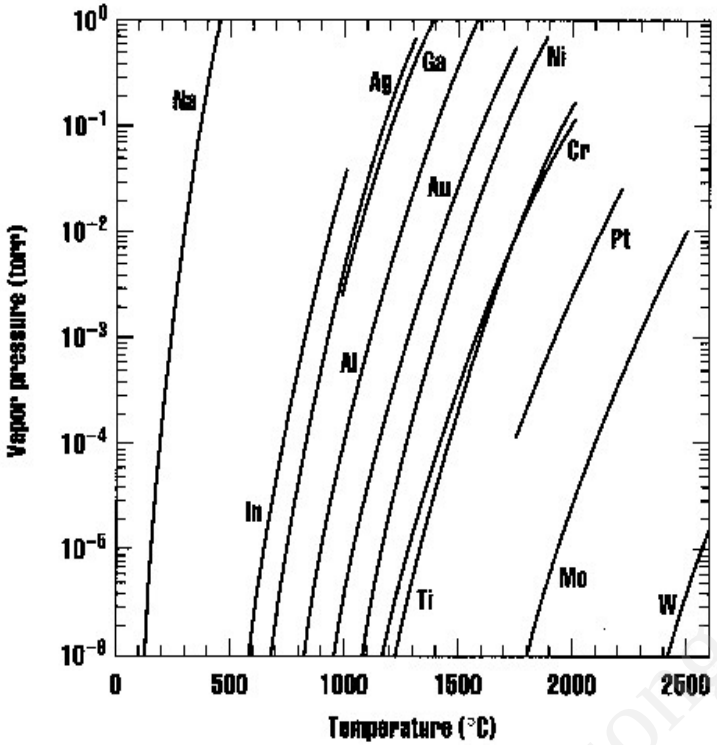
- PVD is a process to form a non-volatile solid film on the substrate by physical methods.
- PVD is mainly used for metallization in Si IC applications.
- Mainly, three PVD methods exist
  - Evaporation (Thermal and e-beam)
  - Sputtering (Glow discharge)
  - Pulsed laser deposition (laser ablation)
    - Very seldom used in Si IC, we will not discuss this technique

EVAPORATION (BASIC OPERATION)



- **Wafers are loaded into a high vacuum chamber that is commonly pumped already**
- **The charge or material to be deposited is loaded into a heated container called the crucible. It can be heated by means of an embedded resistance heater and an external power supply.**
- **As the material in the crucible becomes hot, the charge gives off a vapor.**
- **Since the pressure in the chamber is very low, the atoms of vapor travel across the chamber in a straight line until they strike a surface where they accumulate as a film.**

EVAPORATION (PHASE DIAGRAMS)



Sublimation: vapor is from solid
Evaporation: vapor is from liquid
Normally, evaporation provides higher vapor pressure and hence higher deposition rate

Sublimation and Evaporation

- Vapor pressure is a very strong function of temperature
- **Normally, a partial of about 1-10 mT or more is required to achieve reasonable deposition rates (on the order of 0.1-1 um per minute), and one can see that about 1100°C is needed for the evaporation of Al. This means that the Al is evaporated from the liquid phase.**
- **When the material is evaporated from the liquid phase, the vapor pressure can be given as**

$$P_e = 3x10^{12}\sigma^{3/2}T^{-1/2}e^{\Delta Hv/NkT}$$

Where
σ is surface tension of the metal
N is Avogadro's number
ΔHv is enthalpy of evaporation

EVAPORATION (DEPOSITION RATES)

- **The mass loss rate of the crucible can be calculated as**

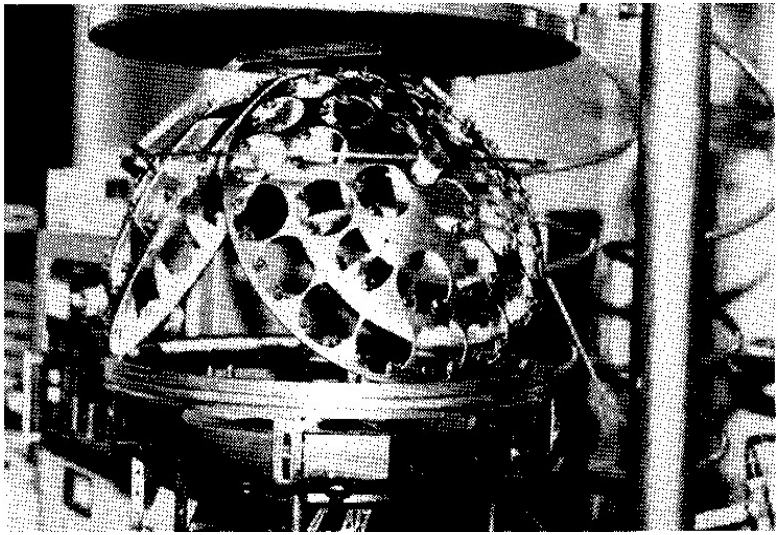
$$R_{ML} = \int \sqrt{\frac{M}{2\pi kT}} P_e dA = \sqrt{\frac{M}{2\pi k}} \int \frac{Pe}{\sqrt{T}} dA$$

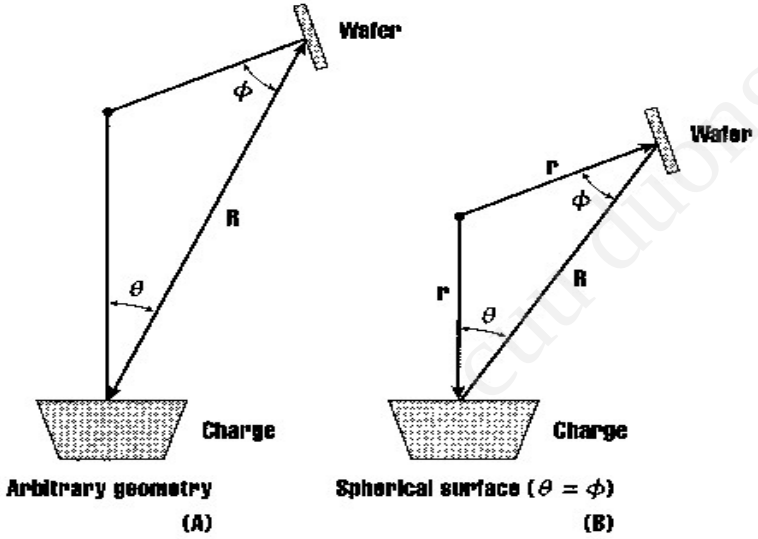
Where, the integral is done over the surface of the charge in the crucible.
M is the atomic mass, P_e is the equilibrium vapor pressure of the crucible material

- **Two approximations:**
  - **If the charge is completely molten it is common to assume that natural convection and thermal conduction will keep the temperature of the charge nearly constant across the crucible**
  - **It is also assumed that the opening of the crucible has a constant area, A**

$$R_{ML} = \sqrt{\frac{M}{2\pi k}} \frac{P_e}{\sqrt{T}} A$$

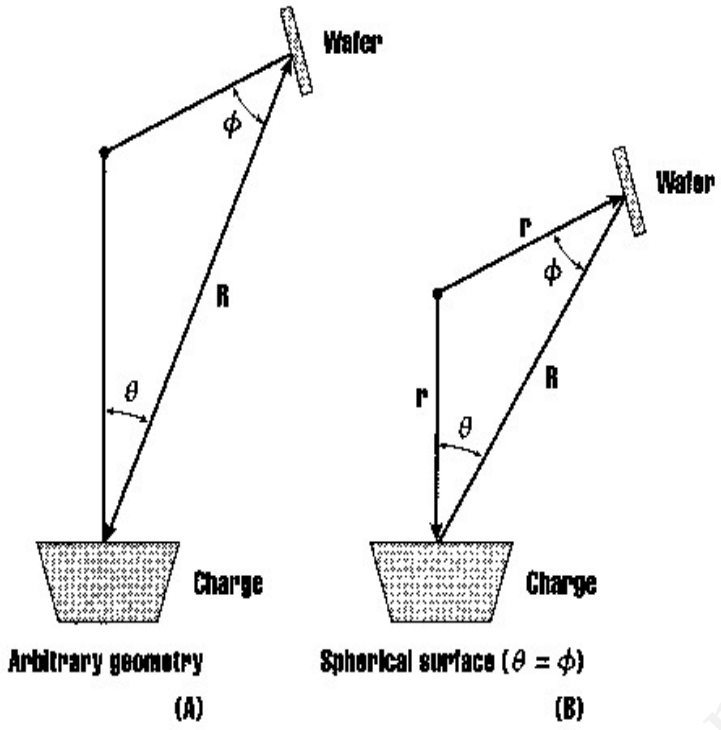
EVAPORATION (DEPOSITION RATES)





- To find the deposition rate on the surface of a wafer, the fraction of the material leaving the crucible that accumulates on the surface of the wafer must be determined.
- Material ejected from the crucible travels in a straight path to the wafer surface due to low pressure.
- Assuming that all of the material that arrives at the wafer sticks and remains there, the arrival rate then is governed by simple geometry.
- Thus, the constant of proportionality is just the fraction of the total solid angle subtended by the wafer as seen from the substrate.

EVAPORATION (DEPOSITION RATES)



- The proportionality constant is given by

$$k = \frac{\cos\theta\cos\phi}{\pi R^2}$$

- Deposition rate depends on the location and orientation of the wafer in the chamber
- Wafers directly above the crucible will be coated more heavily than wafers off to the side
- Film uniformity is also a concern
- One method to obtain good uniformity is to place the crucible and wafers on the surface of a sphere. Then

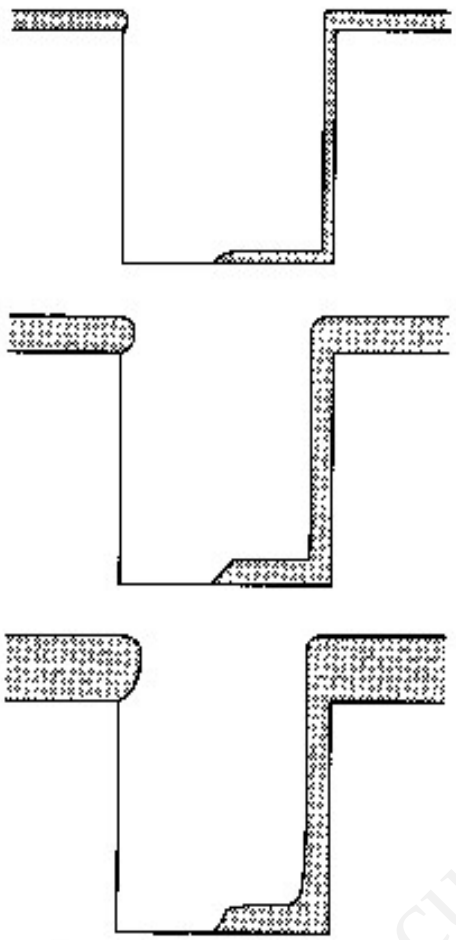
$$\cos\theta = \cos\phi = \frac{R}{2r}$$

- The deposition rate is the mass arrival per unit area divided by the mass density of the film

$$R_d = \sqrt{\frac{M}{2\pi k\rho^2}}\frac{Pe}{\sqrt{T}}\frac{A}{4\pi r^2}$$

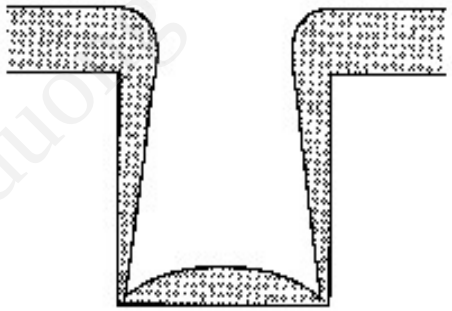
1st term: depends on material
2nd term: depends on temperature
3rd term: depends on geometry of the chamber

EVAPORATION (STEP COVERAGE)



Low adatom mobility and nonrotated

(A)



Heated and rotated

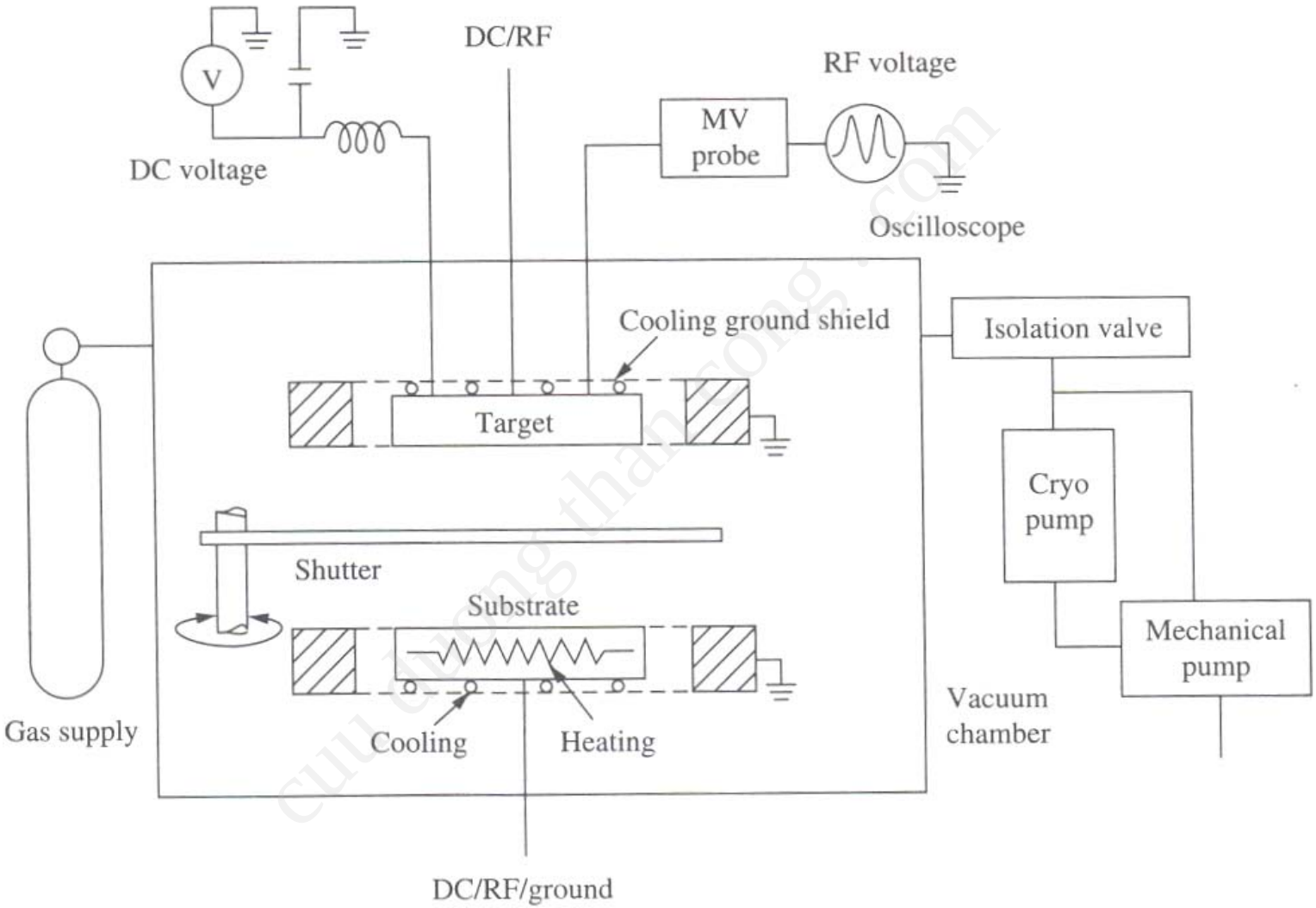
(B)

Two methods to improve step coverage:

(1)To rotate the wafer substrates

(2)To heat the wafer substrate

INTRODUCTION TO PVD (SPUTTERING EQUIPMENT)



SPUTTERING (RF SPUTTER DEPOSITION)

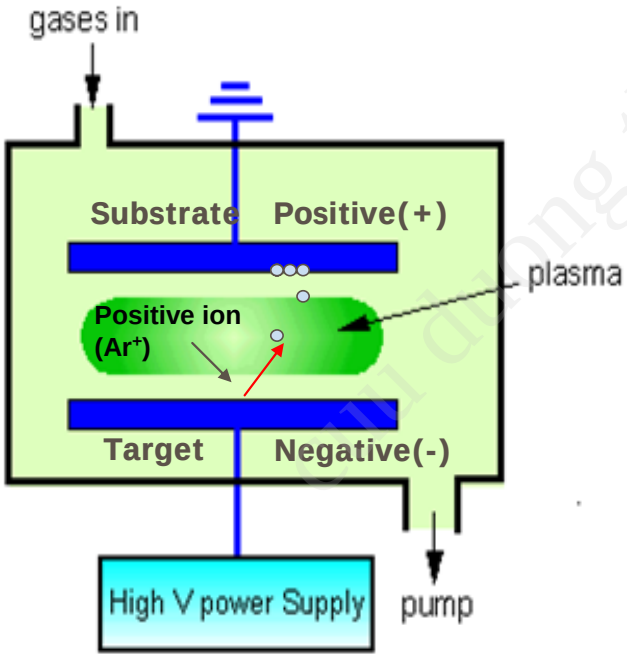
- **DC sputter deposition is not suitable for insulator deposition**
  - **A problem with applying the necessary DC voltage to the insulating target to initiate a plasma**
  - **Other major difficulties arise, such as particle issue**
- **The solution is to use RF, instead of DC. 13.56MHz RF power source is commonly used.**
- **RF voltages can be coupled capacitively through the insulating target to the plasma, so that conducting electrodes are not necessary**
- **The RF frequency is chosen to be high enough so that a continuous plasma discharge is maintained.**

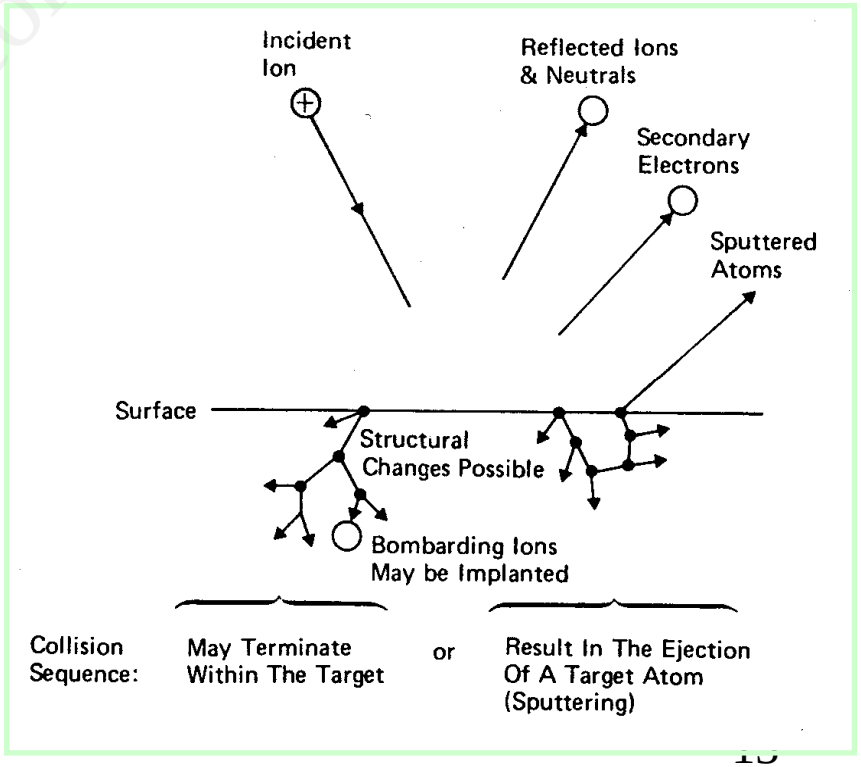
SPUTTERING (BIAS SPUTTERING)

- **Sometimes sputtering of wafer is desirable for**
  - **Precleaning the wafer before actual deposition**
  - **Bias sputtering, where deposition and sputtering are done simultaneously**
- **A negative bias relative to the plasma is applied to the wafer electrode, which is now electrically isolated from the chamber walls.**
- **Positive Ar ions from the plasma will now be accelerated to the wafers on the substrate and sputter off the atoms.**
- **Usually an RF bias is used since the wafers often have insulating films on them.**
- **In sputter etching or cleaning, no deposition is allowed to occur on the wafer by using a shutter to block sputtered material from the target.**
  - **During this step, a controlled thickness of surface material is sputtered off the wafer, removing any contamination or native oxide**
  - **A film can then be sputtered immediately afterward without breaking the vacuum**

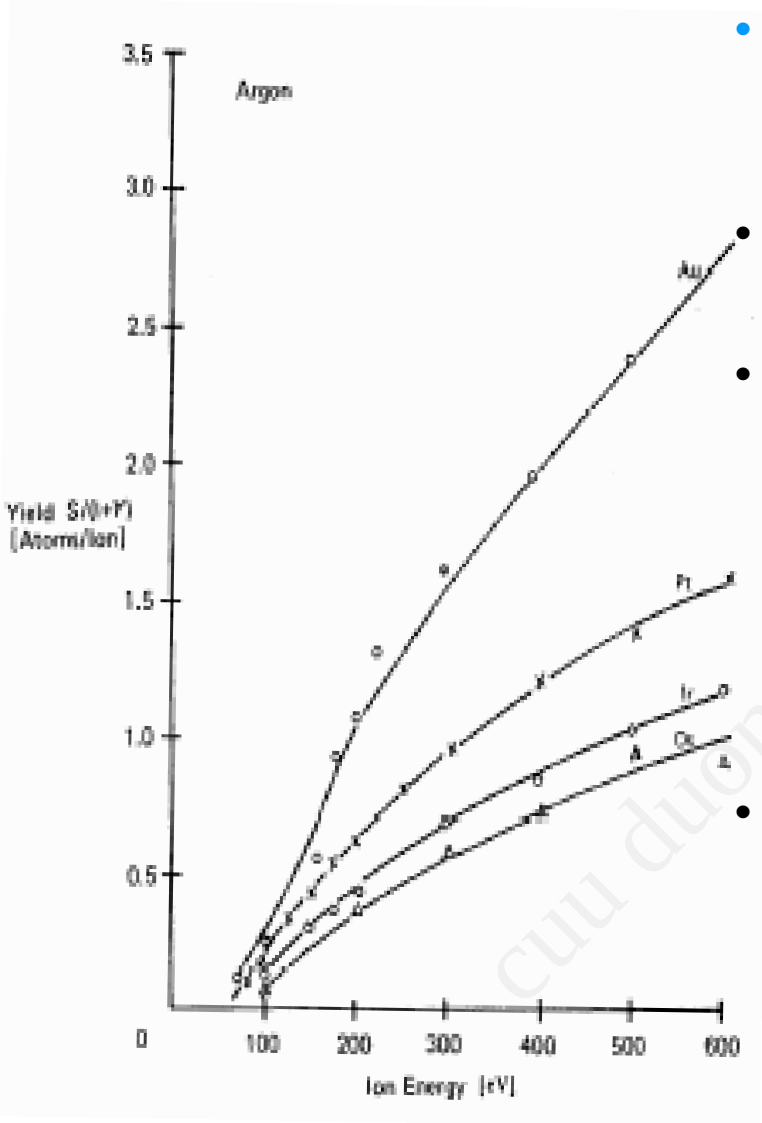
SPUTTERING (FUNDAMENTAL)

- Positive ions in the plasma are accelerated to the negatively biased target (hundreds of volts to thousands of volts)
- Energetic ions strike the target and dislodge or sputter the target atoms
- These atoms then travel freely through the plasma as vapor and strike the surface of the substrates, where they condense to form the deposited film
- Note: since the targets acts as an electrode in the DC mode of sputter deposition, the target must be conductive.





SPUTTERING (DEPOSITION RATE)

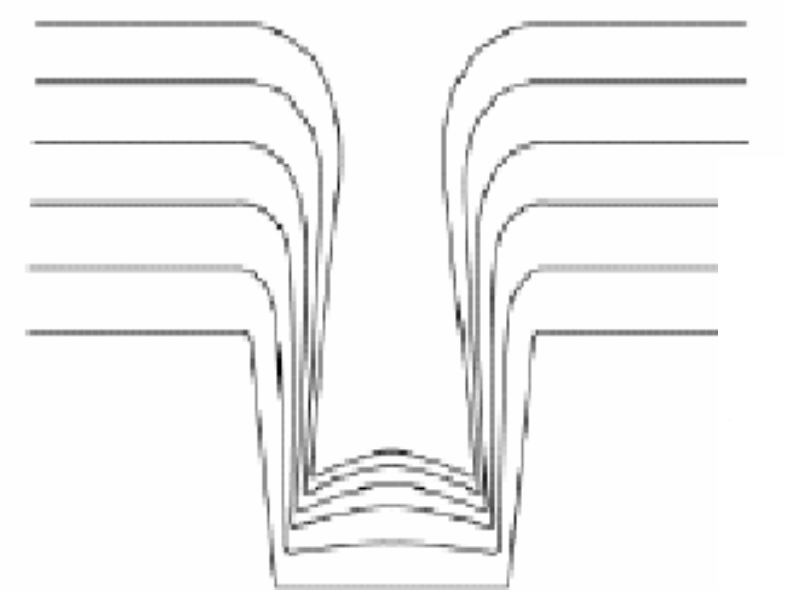


- **Sputter yield (S) is the ratio of the number of target atoms ejected from the target to the number of ions incident on the target.**
- **Sputter yield depends on ion mass, ion energy, target mass and target crystallinity.**
- **Sputter yield is proportional to energy of incident ion (E) but inversely proportional to surface binding energy (U_0)**

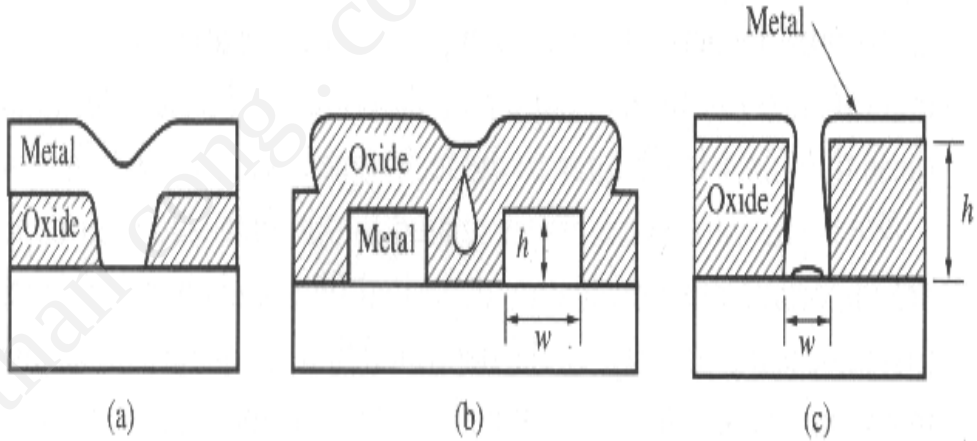
$$S \propto \frac{4 m_t m_{ion}}{(m_t + m_{ion})^2} \frac{E}{U_0}$$

- **For ion energy larger than threshold energy, sputter yield tends to increase as the square of the energy up to about 100eV, then linearly with energy. Above ~1000eV, yield increases only slightly until the onset of implantation.**

SPUTTERING (STEP COVERAGE)



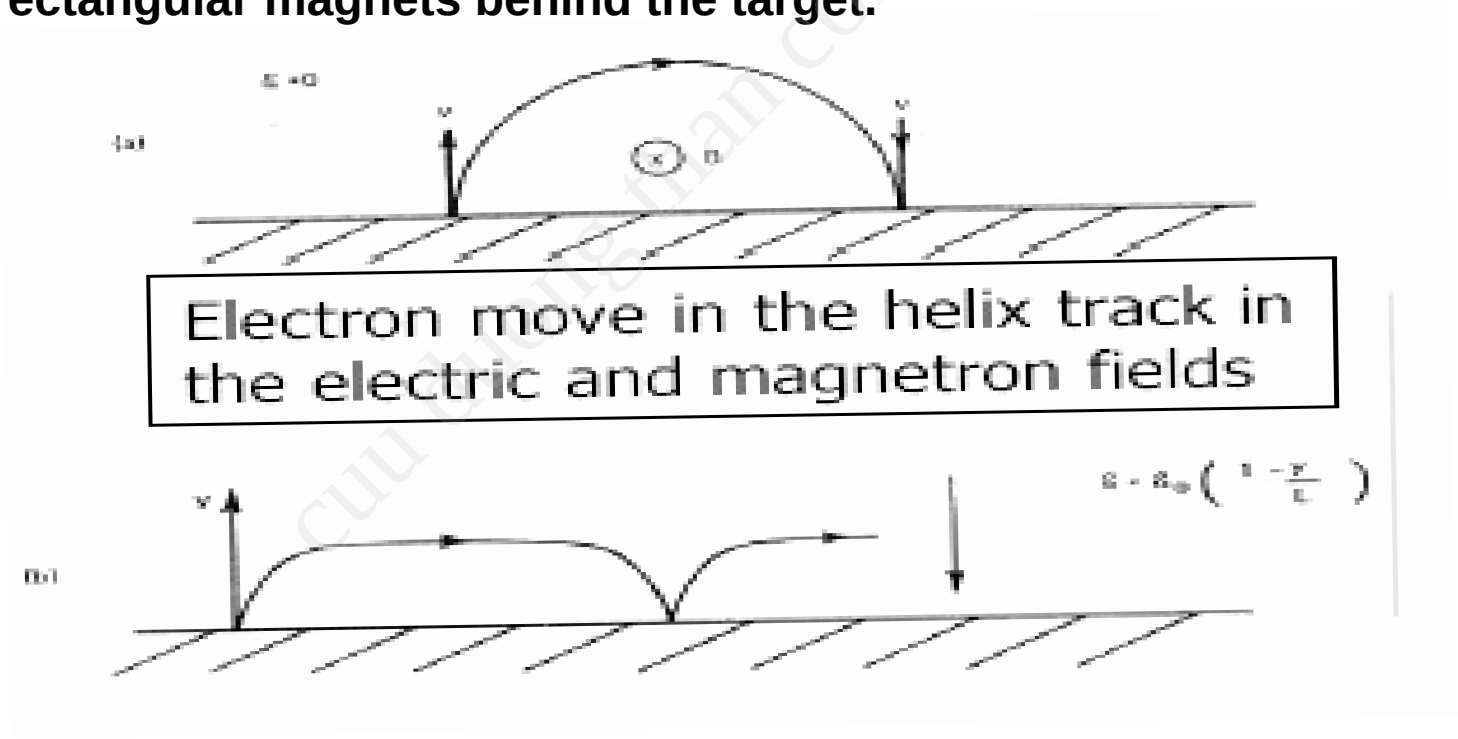
- **Sputter has worse step coverage than CVD**



- **Heating substrate can improve dramatically the step coverage due to surface diffusion**
- **A second technique for improving the step coverage is to apply an RF bias to wafers. (will discuss later)**

SPUTTERING (MAGNETRON SPUTTER DEPOSITION)

- **In both conventional DC and RF sputtering, efficiency of ionization from energetic collision between electrons and gas atoms is rather low**
- **In magnetron sputtering, magnets are used to increase the percentage of electrons that take part in ionization events, and the ionization efficiency is increased significantly (about 10-100 times higher)**
- **A magnetic field is applied at right angle to the electric field, usually by placing large rectangular magnets behind the target.**



INTRODUCTION TO CVD

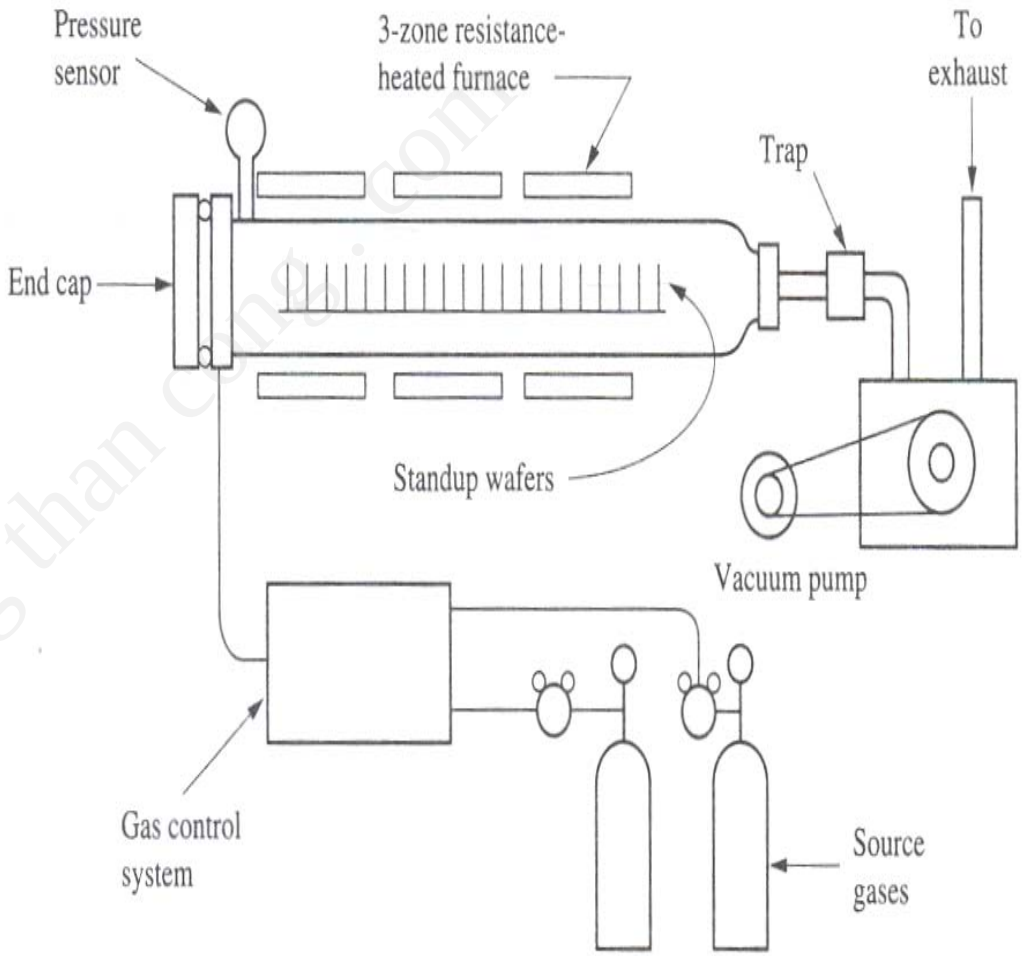
- CVD is a process to form a non-volatile solid film on the substrate by reaction of vapor phase chemicals.

- Energy for reaction is supplied by thermal methods, photons or electrons.

In microelectronics manufacturing, polycrystalline Si (called Poly-Si), dielectric materials such as silicon dioxide (SiO_2) and silicon nitride (Si_3N_4), interconnect / contact plug such as tungsten (W), silicide materials such as tungsten silicide (WSi_6), and diffusion barriers (Ti/TiN) are deposited by CVD techniques.

INTRODUCTION TO CVD

- **Advantages of CVD processes over other competing techniques**
  - **Wide variety of chemical compositions**
  - **High deposition rates with good step coverage**
  - **Low manufacturing cost**
  - **Only one stage (LPCVD) or no pumping (APCVD) processes are possible**



INTRODUCTION TO CVD

- **Desired characteristics of CVD films are**
  - **Good thickness uniformity**
  - **High purity and density**
  - **Controlled composition and stoichiometry**
  - **High degree of structural perfection**
  - **Good adhesion**
  - **Good step coverage***

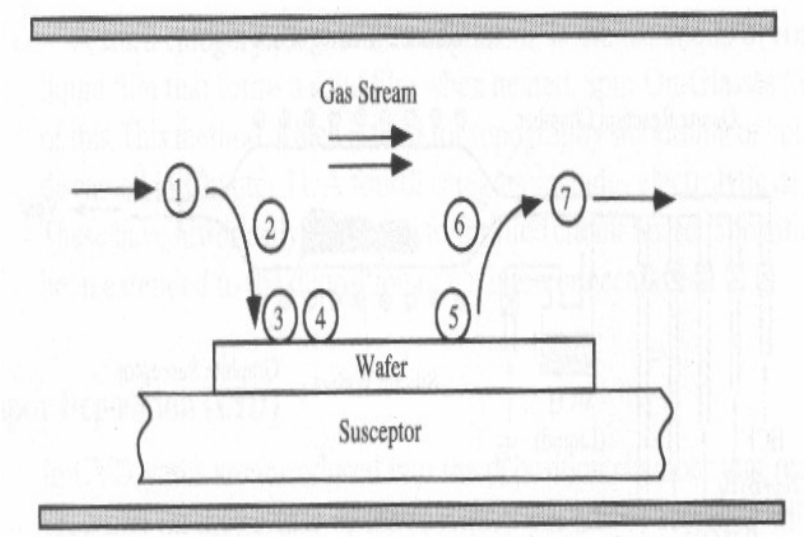
*** Aspect ratio (AR) of a feature (AR = height of feature/width of feature = h/w)**

→ A parameter that can reflect filling and bottom coverage

→ The feature could be a metal line or a spacer such as a gap between metal lines.

→ A deep and narrow contact hole would have a large aspect ratio and would be harder to fill.

INTRODUCTION TO CVD



1) Transport of reactants by forced convection to deposition region.
2) Mass transfer of reactants by diffusion from the main gas stream through the boundary layer to the wafer surface.
3) Adsorption of reactants on the wafer surface.
4) Surface processes, including chemical decomposition or reaction, surface migration to attachment sites, site incorporation and other surface reactions.
5) Desorption of byproducts from the surface
6) Transport of byproducts by diffusion through the boundary layer and back to the main gas stream
7) Transport of byproducts by forced convection away from deposition region.

VARIOUS CVD FILMS (SILICON DIOXIDE DEPOSITION)

- **SiO_2 is a widely used material for insulation in microelectronic fabrication, for example,**
  - **Isolation between cells**
  - **Hard masking**
  - **Insulation between poly-silicon and metals, and passivation.**

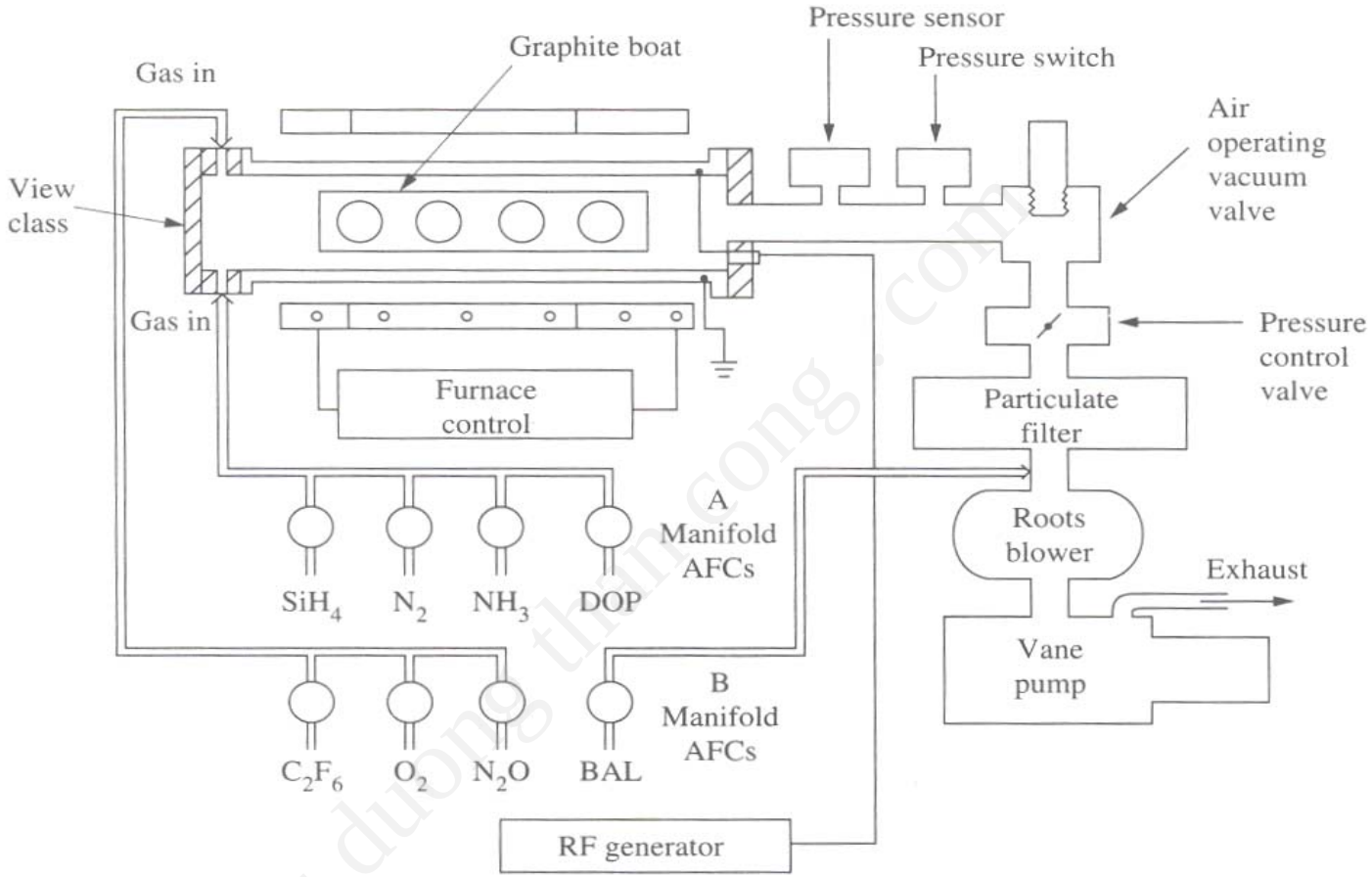
- **Requirements of deposited films:**
  - **Uniform thickness and composition**
  - **Good adhesion to the substrate**
  - **High stress resistance**
  - **Good step coverage**

VARIOUS CVD FILMS (PECVD)

Plasma-Enhanced Deposition (PECVD)

- PECVD uses a rf power to generate a glow discharge to transfer energy to the reactant gases
- Deposition can be achieved at a lower temperature compared to APCVD or LPCVD
- Desired properties, such as good adhesion, low pinhole density, good step coverage, adequate electrical properties, have made PECVD films useful in ULSI circuits.
- PECVD silicon nitride is commonly used as the final passivation layer
- PECVD silicon oxide can be used as insulators between the metal layers
- PECVD amorphous silicon has been widely used in TFT LCD area

VARIOUS CVD FILMS (PECVD EQUIPMENT)



- Use of RF-induced plasma to supply energy into reactant gases
- Plasmas are highly ionized gases
- With additional energy from the plasma to the reactant gases, deposition can occur at lower temperatures

Plasma-Enhanced Deposition (PECVD)

- **Deposition Methods and Variables**
  - **PECVD requires**
    - **control and optimization of rf power density, frequency and duty cycle**
    - **Gas composition, flow rate, temperature, pressure etc.**
  - **PECVD process is a surface-reaction limited process**
  - **PECVD silicon oxide**

$$SiH_4 + O_2 \rightarrow SiO_2 + 2H_2$$

$$SiH_4 + 4N_2O \rightarrow SiO_2 + 4N_2 + 2H_2O$$

  - **PECVD silicon nitride**

$$SiH_4 + NH_3 \rightarrow SiN{:}H + 3H_2O$$

$$SiH_4 + N_2 \rightarrow 2SiN{:}H + 3H_2$$

  - **PECVD amorphous silicon**

$$SiH_4 \rightarrow Si + 2H_2$$

2. Lithography Technology

A. INTRODUCTION

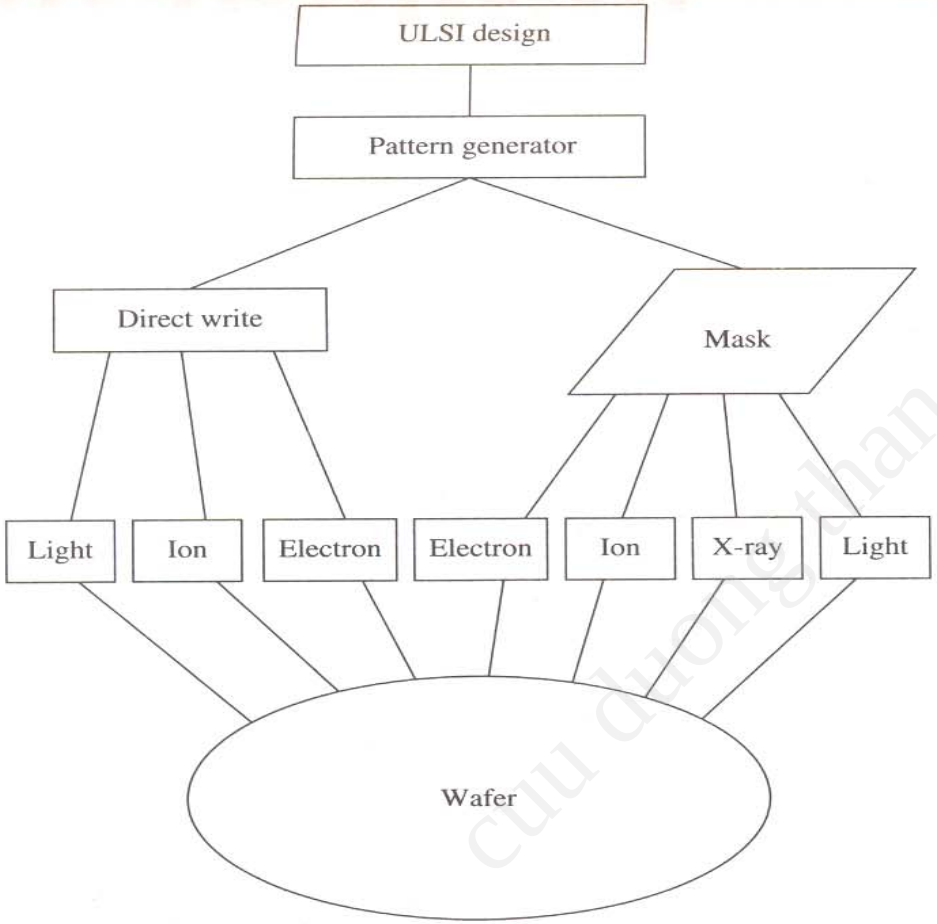
B. PHOTORESIST PROPERTIES

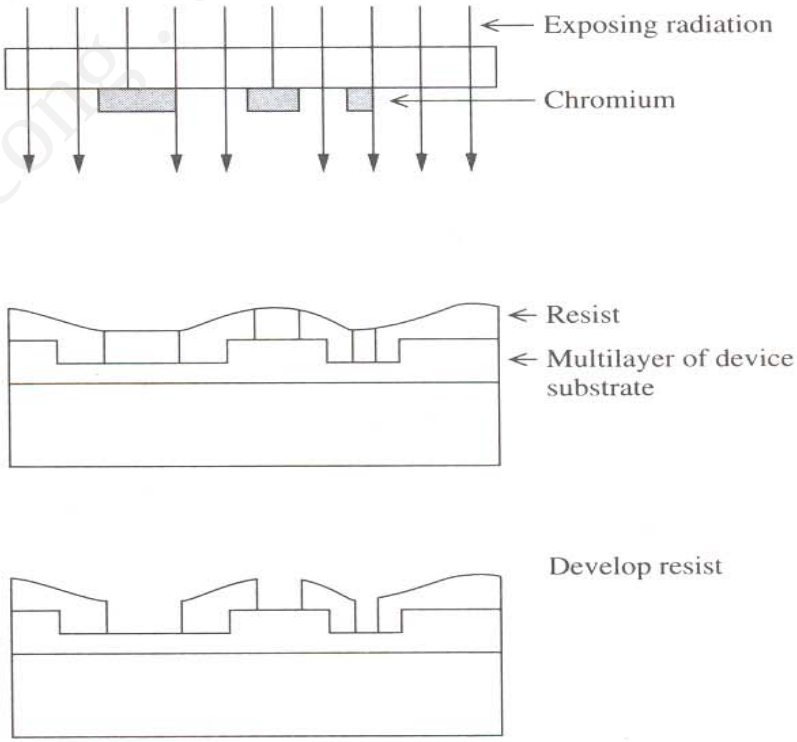
- PHOTORESIST PROCESSING
- PHOTORESIST MATERIAL PARAMETERS

C. OPTICAL LITHOGRAPHY

- KEY PARAMETERS
- OPTICAL SOURCES AND PRINTING METHODS
- MASKS

Introduction to Lithography Process





Introduction to Lithography Process

- A light sensitive photoresist is deposited onto the wafer.

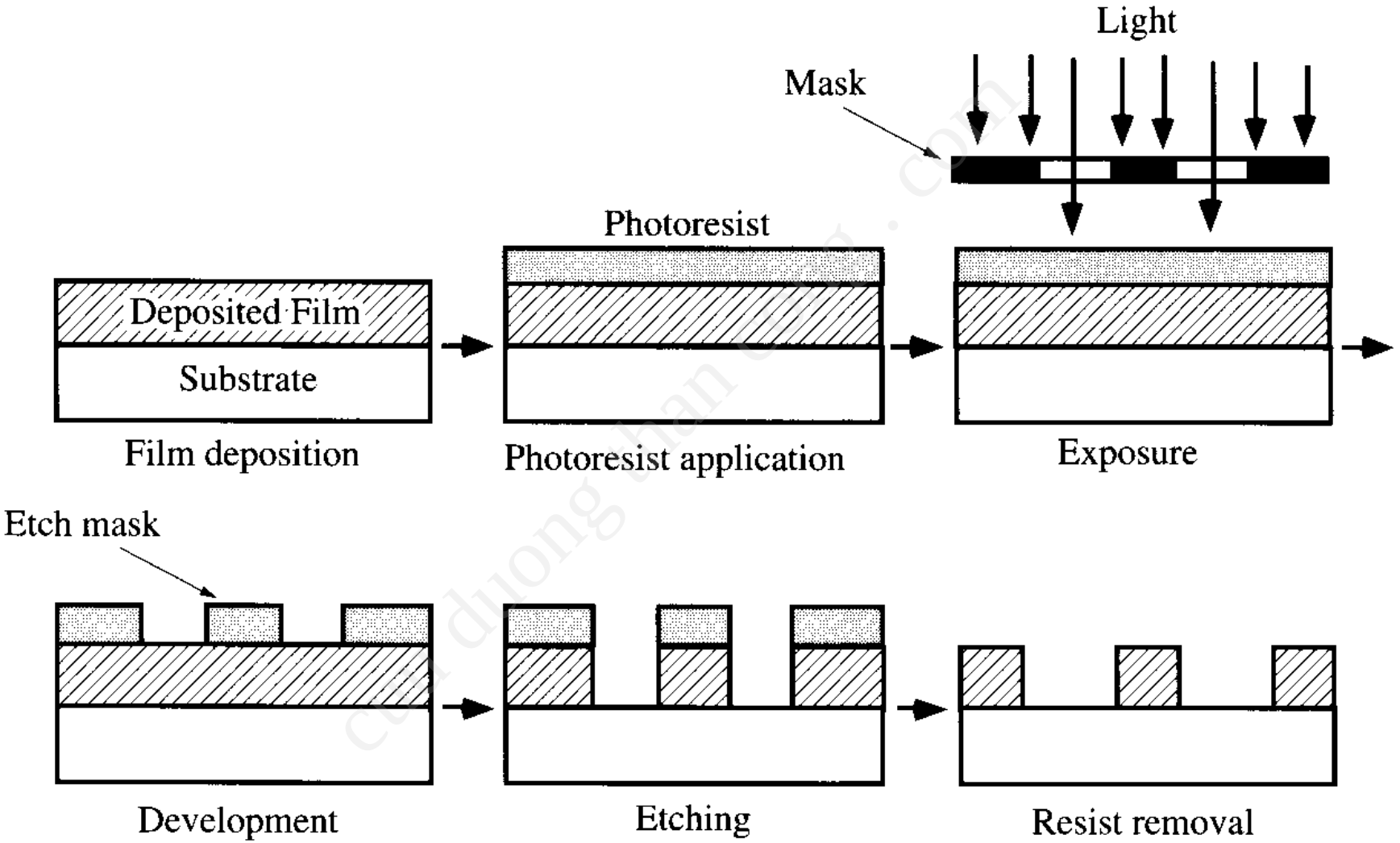
- The photoresist is selectively exposed to light by an optical lithography tool through a mask containing pattern information.

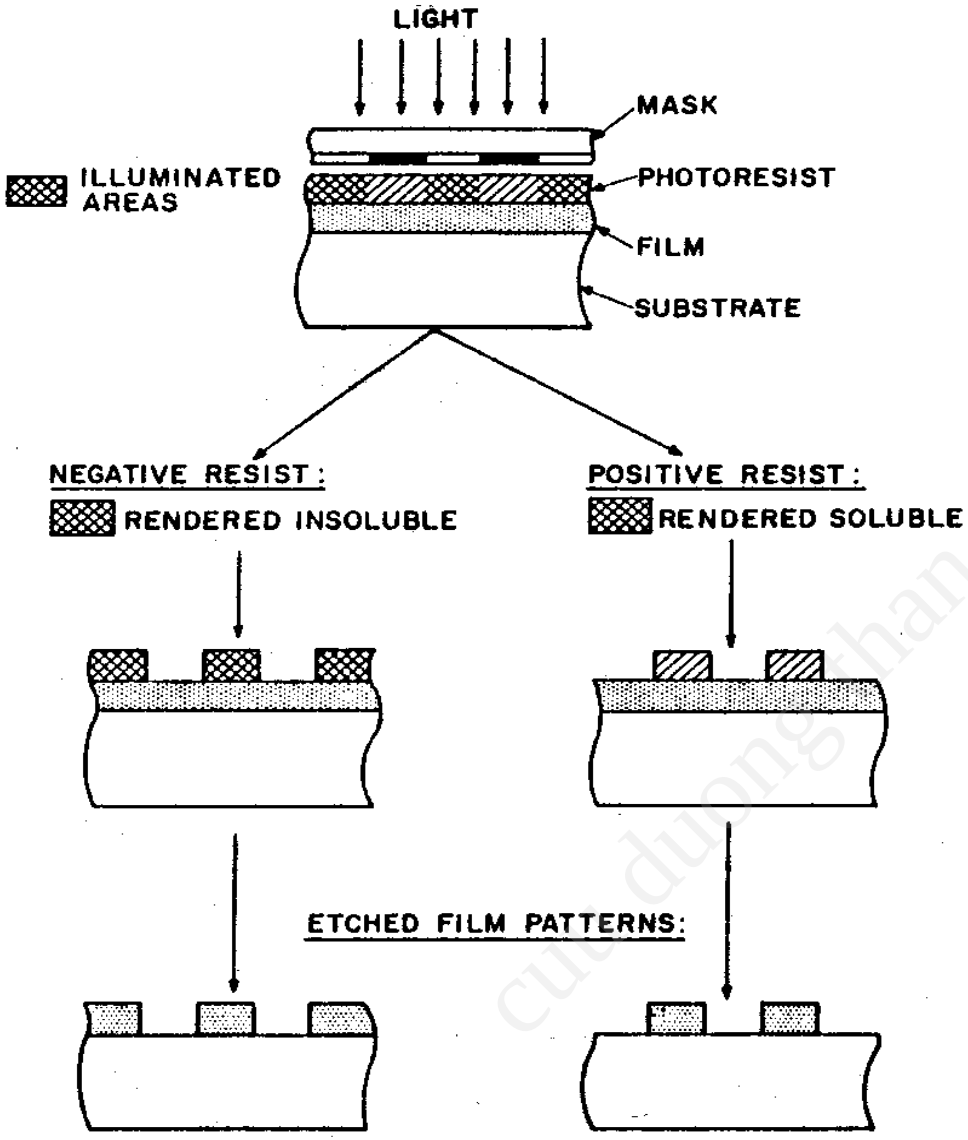
- The photoresist is developed to transfer the pattern information from the mask to the wafer.

- Key aspects to consider in photolithography technology

  A. Resolution
  B. Depth of focus
  C. Field size
  D. Overlay accuracy
  E. Throughput and defect density

Introduction to Lithography Process





- **Positive photoresist:**

The irradiated regions are soluble, a positive image of the mask is produced in the resist.

Positive photoresists are predominantly used in the IC industry because they have better resolution than negative photoresist.

- **Negative photoresist:**

The non-irradiated regions are dissolved by the developer, while the irradiated regions are hardened by cross-linking.

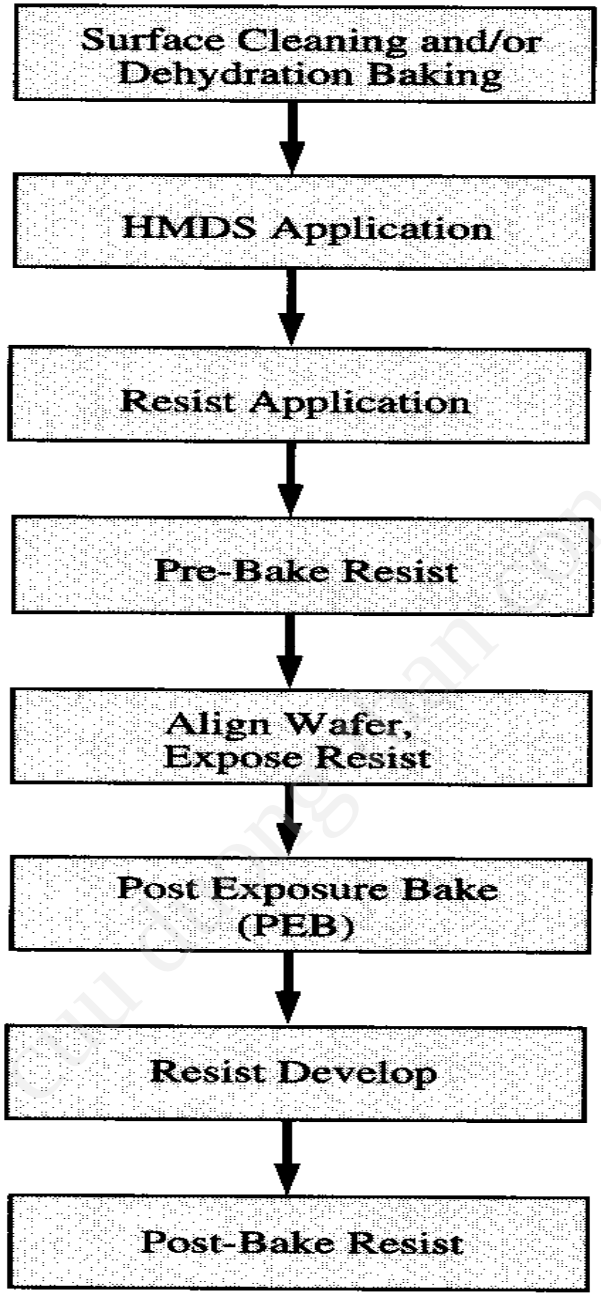
Optical photoresist consists of

A. **Matrix material (resin):** Serves as a binder and establishes the mechanical properties of the resist. It is inert to the incident imaging radiation. It determines other film properties such as thickness, flexibility and thermal flow stability.

B. **Sensitizer (inhibitor):** A photoactive compound (PAC). It provides the resist with its developer with resistance and radiation absorption ability.

C. **Solvent:** Keeps the resist in the liquid state until it is applied to the substrate being processed.

Photoresist Processing



Prepares surface for photoresist application

Adhesion promoter typically spun on the wafer or applied as a vapor

Resist spun on wafer, typically 3000-6000 rpm, forming an ≈ 1.0 µm resist layer

Typically 10 - 30 min @ 90 – 100 °C

Typically aligned at each exposure site, exposed at 150 mJ cm^{-2}

Sometimes used to minimize standing waves in resist Typically 10 min @ 100°C

Typically 30 – 60 sec @ room T using spray or puddle

Typically 10 – 30 min @ 100 - 140 °C

Key Parameters in Photolithography

A. Resolution

B. Depth of focus

C. Field size

D. Overlay accuracy

E. Throughput

F. Defect density

(1) Numerical Aperture

The patterns interfere with each other to produce intensity pattern on the screen in the following way,

$$d \sin\theta_N = N\lambda$$

where *N* is the order of diffraction, *d* is the distance from the slit to the plane, and θ_N is the angle at which the diffraction pattern exists. In optical projection systems, the major factor that limits the resolution capability is the physical design of the objective lens and its numerical aperture (NA). The numerical aperture is a measure of lens' capability to collect diffracted light from an object (for example, photomask) and project it onto the wafer. It is defined by

$$NA = n \sin\alpha$$

where *n* is the refractive index of air, and 2α equals the acceptance angle of the lens.

(2) Resolution Capability

The resolution of a lens depends on the wavelength, the degree of coherence of the incident light and the *NA* of the lens. The criterion can be expressed as

$$2b = 0.61\lambda / NA$$

where *2b* is the separation distance between two images and λ is the wavelength of the light source.

(3) Depth of Focus

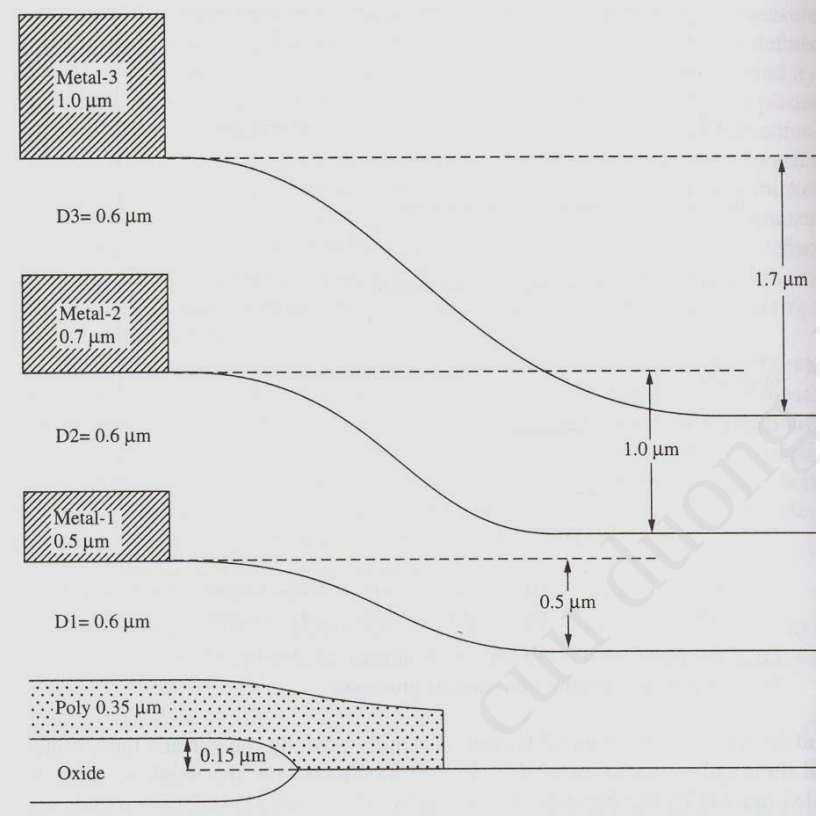
As shown above, the high *NA* can give rise to better resolution. But the depth of focus is inversely proportional to its square. That is,

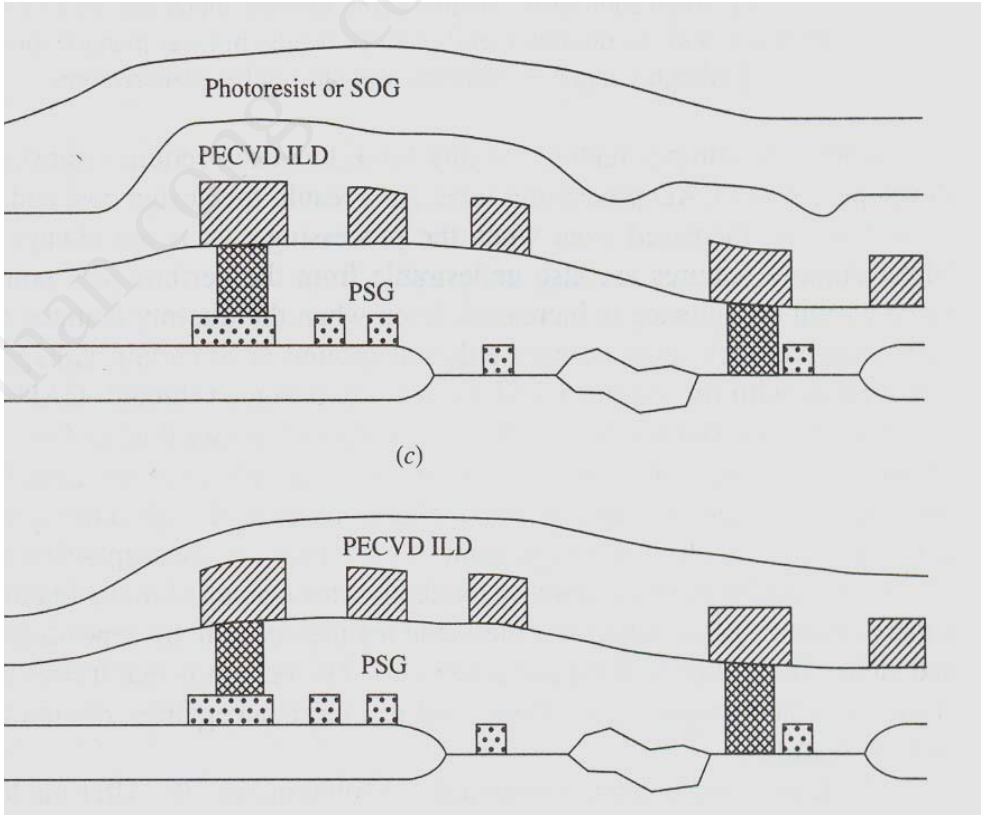
$$\sigma = \lambda / (NA)^2$$

In order to print a pattern on large wafers, consecutive exposures of step-and-repeat must be conducted. The machine for this step-and-repeat exposure is called Stepper.

CHALLENGE IN SMALL DEPTH OF FOCUS:
PLANARIZATION IN INTERCONNECTS

Buildup of topography in multi-level metallization requires an extensive level of planarization (etch back and CMP)





Optical printing methods

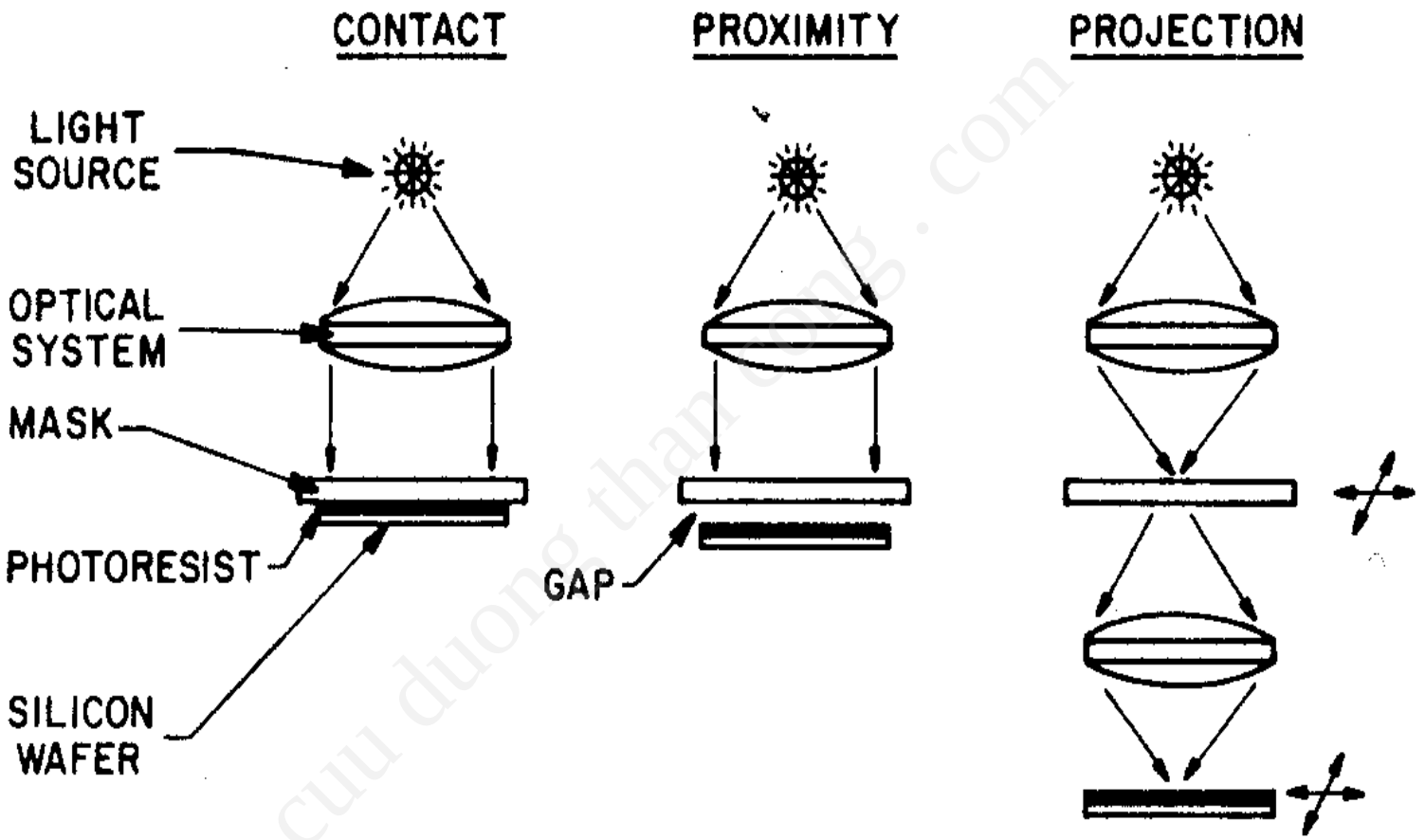
(1) Contact Printing and Proximity Printing

In contact printing, diffraction effects can be minimized, but pattern quality is not good because of hard contact between the mask and the wafer. On the other hand, in proximity printing, the number of defects can be reduced, but the pattern resolution is degraded by diffraction effects. The proximity printing system is used to generate patterns larger than a few mm.

(2) Projection Printing

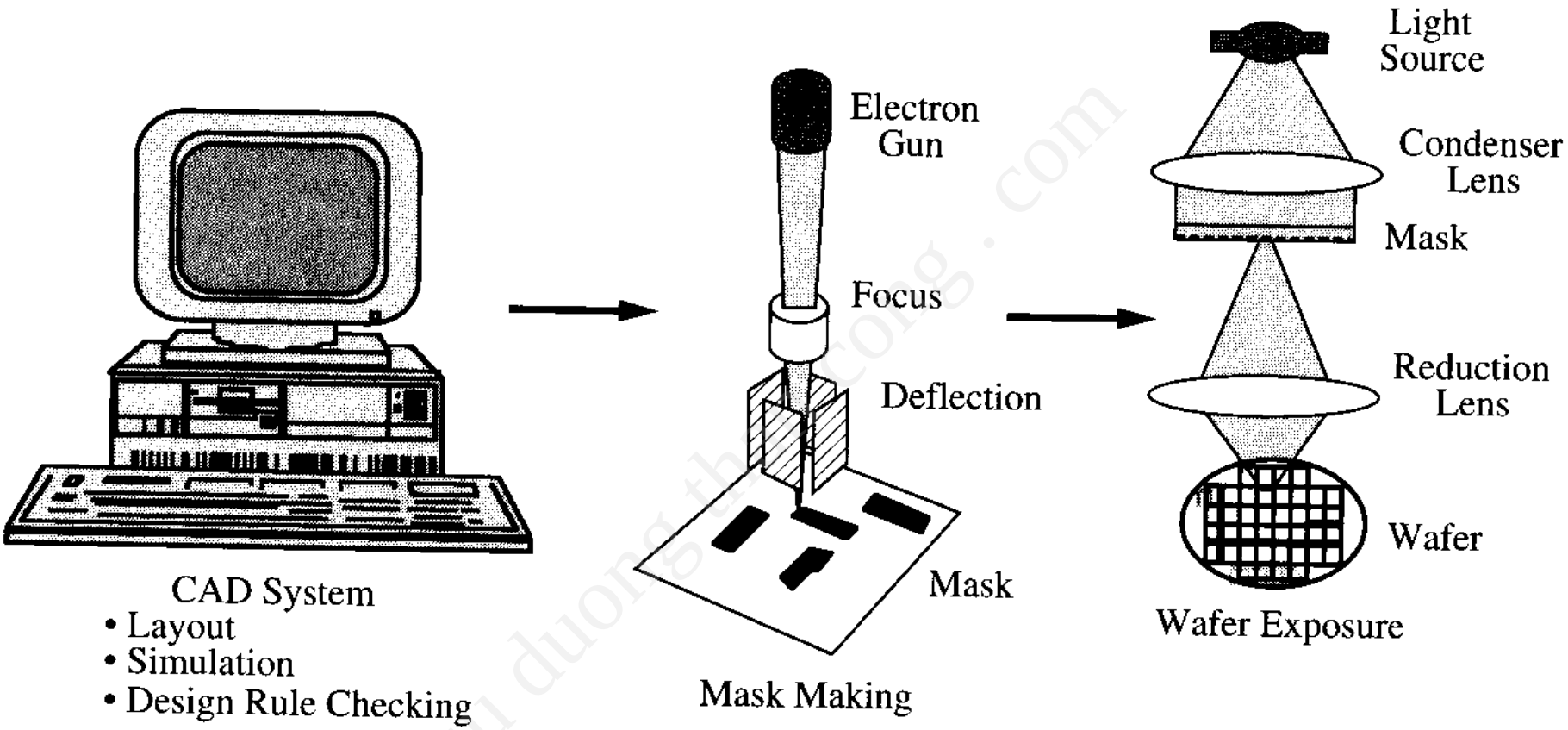
Currently, projection printing is predominantly used for high resolution integrated circuit processes. The mask patterns are reduced to 4 – 5 times by the projection to the wafer. The resolution of the most advanced system is about 0.1 μm and it is generally limited by diffraction effects.

Optical printing methods



Q) What are the advantages and disadvantages of each method?

Mask fabrication



Masks

The patterns of various layers are designed by computer aided design (CAD). The information of each layer is transferred to the mask generation tool using an electron beam or a laser. Defects on the mask should be repaired, because they are transferred to every wafer. To prevent particles from being transferred to the wafer, a thin transparent membrane called a pellicle is used to cover the patterned side of the mask with a distance about 100 mm. Since the depth of focus of advanced lithography tools is only a few mm, the particles on the pellicle are not printed on the wafer.

Q) How can you make patterns on a mask?

Q) How can you maintain a particle-free mask?

Q) Explain the principle of pellicle.

3. Etching Technology

A. PLASMA ETCHING BASIC

- PLASMA ETCHING MECHANISMS
- PLASMA ETCHING MODELS
- ETCHING OF Si, SiO2, AND METAL

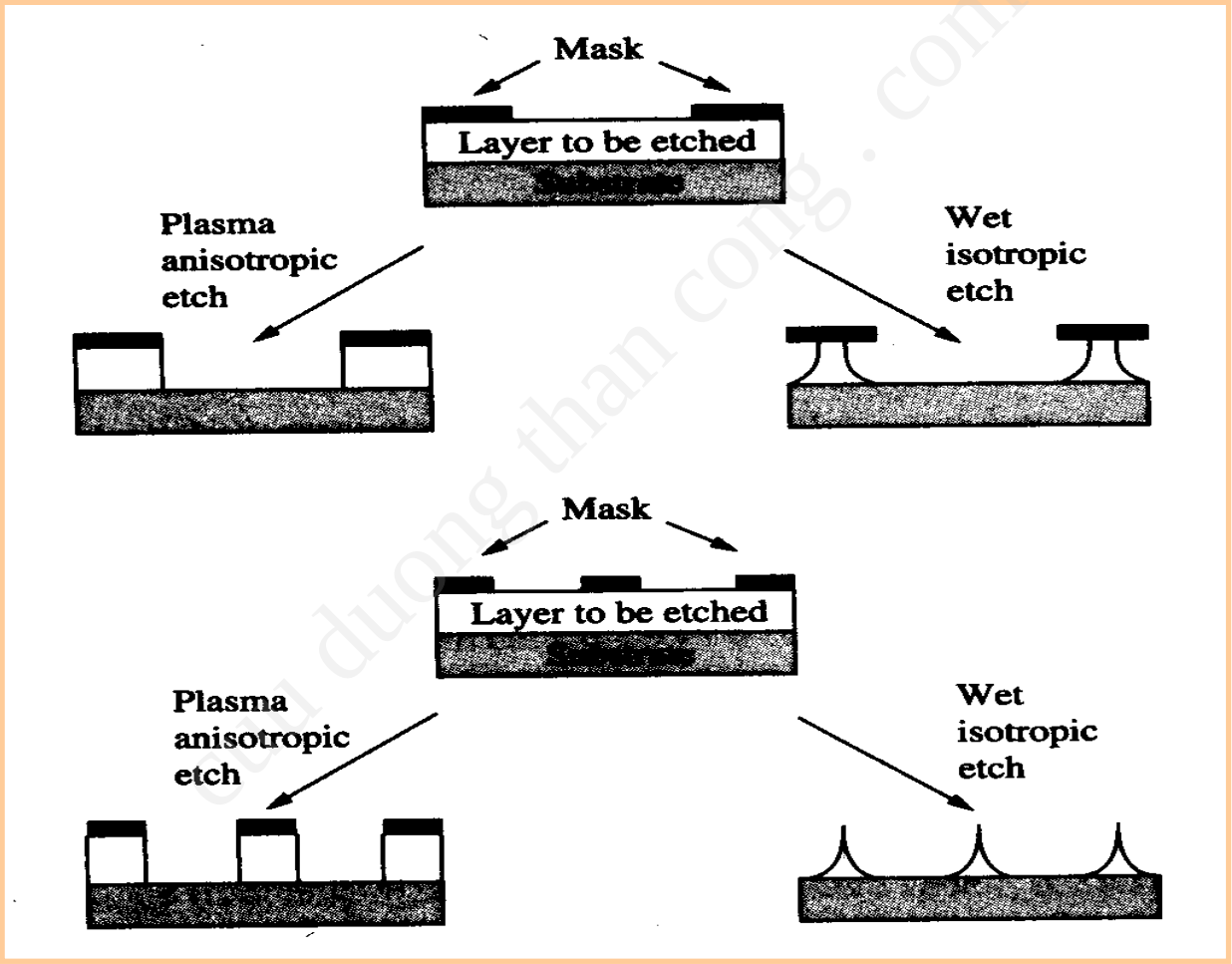
B. ETCHING PROCESS VARIABLES

C. ETCHING PROCESS REQUIREMENTS

D. OTHER ISSUES IN PLASMA ETCHING

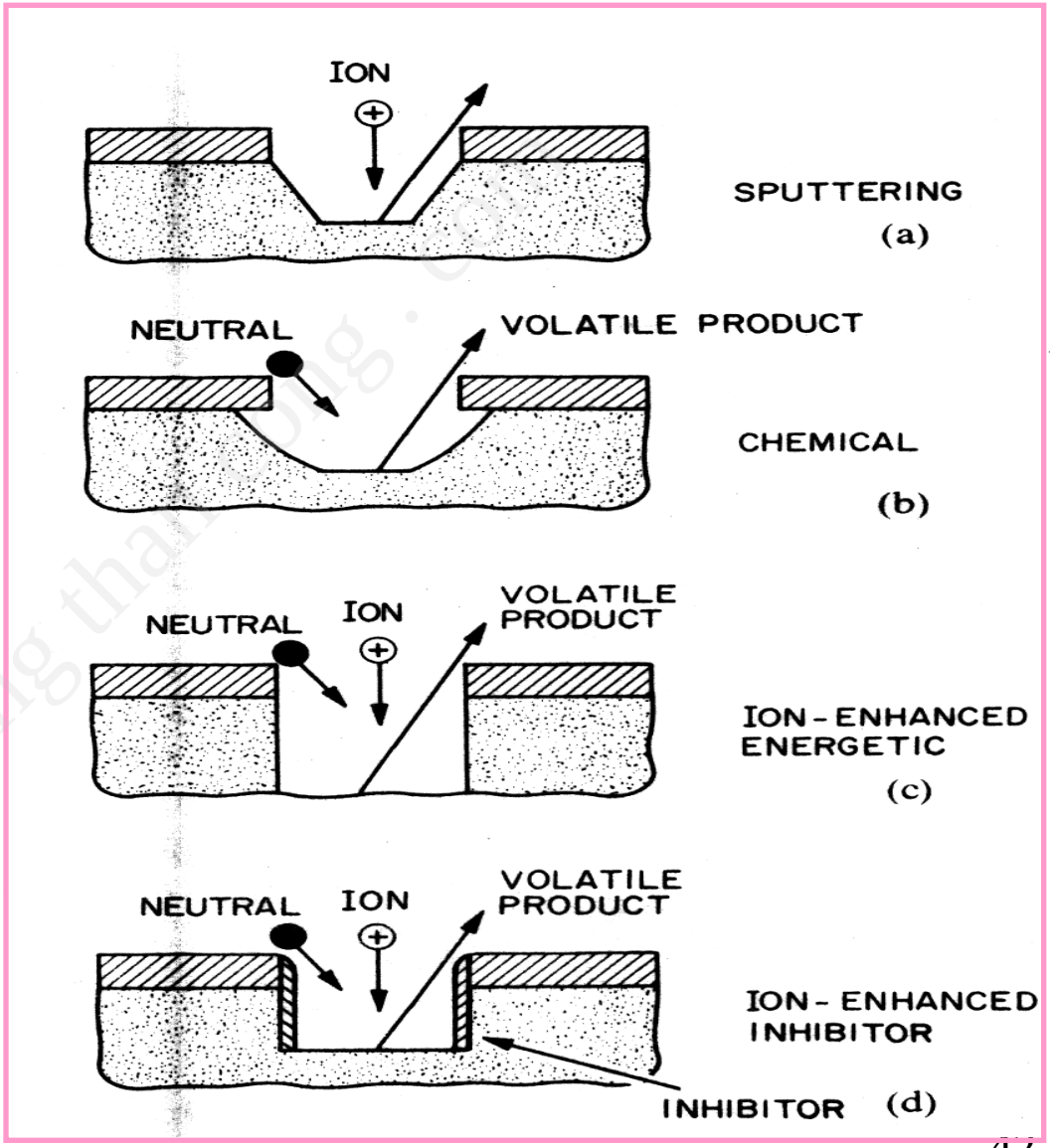
PLASMA ETCHING MECHANISMS

Difference in Plasma Etching and Wet Etching



PLASMA ETCHING MECHANISMS

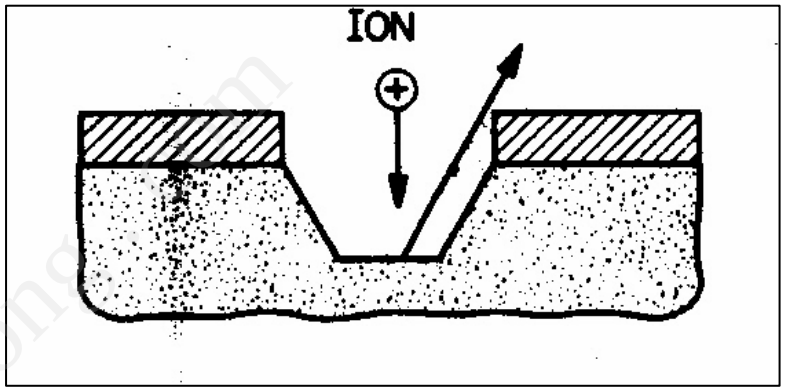
Four Different Plasma Etching Mechanisms



PLASMA ETCHING MECHANISMS

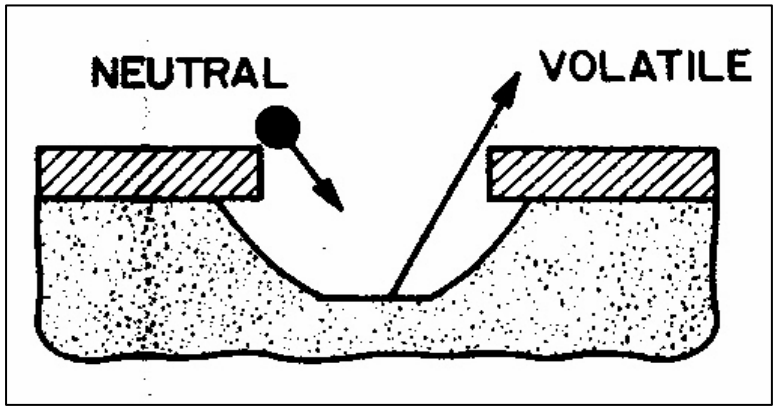
Sputtering:

- Positive ions are accelerated across the sheath with high kinetic energy.
- Directional but has low selectivity.



Chemical etching:

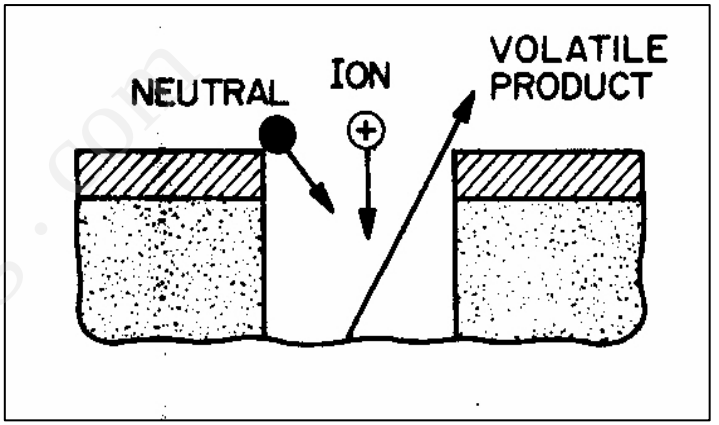
- Active species from the gas phase encounter the surface and react to form volatile product.
- Non-volatile reaction product would remain on the surface and impede further etching.
- Non-directional but can have high selectivity.



PLASMA ETCHING MECHANISMS

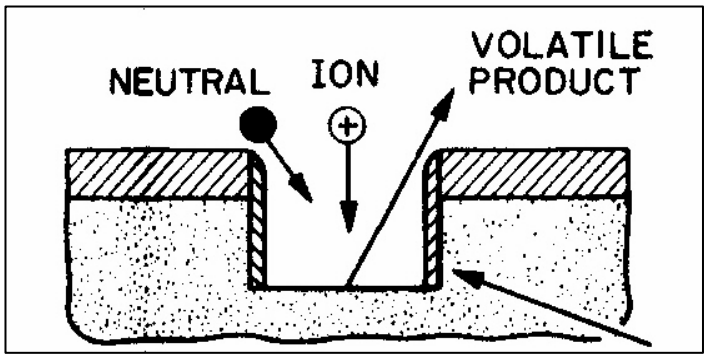
Ion-enhanced directional etching:

- Where neutral species cause little etching, ion bombardment can make the substrate more reactive, the effects of radicals and ions can be synergistic to enhance etching rate.
- Ions accelerated across the plasma sheath edge strike the surface vertically with kinetic energy, causing directional etching.



Inhibitor-driven ion-assisted etching:

- Etching by neutral radicals is spontaneous so ion bombardment does not cause etching reaction.
- Ions sputter off substrate materials to form inhibitor-films on the sidewall, resulting in anisotropic etching.



PLASMA ETCHING MODELS

Various steps of ion-assisted etching of silicon in chlorine plasmas are illustrated as follows:

A. **Ionization:** $e + Cl, Cl_2 \rightarrow Cl^+, Cl_2^+ + 2e$

B. **Dissociation:** $e + Cl_2 \rightarrow 2Cl + 2e$

C. **Adsorption:** $Cl, Cl_2 \rightarrow Si_{surf}\text{-}nCl$

D. **Product formation:** $Si\text{-}nCl \rightarrow SiCl_x\ (adsorbed)$

E. **Product desorption:** $SiCl_x\ (adsorbed) \rightarrow SiCl_x\ (gas)$

PLASMA ETCHING MODELS (F/C)

$$Si + CF_4 = SiF_4\uparrow + C$$

$$SiO_2 + CF_4 = SiF_4\uparrow + CO_2\uparrow$$

F/C ratio = ?

- F for etching and C for polymerization

$$H + F = HF$$

$$C + O_2 = CO\uparrow \text{ or } CO_2\uparrow$$

Q) Is CF_4 reactive ?

PLASMA ETCHING MODELS (F/C)

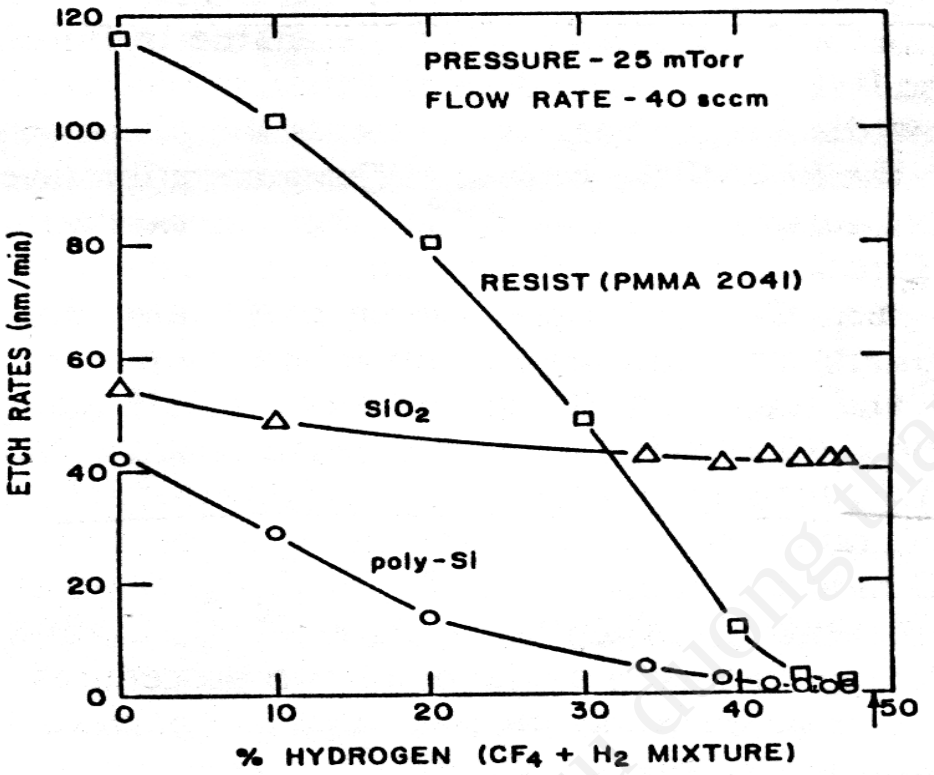
(1) Increasing the F/C ratio increases Si etching rates and decreasing the F/C ratio lowers them. The etching rates of SiO_2, Si_3N_4, Ti, and W are affected similarly by the F/C ratio.

(2) F/C ratio of CF_4 gas is four. As the etching of Si is carried out and the etch products SiF_4 are generated, and F/C ratio decreases.

(3) Addition of H_2 to CF_4 forms HF, thereby the F/C ratio and the etching rate are reduced. This effect is also observed for CHF_3 and C_3F_8 where the F/C ratio is lower than 4.

(4) Addition of O_2 can increase the F/C ratio, because oxygen tends to consume more carbon than fluorine by forming CO or CO_2.

PLASMA ETCHING MODELS (F/C)



The high selectivity of etching rates of SiO_2 versus Si in CF_4+H_2 plasmas can be explained by the F/C model.

- **Although the F/C ratio is less than 4 due to the formation of HF, the SiO_2 can compensate for the decreased F/C ratio since it generates oxygen. Etching rate of SiO_2 does not decrease significantly with the addition of H_2.**

- **Etching rate of Si decreases significantly as the F/C ratio is lowered with the addition of H_2.**

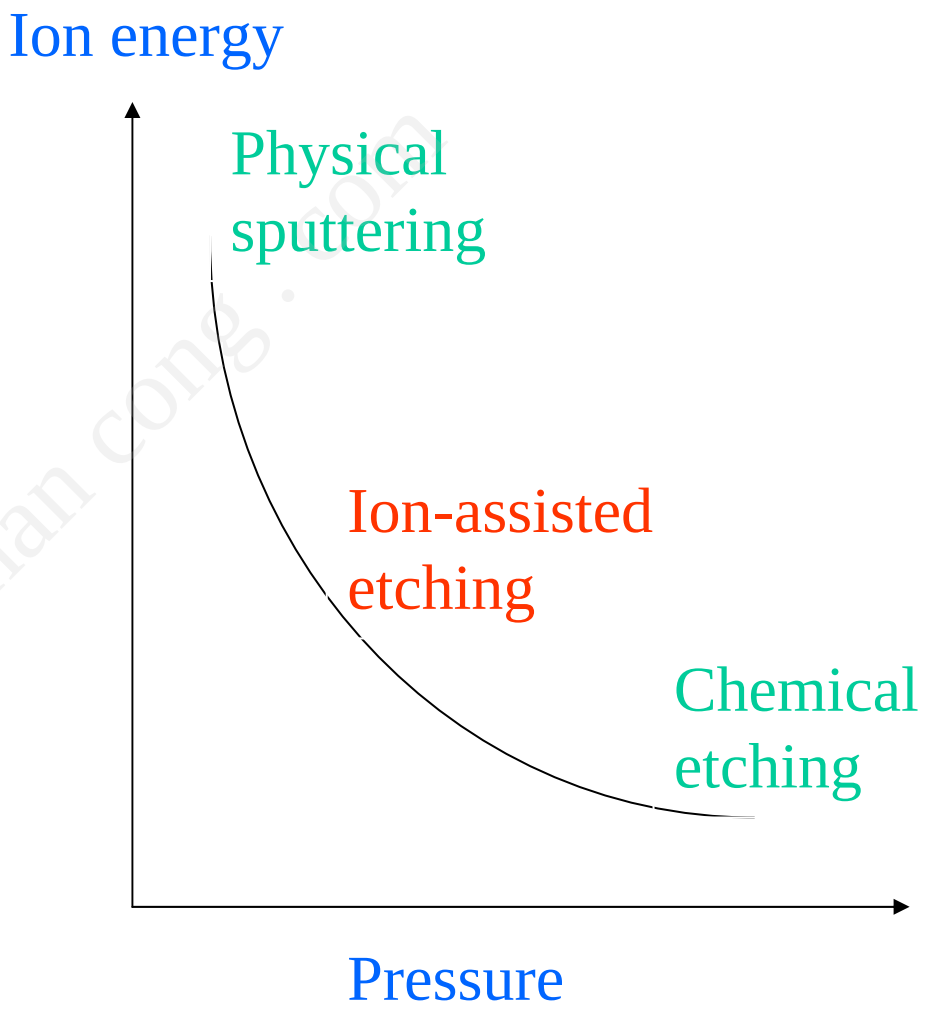
Pressure Effect

(1) Sheath potential and ion energy bombarding the surface

(2) Electron temperature and electron energy distribution

(3) Ionization ratio and collision frequency

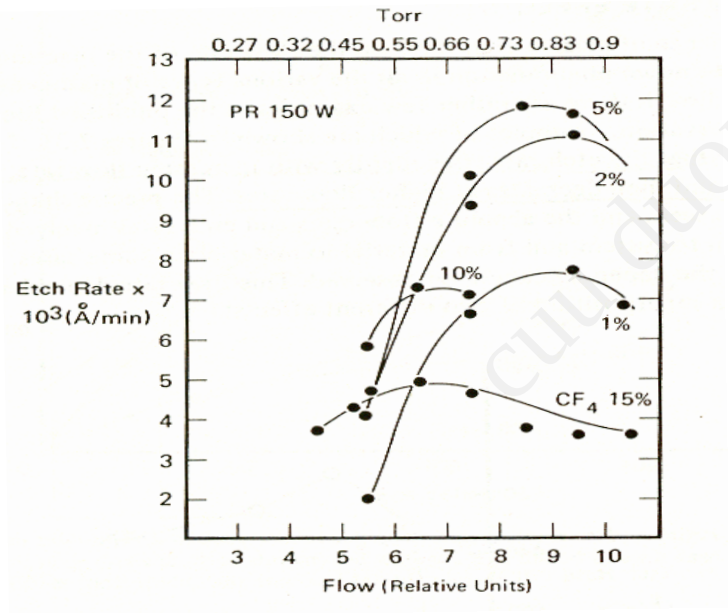
(4) Flux of ions and radical species to the surface

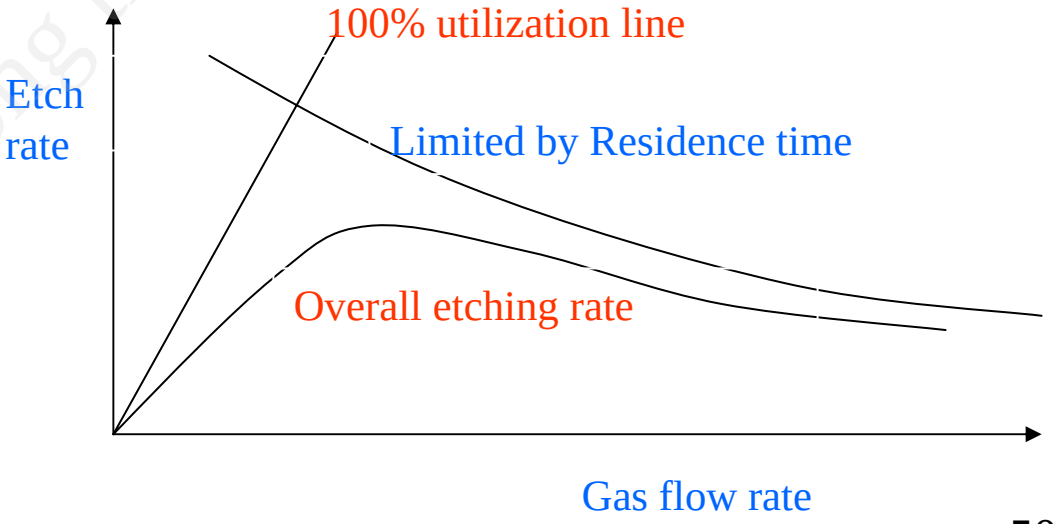


ETCHING PROCESS VARIABLES (FLOW RATE)

Overall flow rate effect

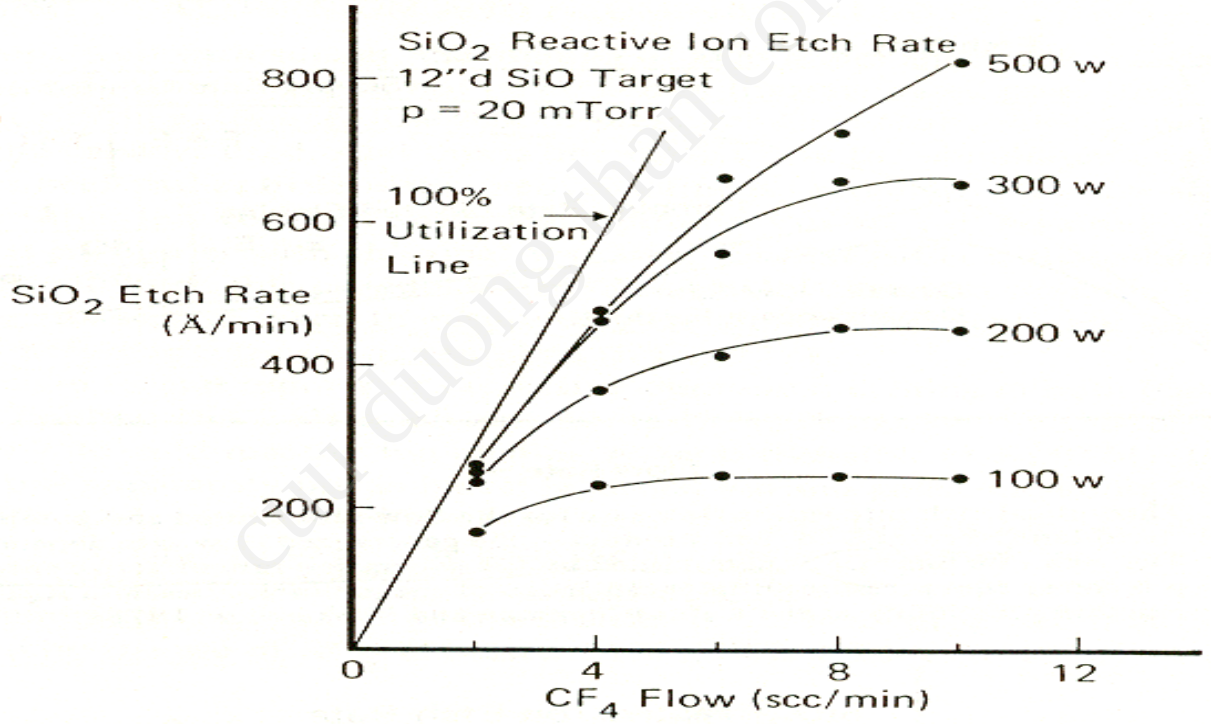
- When pumping speed or flow rate increases to a certain point, residence time of reactive gases becomes too short to etch the substrate.
- Lack of reactant species can lower the utilization factor. This can be minimized by increasing RF power to increase the generation rate of reactive species
- Overall etching rate will be determined by lack of reactant gases at the low flow rate regime and by insufficient residence time of reactant gases at the high flow rate regime.





ETCHING PROCESS VARIABLES (FLOW RATE)

If utilization factor is high, reaction products can affect gas components of the etching plasma. This is often observed in the low flow regime. The following figures show the consumption of the etching gas under the condition with high utilization factor.



ETCHING PROCESS VARIABLES (TEMPERATURE)

- We should be able to differentiate the gas temperature from the surface temperature. The gas temperature is not easily controllable because it depends on power input and heat transfer.

- Instead, the surface temperature is used more practically, because in the processing plasmas the thermal boundary layer (the distance in which the gas temperature is maintained close to the wall temperature due to heat transfer) is much thicker than the mean free path.

- Etching properties such as chemical reaction rates, selectivity, surface morphology and degradation of photo-resist can be affected by the temperature.

- When the etching rates are controlled by the reaction which is a function of the temperature, it can be represented by Arrhenius Equation in the form of $R_e = A \exp(-E_a / kT)$

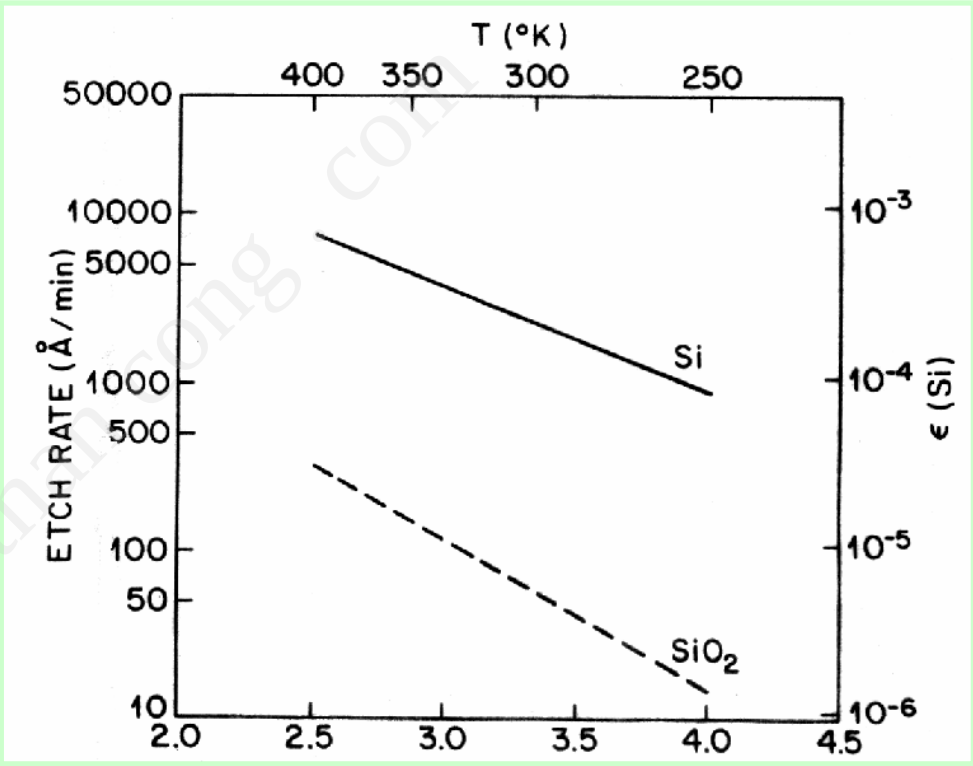
ETCHING PROCESS VARIABLES (TEMPERATURE)

Q) From the Arrhenius plot of Si and SiO_2 etching reactions in a fluorine containing plasma,

(a) Estimate the activation energy for overall etching reactions of Si and SiO_2

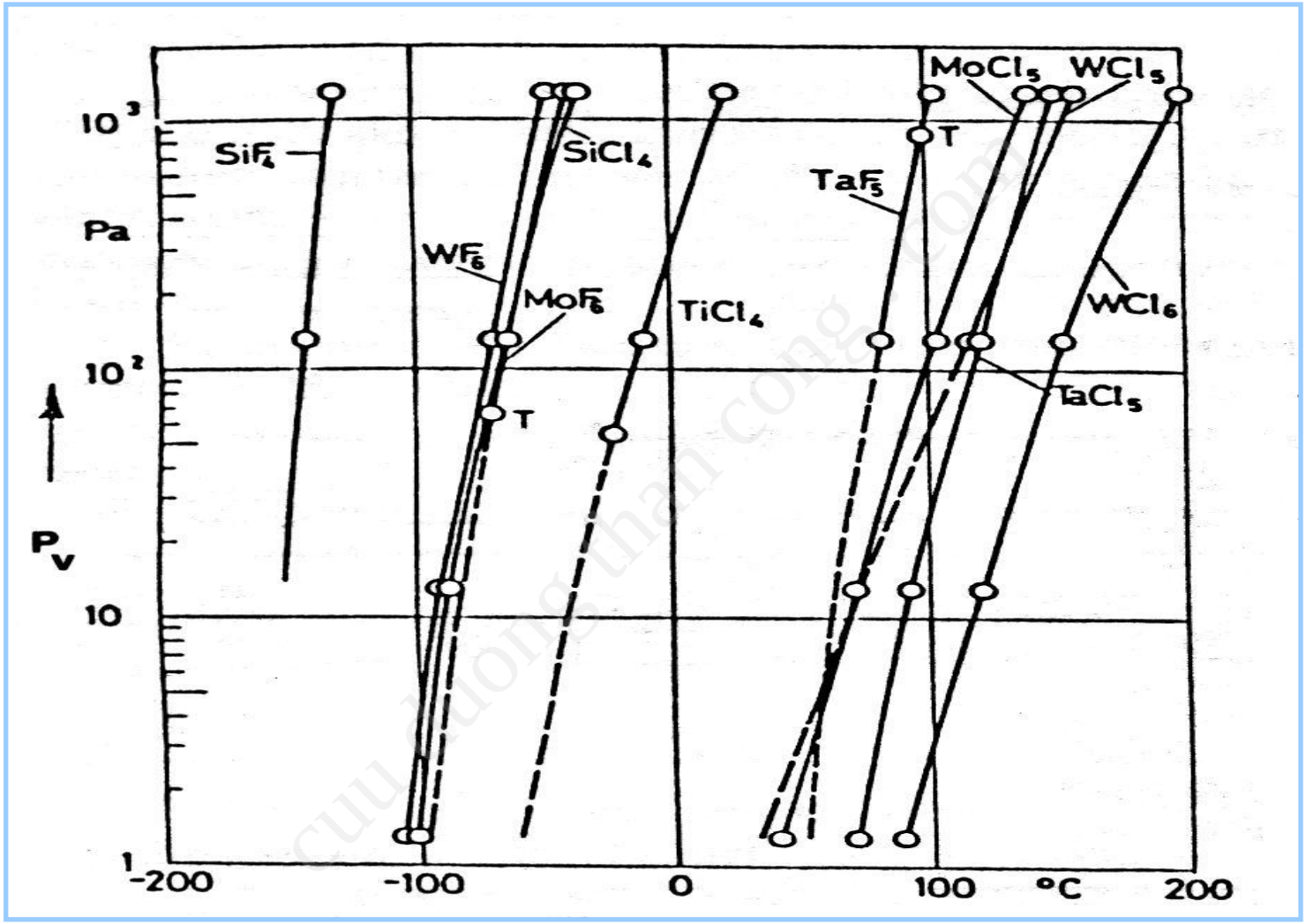
(b) Find complete Arrhenius equations,

(c) Plot the etching selectivities between Si and SiO_2 as a function of temperature.



$$R_e = A\exp(-E_a / kT)$$

ETCHING PROCESS VARIABLES (TEMPERATURE AND VOLATILITY)



Q) Based on these results, explain why fluorine-based gases are preferred to chlorine-based gases for Si etching?

ETCHING PROCESS REQUIREMENTS

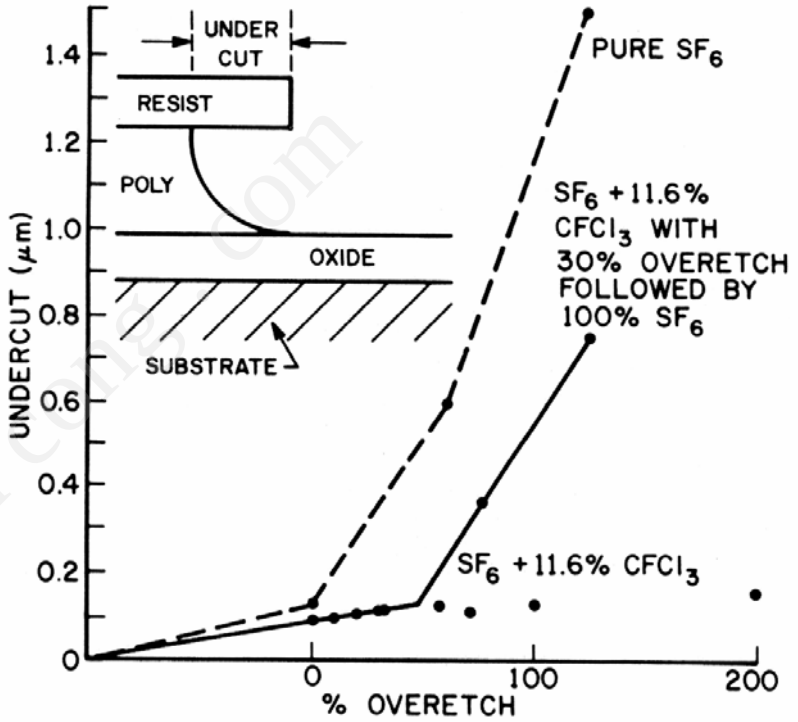
Etch rate (Re)

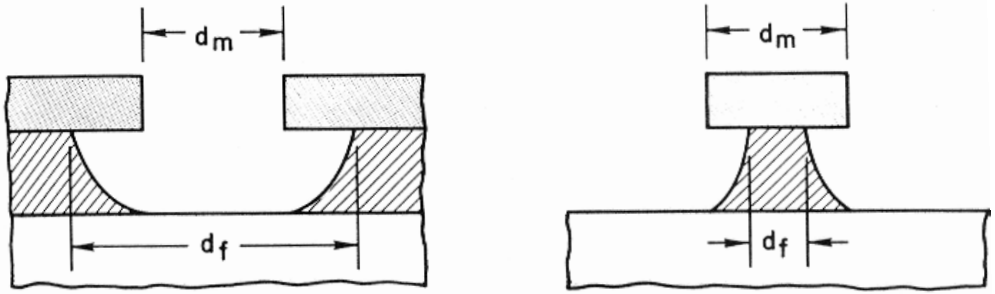
- **Overetch ratio = (Additional etch time / target etch time) x 100%**

- **Uniformity = $[(R_{max} - R_{min}) / (2R_{ave})] \times 100\%$**

- **Anisotropy = $1 - R_h/R_v$**

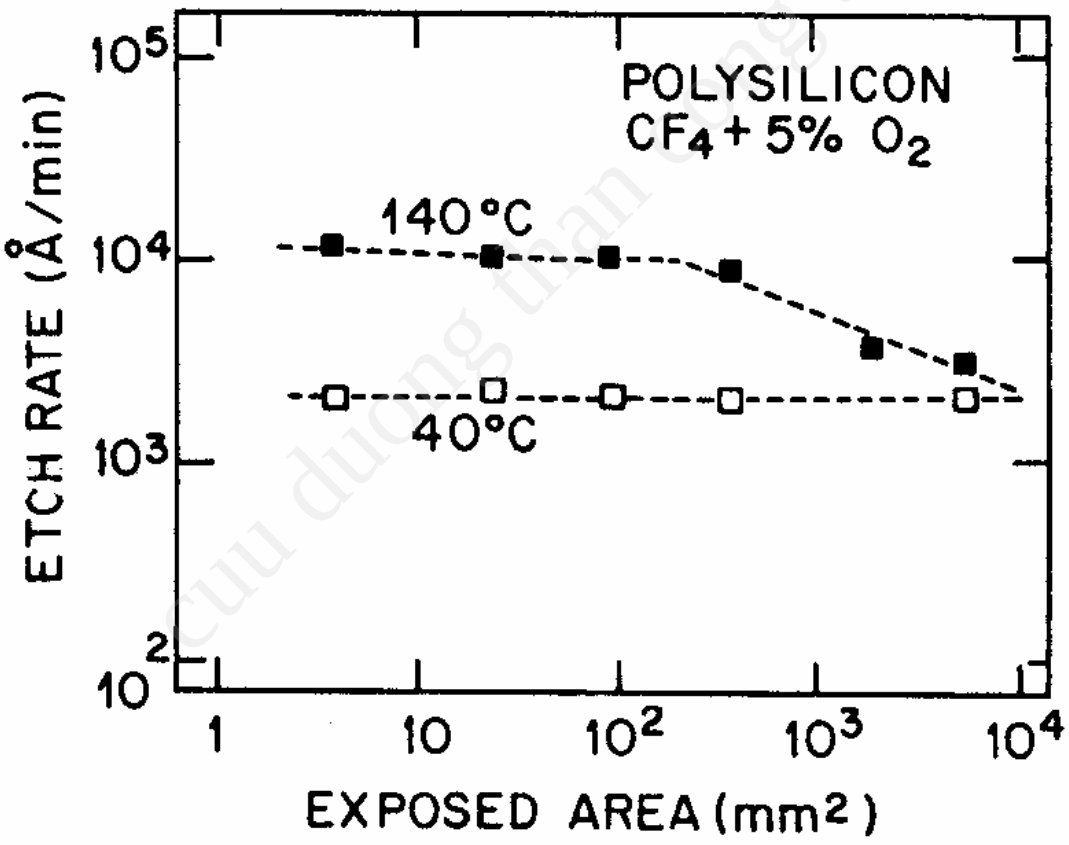
- **Selectivity = R_f/R_s**





ETCHING PROCESS REQUIREMENTS (LOADING)

Where etching rate is controlled by the transport of etchant gases. ie, the amount of available gases on the wafer surface, the etching rate decreases as the open area on the wafer surface increases. This is known as Loading Effect.



ETCHING PROCESS REQUIREMENTS (MICROLOADING)

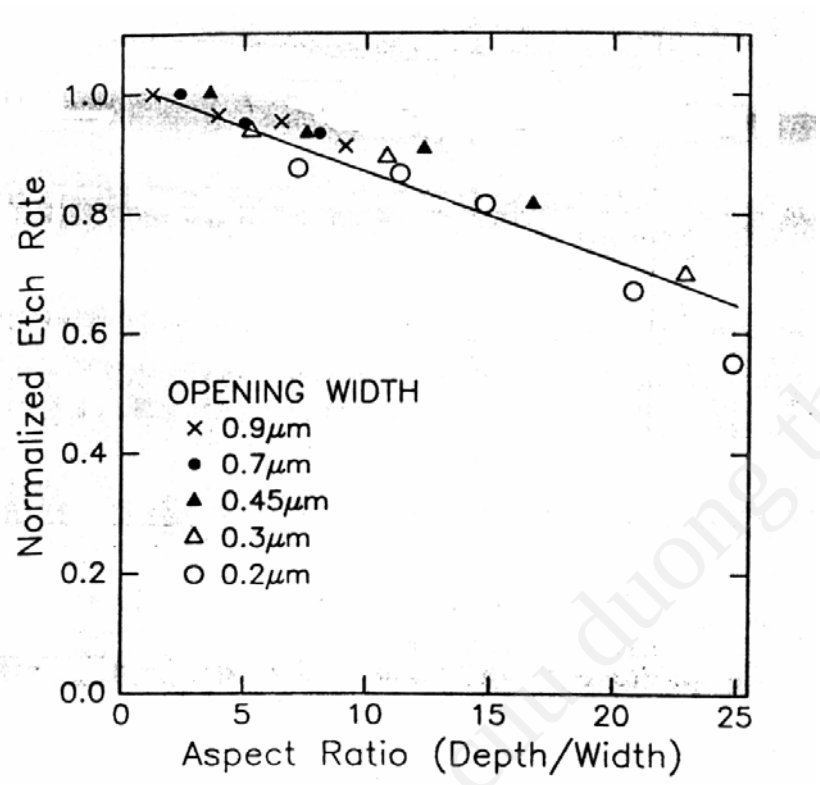
MICROSCOPIC UNIFORMITY IN ETCHING

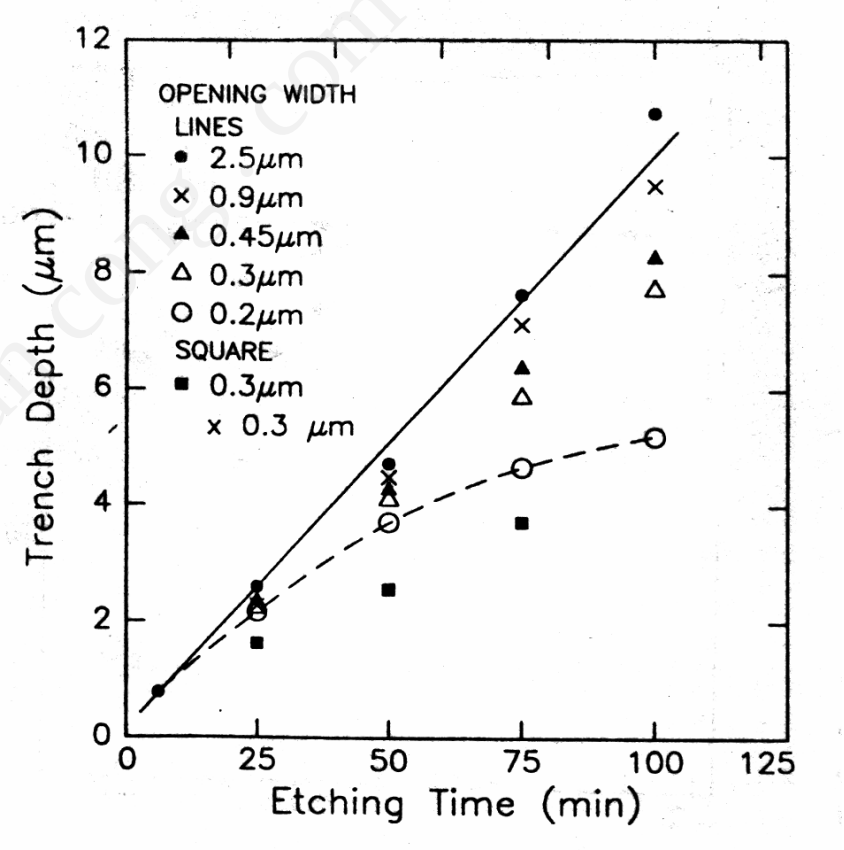
- It is differently named as
  RIE-lag,
  micro-loading,
  aspect-ratio dependent etching (ARDE), and
  pattern dependent etching.

- Defined as a phenomenon where **the etching rates in the small patterns are either lower or higher than the etching rates in the open area,** it can be understood as a phenomenon where the etching rates change as etching is carried out and the aspect ratio of structures becomes higher.

ETCHING PROCESS REQUIREMENTS (MICROLOADING)

MICROSCOPIC NON-UNIFORMITY IN ETCHING





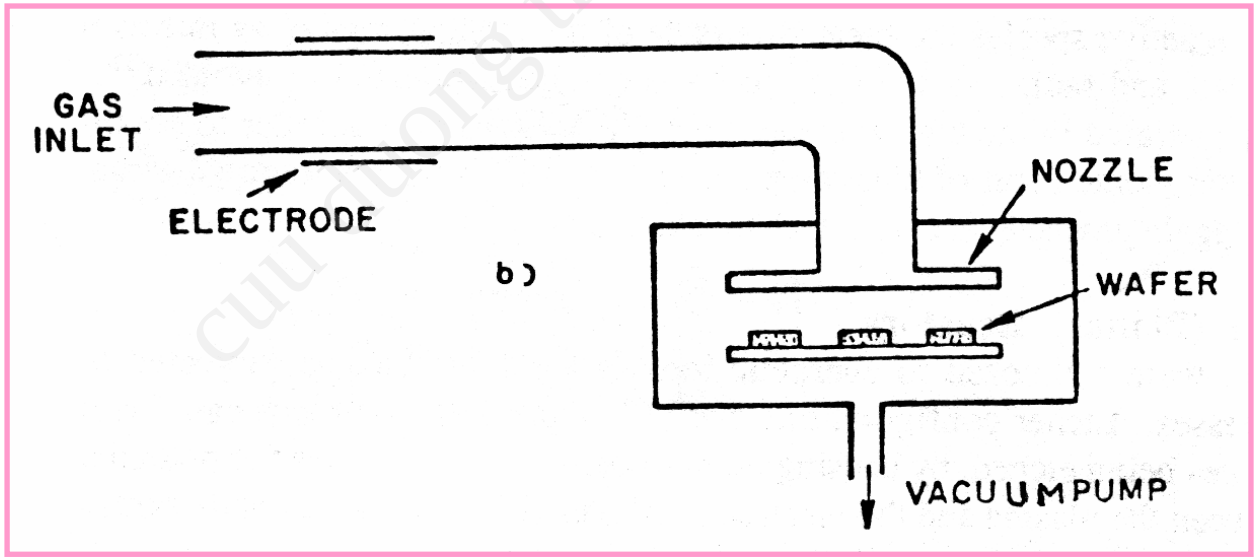
OTHER ISSUES IN PLASMA ETCHING

PHOTO-RESIST STRIPPING (ASHING)

A. Oxygen radicals generated in oxygen plasmas can attack organic photo-resist materials to break polymer chains and form volatile products CO, CO_2 and H_2O.

B. Stripping rates of photo-resist increase with the increase of the oxygen concentration and temperature. Processing temperature is above the glass transition temperature, T_g.

C. Exposure of device structures to the plasma during photo-resist stripping can cause electrical damage and charging to the devices. Downstream plasma systems are widely used to avoid these problems.



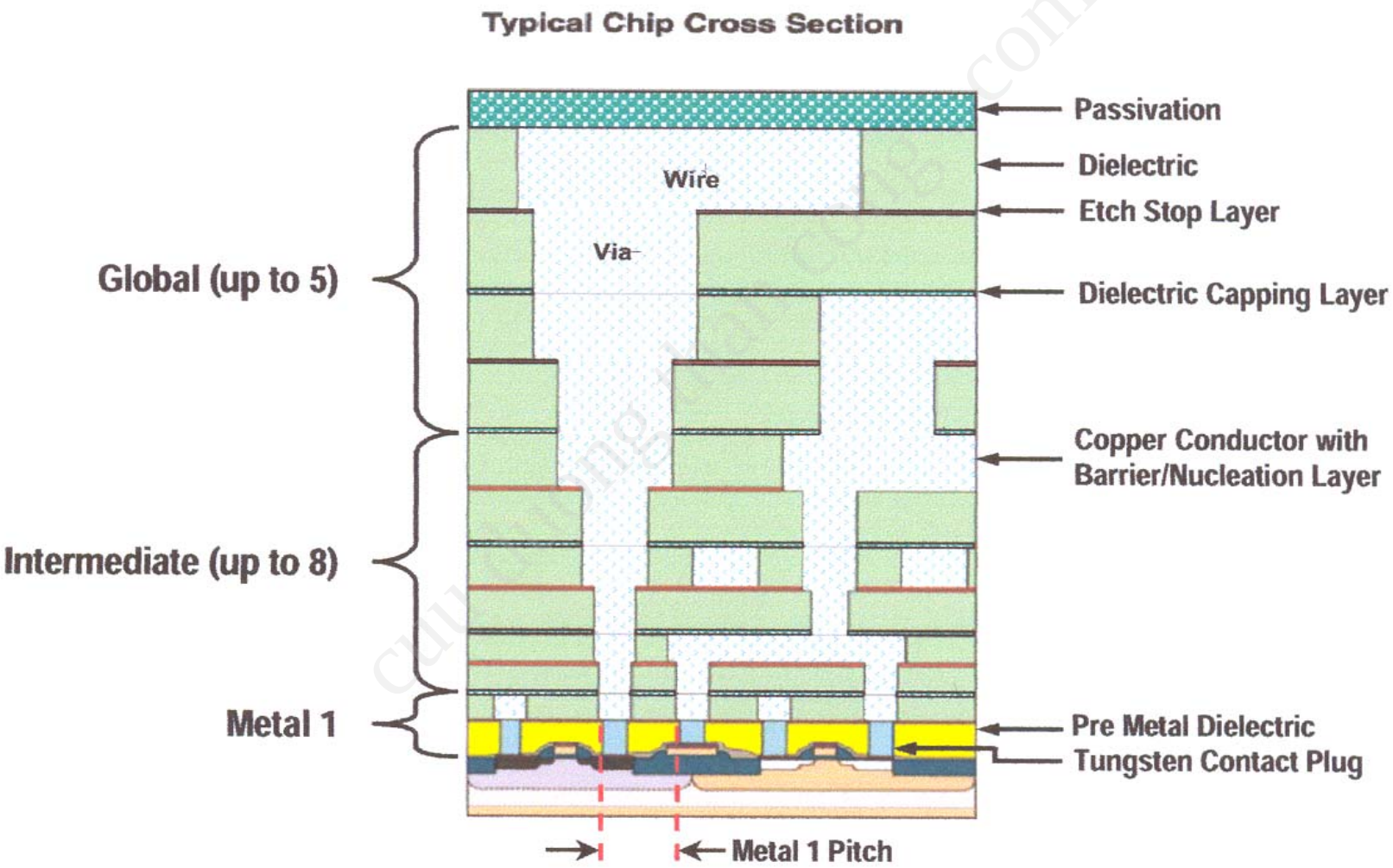
4. Interconnects

A. Introduction to interconnects

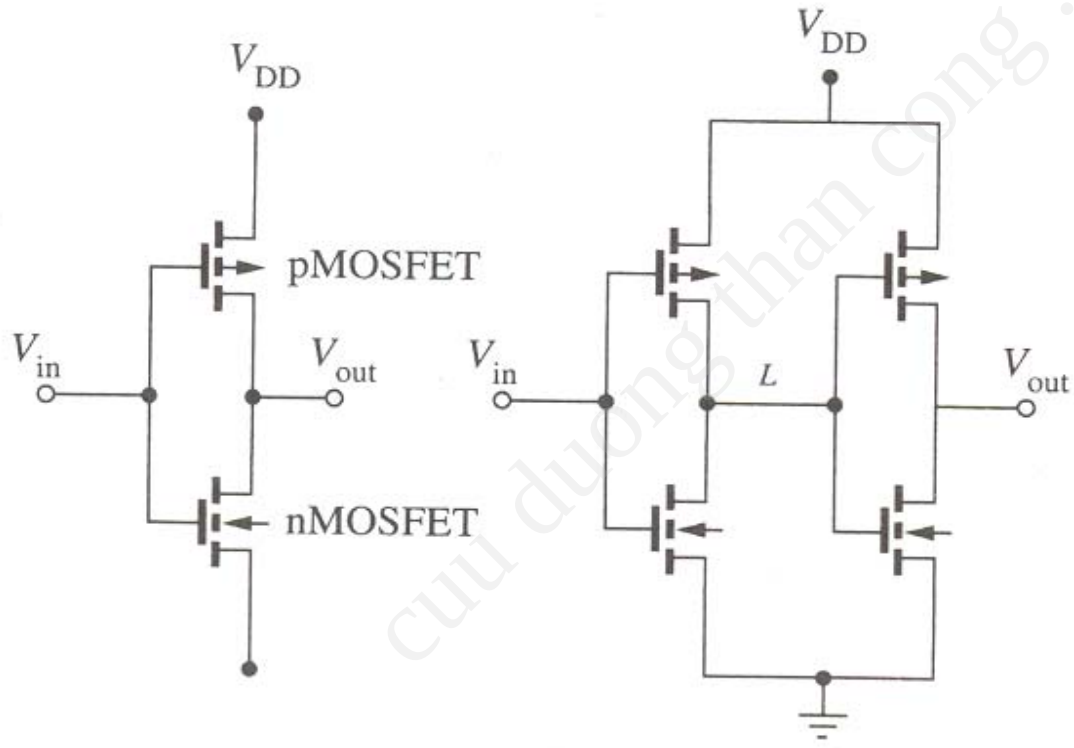
B. RC time delay

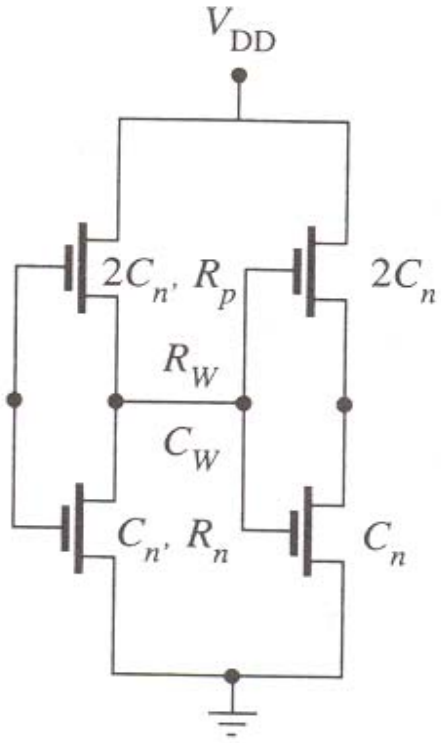
C. Materials in interconnects

- Global interconnects and multilevel metallization



- Local interconnect materials and processes
(Local interconnects in CMOS)

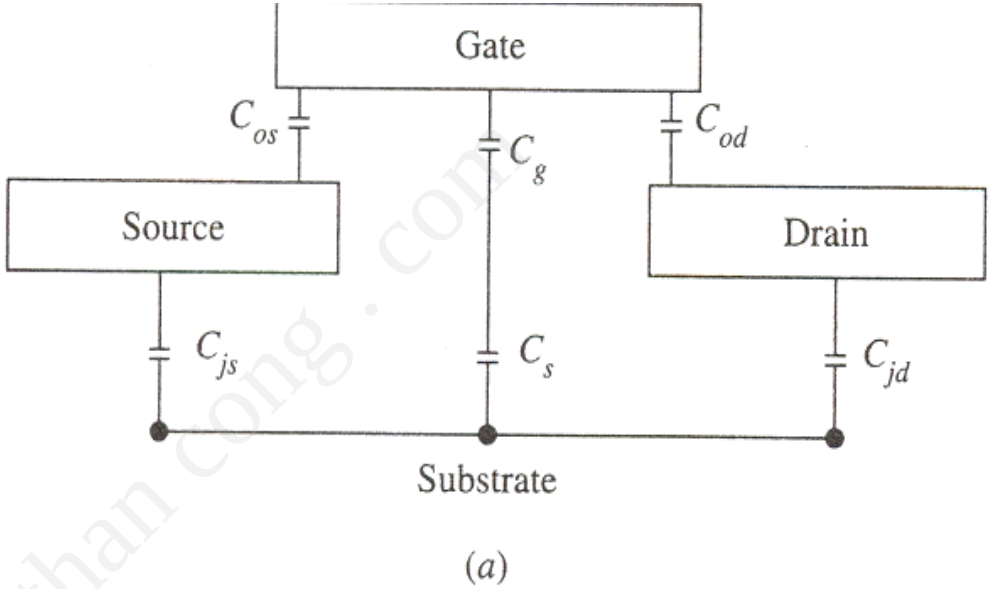




RC time delay

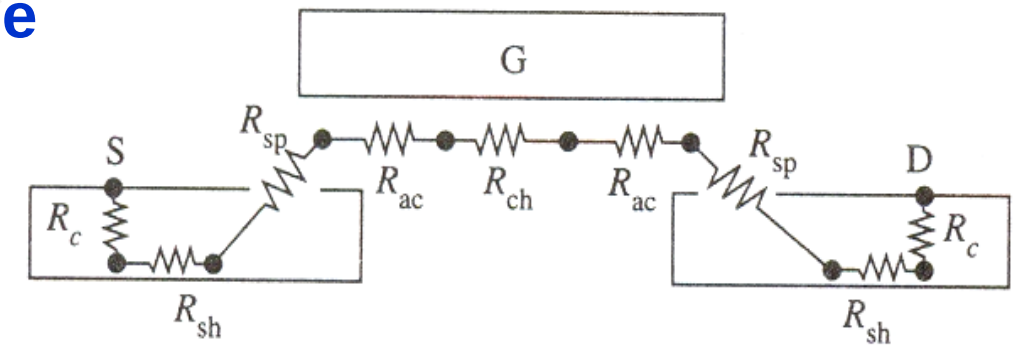
Intrinsic switching speed:

$$t = C_g V / I_{d,sat}$$



(a)

Parasitic capacitance and parasitic resistance



(b)

RC time delay is defined in terms of the circuit response which is given by

$$V_{out} = V_{\max}\left[1 - \exp\left(\frac{-t}{RC}\right)\right]$$

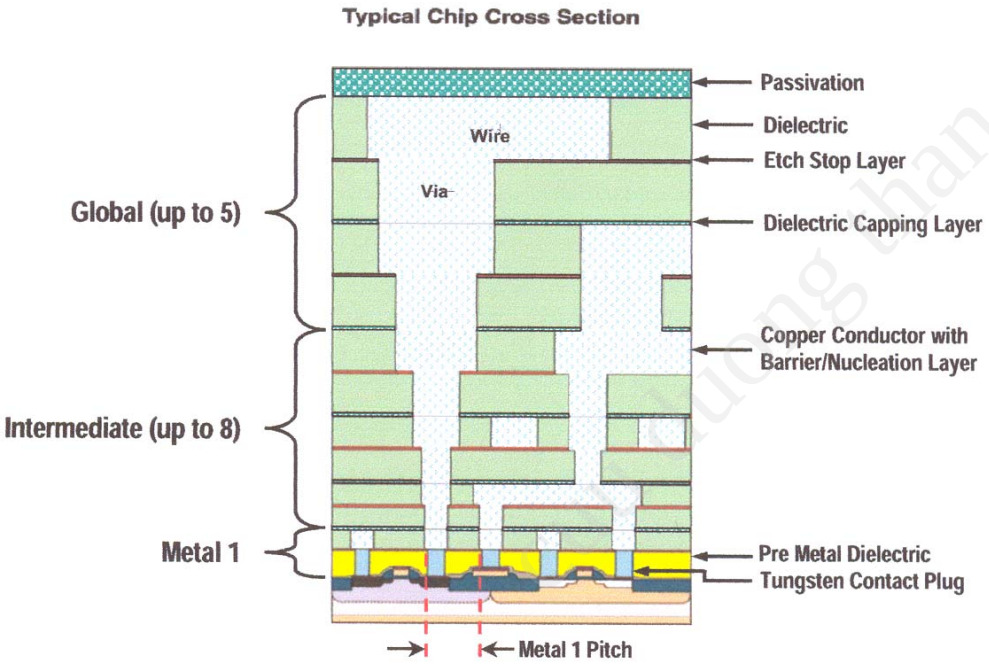
Where V_{out} is the output voltage, and *R* and *C* are total values of all resistances and capacitances of the circuit. Therefore, RC delay is the time when V_{out} attains a value of 63.2% of maximum V_{out}, and can be expressed in the following practical form.

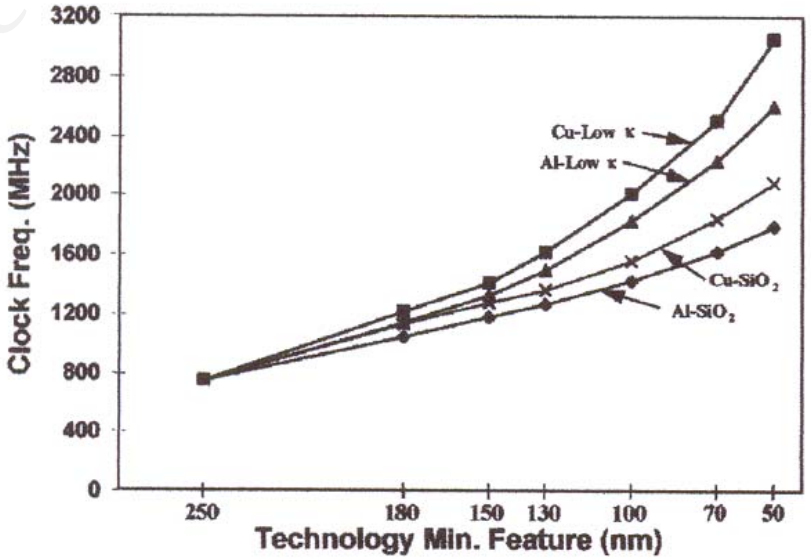
$$RC = L^2 \frac{\rho_M}{t_M} \frac{\varepsilon_{ox}}{t_{ox}}$$

Approaches to reduce RC time delay

(1) Multi-level metallization
(2) Use of low resistivity conductor
(3) Use of low dielectric constant dielectric

$$RC = R_s L^2 \frac{\varepsilon_{ox}}{t_{ox}}$$





Comparison of properties of interconnect materials

	Ag	Al	Al-alloy	Au	Cu	W
Resistivity (μΩ-cm)	1.59	2.66	3.5	2.35	1.67	5.65
Electromigration resistance (at 0.5 μm)	Poor	Poor	Fair-Poor	Very Good	Good	Very Good
Corrosion resistance	Poor	Good	Good	Excel	Poor	Good
Adhesion to SiO_2	Poor	Good	Good	Poor	Poor	Poor
Si deep levels	Yes	No	No	Yes	Yes	No
CVD processing					Avail	Avail
RIE etch		Avail	Avail			Avail