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REVIEW

Ferroelectric Random Access Memories

Hiroshi Ishiwara

Department of Physics, Division of Quantum Phases and Devices, Konkuk University, Seoul 143-701, Republic of Korea

Ferroelectric random access memory (FeRAM) is a nonvolatile memory, in which data are stored using hysteretic *P–E* (polarization vs. electric field) characteristics in a ferroelectric film. In this review, history and characteristics of FeRAMs are first introduced. It is described that there are two types of FeRAMs, capacitor-type and FET-type, and that only the capacitor-type FeRAM is now commercially available. In chapter 2, properties of ferroelectric films are discussed from a viewpoint of FeRAM application, in which particular attention is paid to those of $Pb(Zr,Ti)O_3$, $SrBi_2Ta_2O_9$, and $BiFeO_3$. Then, cell structures and operation principle of the capacitor-type FeRAMs are discussed in chapter 3. It is described that the stacked technology of ferroelectric capacitors and development of new materials with large remanent polarization are important for fabricating high-density memories. Finally, in chapter 4, the optimized gate structure in ferroelectric-gate field-effect transistors is discussed and experimental results showing excellent data retention characteristics are presented.

Keywords: Ferroelectric, Memory, FeRAM, FeFET, $Pb(Zr,Ti)O_3$, $SrBi_2Ta_2O_9$, $BiFeO_3$.

CONTENTS

1. INTRODUCTION

Ferroelectric random access memories (FeRAMs) are being mass-produced at present and widely used in IC (integrated circuits) cards and RF (radio frequency) tags. Their features are (1) nonvolatile data storage (The stored data do not disappear even if electricity is turned off.), (2) the lowest power consumption among various semiconductor memories, and (3) the operation speed as fast as that of DRAMs (dynamic RAMs). The idea of ferroelectric memories was first presented by the researchers in Bell Laboratory in 1955. In their patents, various structures composed of ferroelectric films and semiconductors were proposed and a prototype of the current ferroelectric-gate field-effect transistor (FeFET) was also included. The device structure illustrated in the patent by Ross[1] is shown in Figure 1. It is evident that the device operates as an *n*-channel enhancement-type FET, if the electrical properties at the ferroelectric/semiconductor interface are good.

Si-based FeFETs were first fabricated by Wu in 1974.[2] He deposited a $Bi_4Ti_3O_{12}$ film on a Si(100) substrate as the gate insulator of an FET and observed hysteresis loops in I_D–V_{GS} (drain current vs. gate voltage) characteristics. However, the rotation direction of the loops was opposite to the direction expected from the polarization of the ferroelectric film, which means that the charge injection phenomenon at the ferroelectric/semiconductor interface was more pronounced than the polarization effect. The charge injection phenomenon was found to be sufficiently suppressed by inserting a thin SiO_2 layer between the $Bi_4Ti_3O_{12}$ film and Si substrate, that is, by forming MFIS (M: metal, F: ferroelectric, I: insulator, S: semiconductor) structure.[3] This improvement stimulated the studies on the FeFETs very much. However, since it was difficult to form ferroelectric/semiconductor interfaces with good electrical properties, and since the semiconductor industry was conservative in introducing novel materials containing such elements as Pb and Bi, these studies almost stopped in the 1980s.

In the meantime, a new type of FeRAM, in which data are stored by the polarization direction in ferroelectric capacitors (MFM capacitors) and read out using the polarization reversal current, was proposed and successfully operated in the late 1980s.[4,5] Since the operation of

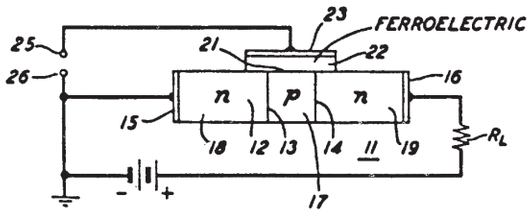

Fig. 1. Semiconductor translating device drawn in the patent by Ross. Reprinted with permission from [1], I. M. Ross, US Patent No. 2791760 **(1957)**. © 1957.

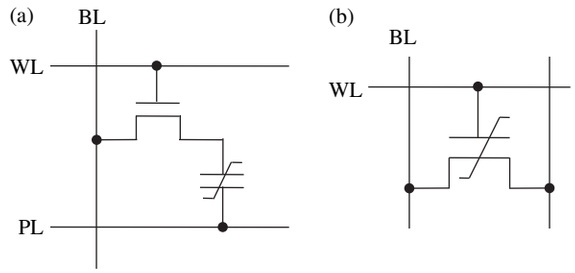

Fig. 2. Classification of FeRAMs. (a) 1T1C-type and (b) 1T-type.

this capacitor-type FeRAM was more stable than that of an FeFET, the studies on this type of FeRAMs became very popular in US, Japan, and Korea in the 1990s. In the mid-1990s, the reliability of the ferroelectric capacitors was much improved by optimization of the deposition conditions of the ferroelectric films, development of passivation films for preventing hydrogen penetration, development of conductive oxide films such as IrO_2 and $SrRuO_3$ for preventing polarization fatigue of the ferroelectric films, and so on.

By using the optimized processes and materials, it became possible to rewrite data more than 10^{12} times and mass-production of FeRAMs began. At present, the maximum memory capacity of the commercially available chip is 4 Mbits and the operation voltage is 1.5 V in the chips using $PbZr_XTi_{1-X}O_3$ (PZT) capacitors and it is 0.9 V in the chips using $SrBi_2Ta_2O_9$ (SBT) capacitors. After the success of the capacitor-type FeRAM, the studies on FeFETs have again become popular. Typical research topics at present are optimization of the buffer layer which is inserted between the ferroelectric film and Si substrate for preventing inter-diffusion of the constituent elements, and development of ferroelectric films with low dielectric constants such as P(VDF-TrFE) (polyvinyliden fluoride-trifluoroethylene)[6] and Si-doped HfO_2.[7]

As described above, FeRAMs are classified in two categories; capacitor-type FeRAMs and FET-type FeRAMs.[8] A typical cell structure in the capacitor-type FeRAM is a 1T1C-type cell shown in Figure 2(a), while a typical cell structure in the FET-type FeRAM is a 1T-type cell shown in Figure 2(b). The cell structure of the 1T1C-type is similar to that of DRAM, except that the cell is connected to the third line (the plate line: PL) in addition to the bit line (BL) and the word line (WL). In this cell, since the polarization reversal current of the ferroelectric capacitor is detected, the readout method is destructive and the "rewrite" operation is necessary. In the 1T-type FeRAM, on the other hand, the memory cell is composed of a single FeFET and the cell size can be shrunk using the proportionality rule. It is also advantageous that the stored data can be non-destructively read out using the drain current of FET.

2. FERROELECTRIC FILMS USED FOR FeRAMs

2.1. Properties Necessary for FeRAMs

A ferroelectric material exhibits a polarization (an electric dipole moment per unit volume) even in the absence of an external electric field, and the direction of the spontaneous polarization can be reversed by an external electric field. In the ferroelectric state the center of the positive charge in a unit cell in the crystal does not coincide with the center of negative charge. A typical plot of polarization versus electric field (P–E) in a ferroelectric film is shown in Figure 3, in which the coercive field E_C is the reverse field necessary to bring the polarization to zero and the remanent polarization P_r is the value of P at $E = 0$.

In a capacitor-type FeRAM cell, data are stored by the polarization direction in a ferroelectric film and the stored data are read out using the polarization reversal current. Thus, the following characteristics are desired for

Hiroshi Ishiwara was born in 1945. He received the B.S., M.S., and Ph.D. degrees in electronic engineering from Tokyo Institute of Technology in 1968, 1970, and 1973, respectively. He was with Tokyo Institute of Technology, as Research Associate (1973–1976), Associate Professor (1976–1989), and Professor (1989–2011) and he is now Professor Emeritus. In 2004 and 2005, he was the Dean of professor at Interdisciplinary Graduate School of Science and Engineering. Since 2010, he is WCU (world Class University) Professor in Department of Physics, Konkuk University, Korea. Dr. Ishiwara was the President of the Japan Society of Applied Physics (JSAP) in 2008 and 2009. He is fellows of IEEE (the Institute of Electrical and Electronics Engineers), MRS (Materials Research Society), IEICE (the Institute of Electronics, Information and Communication Engineers), and IEEJ (the Institute of Electrical Engineers in Japan), and a honorable member of JSAP.

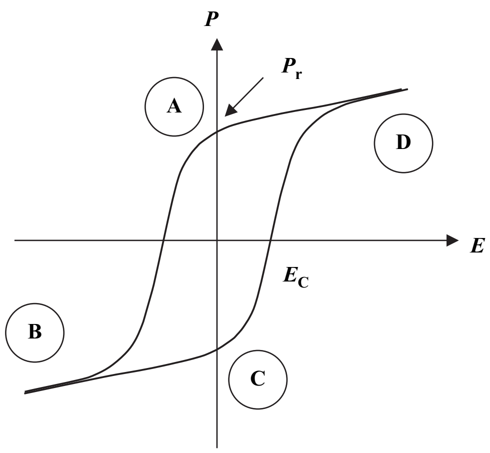

Fig. 3. Schematic drawing of a *P–E* hysteresis loop in a ferroelectric film. P_r: remanent polarization, E_C: coercive field.

a ferroelectric film. The remanent polarization should be large, so that a large polarization reversal current can be derived from a small-area capacitor. The dielectric constant should be low, because a high dielectric constant material produces a large displacement current (linear response) and hinders detection of the polarization reversal current. The coercive field should be low for low-voltage operation of the FeRAM. Degradation of the ferroelectric film should be as low as possible, which is caused during the operation of FeRAMs as well as in the fabrication process. On the other hand, in case of the FET-type FeRAM, since the ferroelectric film is used as the gate insulator of an FET, the large remanent polarization is not necessarily important, but the low reactivity of the ferroelectric film with the semiconductor substrate or with the insulating buffer layer is more important.

Typical degradation mechanisms in the ferroelectric films are polarization fatigue, imprint, and retention loss. Polarization fatigue describes that the remanent polarization P_r becomes smaller when a ferroelectric film experiences a large number of polarization reversals. Variation of the hysteresis loop due to fatigue is schematically shown in Figure 4(a). The physical origin of fatigue is not very clear, but the following factors will be related to the phenomenon; domain wall pinning by charged defects, inhibition of domain nucleation by injected charges, and voltage drop at the interfacial layer between the ferroelectric film and the electrode. The fatigue endurance in FeRAMs is known to be typically 10^{12} switching cycles.

Imprint describes such a phenomenon that when a ferroelectric film experiences a high DC voltage or repeated unipolar pulses for a long time, particularly at a high temperature, its polarization is not fully reversed by application of a single voltage pulse with the opposite polarity. Imprint leads to a shift of the *P–E* hysteresis loop along the electric field axis as well as to a loss of P_r, which is shown in Figure 4(b). Retention loss describes decrease of P_r during absence period of external voltage, as shown in Figure 4(c). Similar to the fatigue, the difference between switching and non-switching charges becomes smaller. The fatigue, imprint, and retention loss characteristics have been greatly improved by optimizing the materials of the ferroelectric capacitors as well as the fabrication processes.

So far, many ferroelectric materials have been investigated, and at present the following three materials are known to be most important for fabricating FeRAMs: PZT, SBT, and $(Bi,La)_4Ti_3O_{12}$ (BLT). Their typical characteristics as polycrystalline films are summarized in Table I. Fabrication methods of the ferroelectric films are CSD (chemical solution decomposition), RF (radio frequency)-sputtering, MOCVD (metal-organic chemical vapor deposition), and so on. Concerning the electrodes for ferroelectric capacitors, noble metals such as Pt and Ir or conductive oxides such as IrO_2 and $SrRuO_3$ are usually used, since the ferroelectric films are crystallized in oxidizing gas at an elevated temperature.

2.2. $Pb(Zr,Ti)O_3$ and Bi-Layer Structured Ferroelectrics

$PbZr_XTi_{1-X}O_3$ (PZT) is a typical ferroelectric material with a perovskite crystal structure and its large P_r value is advantageous for fabricating FeRAMs. PZT has the morphotropic phase boundary (MPB) between tetragonal ($PbTiO_3$-rich) and rhombohedral ($PbZrO_3$-rich) crystal structures at the Zr composition (X) of 0.52, and high dielectric and piezoelectric constants are obtained in the

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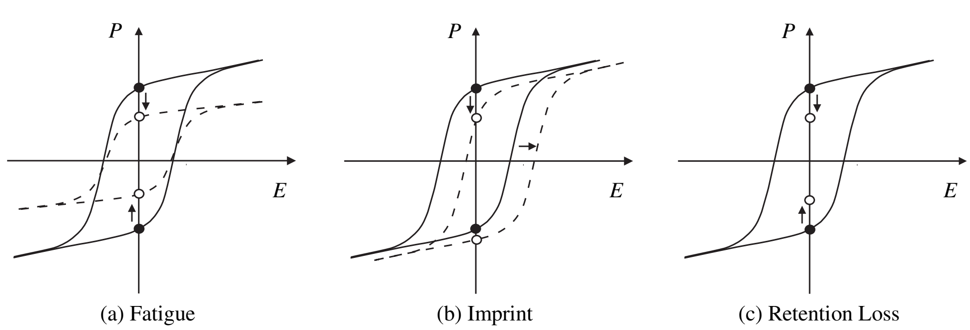

Fig. 4. Various degradation of *P–E* hysteresis loops.

Table I. Properties of typical ferroelectric thin films used for FeRAMs.

Materials	P_r (μC/cm^2)	E_C (kV/cm)	Crystallization Temperature (°C)
$Pb(Zr,Ti)O_3$ (PZT)	30	60	600
$SrBi_2Ta_2O_9$ (SBT)	10	40	750
$(Bi,La)_4Ti_3O_{12}$ (BLT)	20	80	700

vicinity of the MPB composition. The crystallization temperature of PZT films is lower than 650 °C. In FeRAM applications, since the dielectric constant of the ferroelectric film is not necessary to be high, the composition X of 0.3 to 0.4 is usually used and conductive oxide electrodes such as IrO_2 and $SrRuO_3$ are used to minimize the fatigue and imprint phenomena. Properties of PZT such as resistivity, ferroelectricity, piezoelectricity, and electro-optical effect are improved by substituting impurity atoms such as La, Mg, Ca, Sr, and Ba atoms for the Pb site and Nb, Ta, and W atoms for the Zr or Ti site.

It has also been reported that the ferroelectric properties of PZT are improved by forming solid solutions with other ferroelectrics having the same perovskite structure. A typical example is the solution with $BiFeO_3$. A P_r value as large as 32 μC/cm^2 has been reported in a 100nm-thick $[PZT]_{0.95}$-$[BiFeO_3]_{0.05}$ film at an applied voltage of 2 V.[9] Another example is the solid solution with $BiZn_{0.5}Ti_{0.5}O_3$. In this experiment, approximately 200 nm-thick $PbZr_{0.4}Ti_{0.6}O_3$ and $[PbZr_{0.4}Ti_{0.6}O_3]_{0.95}$-$[BiZn_{0.5}Ti_{0.5}O_3]_{0.05}$ films were deposited by spin-coating and crystallized at 600 °C for 30 min in O_2 atmosphere.[10] Figure 5 shows a comparison of the P–E hysteresis loops of MFM capacitors composed of a pure PZT and the solid-solution films. It can be seen from the figure that the P_r value increases from 35 μC/cm^2 to 45 μC/cm^2 by forming the solid solution. It has also been found that the fatigue

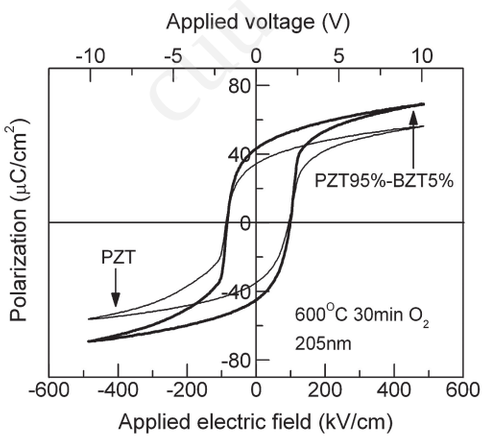

Fig. 5. Comparison of P–E hysteresis loops of $PbZr_{0.4}Ti_{0.6}O_3$ and $[PbZr_{0.4}Ti_{0.6}O_3]_{0.95}$-$[BiZn_{0.5}Ti_{0.5}O_3]_{0.05}$ films Reprinted with permission from [10], M.-H. Tang, et al., *Semicond. Sci. Technol.* 25, 035006 (**2010**). © 2010, IOP Publishing Ltd. The capacitor diameter is 200 μm and the measurement frequency is 10 kHz.

endurance cycles, at which the switching charge becomes a half of the initial value is prolonged from 1×10^5 cycles to 6×10^7 cycles.

SBT and BLT are typical Bi-layer structured ferroelectrics (BLSF). The largest advantage of an SBT film is that it does not show the fatigue phenomenon up to 10^{13} switching cycles, even if Pt electrodes are used. It is also known that the imprint and retention characteristics at high temperatures are superior to those of PZT. On the contrary, it is disadvantageous that the crystallization temperature of BLSF is generally higher than 700 °C. In some cases, Nb atoms are added to SBT up to 20 to 30%. The Nb addition increases the switched charge density $2P_r$ typically from 18 μC/cm^2 to 24 μC/cm^2, but the coercive field E_C also increases typically from 40 to 63 kV/cm. For similar reasons, 20–30% Sr-deficient and 10–15% Bi-rich compositions are often used to increase the remanent polarization and the switched charge.[11]

2.3. $BiFeO_3$

In order to fabricate future capacitor-type FeRAMs with high packing density and low operation voltage, a ferroelectric film with a large P_r and a low E_C is needed. $BiFeO_3$ (BFO) is one of the most promising candidates for this purpose. BFO is a multiferroic material exhibiting ferroelectricity and antiferromagnetism at room temperature (RT) and its crystal structure is a rhombohedrally distorted perovskite structure. In 2003, a remanent polarization as large as 90 μC/cm^2 was found in a single crystalline BFO film grown on a $SrRuO_3$-coated $SrTiO_3$(111) substrate.[12] BFO has another advantage that the crystallization temperature is as low as 550 °C. However, the coercive field is still higher than 200 kV/cm and the leakage current density at a high electric field is very high in polycrystalline BFO films.

To further improve the ferroelectric, dielectric, and insulating properties of BFO thin films, many studies have been conducted, which include optimization of the fabrication methods and process parameters, substitution of impurity atoms, formation of solid solutions with other ferroelectrics, optimization of the electrode materials, and so on. In the impurity substitution studies, almost all rare earth and transition metal elements have been introduced in BFO thin films.[13] The rare earth elements are mainly substituted for the Bi site and they are used for decreasing oxygen vacancy concentration and for decreasing the leakage current. Another purpose of the substitution of rare earth elements is to enhance the ferroelectric properties, which can be achieved through the internal strain caused by presence of impurity ions with the different size. On the contrary, the transition metal elements are mainly substituted for the Fe site and they are used to suppress the valence fluctuation of Fe ions, by which decrease in the leakage current can be expected.

Among various impurity atoms so far attempted, La and Mn atoms seem to be most effective to improve ferroelectric and insulating properties of BFO films. In La substitution for the Bi site, such characteristics as the enhanced remanent polarization, the reduced coercive electric field, the improved fatigue endurance, and the reduced leakage current have been reported. The most pronounced La substitution effect seems to be decrease of the coercive electric field. It has been shown in epitaxial films grown on $SrTiO_3$-templeted Si substrates that E_C decreases from 200 kV/cm in an undoped film to 90 kV/cm in the 15 at%-La-substituted film, keeping a $2P_r$ value as large as 80–90 μC/cm^2. The origin of the low coercivity is speculated to be the high domain wall density in the La-substituted BFO film.[14]

In the case of Mn substitution for the Fe site, the most pronounced effect seems to be the improvement of the leakage current density in the high electric field region. Figure 6 shows J–E (current density vs. electric field) characteristics of undoped and Mn-substituted BFO films.[15] The films were formed on Pt/Ti/SiO_2/Si substrates using chemical solution decomposition and a typical film thickness was 400 nm. As can be seen from the figure, the current density in the undoped BFO film is very low at a lower electric field than 0.3 MV/cm, but it increases sharply when the electric field exceeds 0.3 MV/cm and reaches the range of 10^{-2} A/cm^2 at 1 MV/cm. In the Mn-substituted films, on the other hand, the current densities in the low electric field region steadily increase with increase of the Mn substitution ratio, but that the critical electric field at which current increases sharply shifts to a field higher than 1 MV/cm. As the result, the leakage current densities at 1 MV/cm are lower in the 3 and 5 at% Mn-substituted films than that in the undoped BFO film.

Figure 7 shows comparison of P–E hysteresis loops measured at 1 kHz between undoped and 5 at% Mn-substituted BFO films. As can be seen from the figure, the hysteresis loops in the undoped BFO film are rounded because of the high leakage current density, while the loops are well saturated in the 5 at% Mn-substituted BFO film. In this film, the remanent polarization and coercive field at 1.6 MV/cm were 100 μC/cm^2 and 0.33 MV/cm, respectively. In the 10 at% Mn-substituted film, the leakage current density became high again and the rounded hysteresis loops were obtained. These results clearly show that decrease in the leakage current in the high electric field region is essential in obtaining saturated P–E hysteresis loops.

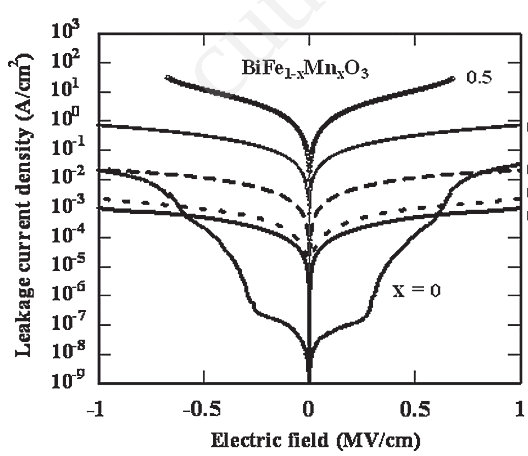

Fig. 6. J–E characteristics of $BiFe_{1-x}Mn_xO_3$ ($x = 0$–0.5) films on a Pt/Ti/SiO_2/Si(100) structure measured at RT. Reprinted with permission from [15], S. K. Singh, et al., *Appl. Phys. Lett.* 88, 262908 **(2006)**. © 2006, American Institute of Physics.

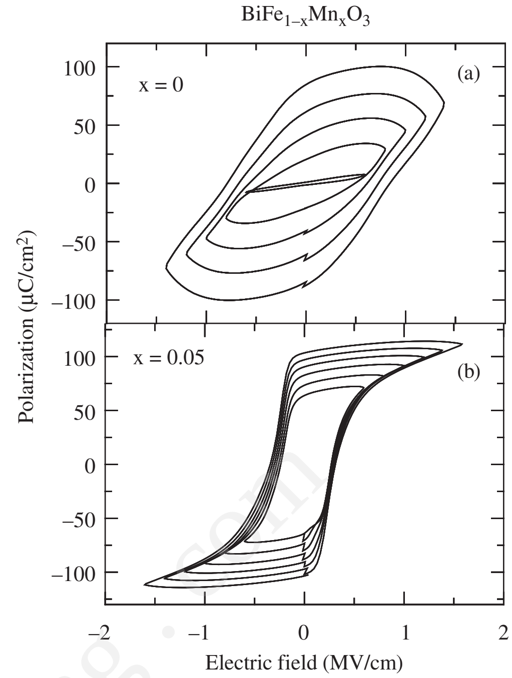

Fig. 7. P–E hysteresis loops of (a) $BiFeO_3$ and $BiFe_{0.95}Mn_{0.05}O_3$ films on a Pt/Ti/SiO_2/Si(100) structure. Reprinted with permission from [15], S. K. Singh, et al., *Appl. Phys. Lett.* 88, 262908 **(2006)**. © 2006, American Institute of Physics.

3. CELL STRUCTURE AND OPERATION PRINCIPLE OF CAPACITOR-TYPE FeRAMs

3.1. Cell Structure of 1T1C-Type FeRAMs

There are several structures in the 1T1C-type FeRAM cells. In a planar capacitor cell, a ferroelectric capacitor is formed on a field oxide film and it is connected to the drain of the FET using the upper electrode, as shown in Figure 8(a). To fabricate this cell, the FET structure is first formed, then the chip surface is covered with the inter-layer oxide and planarized by chemical mechanical polishing. Next, the Pt bottom electrode with a Ti or TiO_2 sticking layer to SiO_2, the ferroelectric film, and the Pt top electrode are successively blanket-deposited and the capacitor structure is formed by etching the films using

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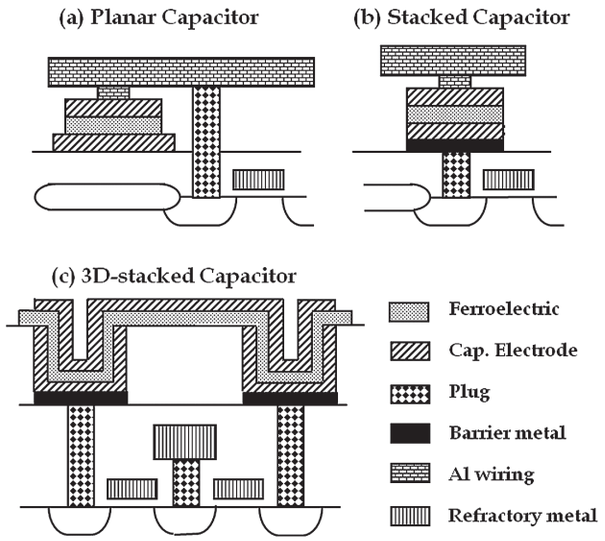

Fig. 8. Classification of cell structures. (a) Planar capacitor cell, (b) stacked capacitor cell, and (c) 3D-stacked capacitor cell.

2 or 3 different masks. In FeRAMs, since a plate line is connected to the individual capacitors, it is necessary to separate ferroelectric capacitors cell by cell, which is different from DRAM cells.

In a stacked capacitor cell shown in Figure 8(b), the ferroelectric capacitor is formed on the FET and the bottom electrode of the capacitor is connected to the drain of the FET using a plug. A key technology to fabricate this structure is the electrical connection between the plug and the bottom electrode, because plug materials such as poly-Si and W are easily oxidized and electrically disconnected through the crystallization process of the ferroelectric film. To solve this problem, a barrier metal layer such as Ir/IrO_2 or Ir/IrO_2/TiAlN is inserted between the bottom electrode and the plug. In this cell structure, it is possible to etch the stacked films continuously using a single mask. This method has an advantage that the capacitor area can be reduced, particularly when the etching angle is close to 90°.

In future high-density memories, it is important to further shrink the cell size without reducing the stored charge. One method for this purpose is to develop a novel ferroelectric material with a large remanent polarization, as discussed in 2.3. The other method is to fabricate ferroelectric capacitors in three-dimension, as shown in Figure 8(c). In fabrication of this structure, MOCVD technique is needed for depositing a ferroelectric film uniformly on the side wall of the holes as well as the bottom face. After fabrication of the capacitors, the wafer surface is again planarized by depositing a SiO_2 film. During this process, since SiH_4 gas is decomposed, hydrogen gas is inevitably generated. Furthermore, it has been found that H_2 gas is decomposed to hydrogen atoms by the catalytic action of Pt and the ferroelectric properties of the film are severely degraded by penetration of hydrogen atoms. Thus, to minimize degradation of the ferroelectric properties of the capacitors, formation of a hydrogen barrier layer such as an Al_2O_3 layer is needed prior to deposition of a SiO_2 film.

3.2. Operation Principle of 1T1C-Type FeRAMs

Figure 9 shows the time sequence diagram of voltage pulses for writing data in a 1T1C cell. To write a "1" datum, the BL and PL in Figure 2(a) are raised to V_{DD} (power supply voltage). Then, the WL is raised to V_{PP} ($V_{DD} + V_T$ or the higher voltage) so that the voltage drop across the FET is negligible, where V_T is the threshold voltage of the FET. At this time, the polarization direction of the ferroelectric film is unchanged, because the voltages of the PL and the BL are equal. Next, the voltage of the PL is driven back to zero, keeping the voltage of the BL at V_{DD}. At this time, the film is polarized downwards. Finally, the BL and the WL are driven back to zero. To write a "0" datum, the voltage pulses with the same time sequence are applied to the PL and WL, while the BL is kept grounded. As the result, the film is polarized upwards when the PL is raised to V_{DD}.

To read the stored data, the PL is raised to V_{DD} and a sense amplifier connected between the BL and a reference voltage is turned on. If the stored datum is "1", polarization of the ferroelectric film is reversed and the BL voltage increases because of the current flowing out of the capacitor. This small unbalance is amplified by the sense amplifier and the BL voltage reaches V_{DD} in a short time. The voltage difference is transferred to the periphery circuit as the datum "1" signal. After the BL voltage reaches V_{DD}, the voltage of the PL is driven back to zero, by which the polarization of the ferroelectric film returns to the downward direction ("rewrite" operation). To generate the reference voltage in a 1T1C cell array, which is requested to be kept in the middle of the cell voltages corresponding to "1" and "0" data, a ferroelectric capacitor with a larger area is used and its polarization is reversed whenever "read" or "write" operation is conducted. In this

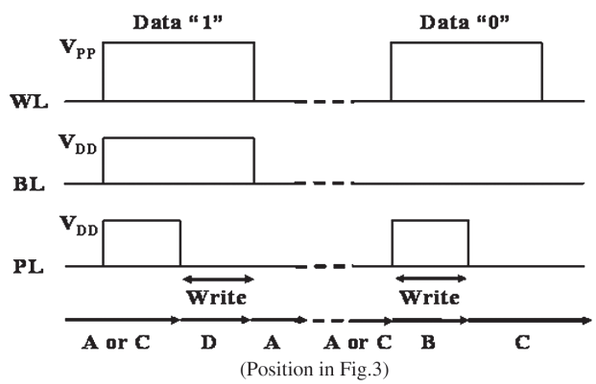

Fig. 9. A schematic time sequence diagram for "write" operation.

case, the reference voltage gradually changes by fatigue of the ferroelectric capacitor and the change in the reference voltage roughly coincides with that of the cell voltages.

3.3. Other Capacitor-Type FeRAMs

To decrease the cell area and to increase the stability in "write/read" operation, a chain FeRAM has been proposed and its operation has successfully been demonstrated.[16] Figure 10 shows the circuit diagram of a chain cell block. As shown in the figure, a ferroelectric capacitor and a MOSFET are connected in parallel in each cell and the cells are connected in series, forming a chain cell block. During the stand-by period, the gate voltage of the FET (BS0) for selecting the cell block is grounded, while all word lines are boosted to V_{PP} so that all ferroelectric capacitors are short-circuited by the FETs, by which a possibility such that polarization of the ferroelectric capacitors is reversed by noise signals becomes very low.

In "write/read" operation, the gate voltage of the selected BS0 is raised to V_{DD} and the FET in the selected cell is turned off by pulling down the voltage of the selected WL. Under this condition, since the BL voltage is applied only to the ferroelectric capacitor in the selected cell, the "write/read" operation can be conducted by the similar manner as that for a 1T1C-type cell. Additionally, high-speed operation can be expected, because the voltage is not applied to the unnecessary ferroelectric capacitors.

Another group in capacitor-type FeRAMs is NVSRAMs (non-volatile static RAMs), in which ferroelectric capacitors are connected to the storage nodes of SRAM cells through pass transistors[4] or directly.[17] The circuits usually operate as SRAM and when electricity is turned off, the voltages at the storage nodes are transformed to the polarization direction of the ferroelectric capacitors by conducting "store" operation. When electricity is turned on, the data stored in the ferroelectric capacitors are returned to the SRAM by conducting "recall" operation. In a 6T4C-type NVSRAM,[17] four ferroelectric capacitors are stacked on the SRAM circuit, so that the cell area is almost same as that of a usual volatile SRAM. Furthermore, since the polarization direction does not change during the normal operation of this circuit, the operation speed is as fast as that of a usual SRAM and there is practically no limitation in "write/read" cycles.

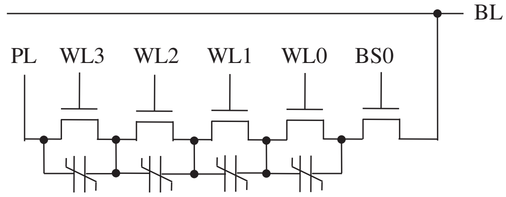

Fig. 10. Circuit configuration of a cell block in a chain FeRAM.

4. CELL STRUCTURE AND OPERATION PRINCIPLE OF FET-TYPE FeRAMs

4.1. Optimization of FeFET Structure

One-transistor-type (1T-type) FeRAM shown in Figure 2(b) has a potential to be integrated in high-density, because each memory cell is composed of a single ferroelectric-gate FET (FeFET) and because the FET can be scaled down using the proportionality rule. In an FeFET, electrons or holes are accumulated at the surface of semiconductor according to the polarization direction of the gate ferroelectric film, and drain current flows between the source and drain regions, only when one type of the carriers is accumulated at the interface. Thus, 1T-type FeRAM has another advantage that stored data can non-destructively be read out using drain current of the FET. Concerning the remanent polarization of the gate ferroelectric film, a large value is unnecessary, because the surface carrier density necessary for operation of MOSFETs is on the order of 10^{12} electrons (holes)/cm^2 (0.16 μC/cm^2).

However, it is very difficult to fabricate FeFETs with excellent electrical properties, because of inter-diffusion of the constituent elements in the film and the substrate. That is, when a ferroelectric film is deposited directly on a Si substrate, the constituent elements in the both sides diffuse each other during crystallization annealing. To avoid degradation due to the inter-diffusion, an insulating buffer layer is often inserted between the ferroelectric film and the Si substrate. Even in this structure, carriers are induced on the semiconductor surface by polarization of the ferroelectric film, as long as the charge neutrality condition is satisfied at the interface between the ferroelectric film and the insulating buffer layer.

In these structures, however, new problems arise such that the data retention time is short and the operation voltage is high. The reason why the data retention time is short is explained by the following series connection model of ferroelectric and dielectric capacitors.[18] In an FeFET, when the power supply is off and the gate terminal of the FET is grounded, the top and bottom electrodes of the two capacitors are short-circuited. At the same time, electric charges $\pm Q$ remain on the electrodes of the both capacitors due to the remanent polarization of the ferroelectric film and due to the charge neutrality condition at a node between the two capacitors. The Q–V (charge vs. voltage) relationship in the dielectric capacitor is $Q = CV$ (C: capacitance of the dielectric layer), and thus the relationship in the ferroelectric capacitor becomes $Q = -CV$ under the short-circuited condition. This relationship means that the direction of the electric field in the ferroelectric film is opposite to that of the polarization. This field is known as the depolarization field and it reduces the data retention time significantly.

In order to make the depolarization field low, C must be as large as possible. That is, a thin buffer layer with a high

dielectric constant is desirable. Another important point is to reduce the leakage current in both the ferroelectric film and the buffer layer. If the charge neutrality at a node between the two capacitors is destroyed by the leakage current, electric charges on the electrodes of the buffer layer capacitor disappear, which means that carriers on the semiconductor surface disappear and the stored data cannot be read out by drain current of the FET, even if the polarization of the ferroelectric film is retained. Thus, it is very important to reduce the leakage current across both a ferroelectric film and a buffer layer.

Based on these considerations, various buffer layer materials have been investigated experimentally. Among the various candidates, excellent data retention characteristics have been obtained in FeFETs with HfAlO[19] and HfO_2 buffer layers,[20] as discussed in the next section. In addition to the studies on the buffer layer materials, studies on ferroelectric materials with low dielectric constants have also been conducted. When the dielectric constant of a ferroelectric film is low, the external voltage is more effectively applied to the ferroelectric film and thus a wider memory window in drain current versus gate voltage (I_D–V_{GS}) characteristics is expected. Typical materials are $Sr_2(Ta,Nb)_2O_7$,[21] P(VDF-TrFE),[6] and Si-doped HfO_2.[7]

4.2. Data Retention Characteristics of FeFETs

MFIS diodes and FETs have been fabricated on a Si substrate using HfO_2 as a buffer layer and using SBT or $(Bi,La)_4Ti_3O_{12}$ (BLT) as a ferroelectric film.[20] The buffer layer was deposited by vacuum evaporation of sintered HfO_2 targets at room temperature and subsequently annealed in O_2 atmosphere at 800 °C for 1 min. Then, an SBT or BLT film was deposited by spin-coating, dried and calcined in air, and annealed in O_2 atmosphere at 750 °C for 30 min for crystallization. Finally, Pt top electrodes were deposited. Figure 11 shows I_D–V_{GS} characteristics of FeFETs with SBT(400 nm)/HfO_2(8 nm) and BLT(400 nm)/HfO_2(8 nm) gate structures.[22] As can be seen from the figure, I_D–V_{GS} characteristics show clockwise hysteresis and the drain current on/off ratio at a gate voltage of 0.8 V is as large as 10^5 in the SBT/HfO_2 sample. The memory window width in the hysteresis loop is about 1.0 V in the SBT/HfO_2 sample and it is about 0.5 V in the BLT/HfO_2 sample.

Figure 12 shows data retention characteristics of FeFETs with the Pt/SBT/HfO_2/Si and Pt/BLT/HfO_2/Si gate structures. In these measurements, "write" pulses of ±10 V in amplitude and 1 μs in width were initially applied to the gate, and variation of the drain currents with time was measured. In the SBT/HfO_2 sample, the drain current on/off ratio was larger than 10^3 even after 30 days had elapsed. Furthermore, if the experimental data are simply extrapolated toward a longer time scale, the current on/off ratio at 10 years (3×10^8 sec) is expected to be

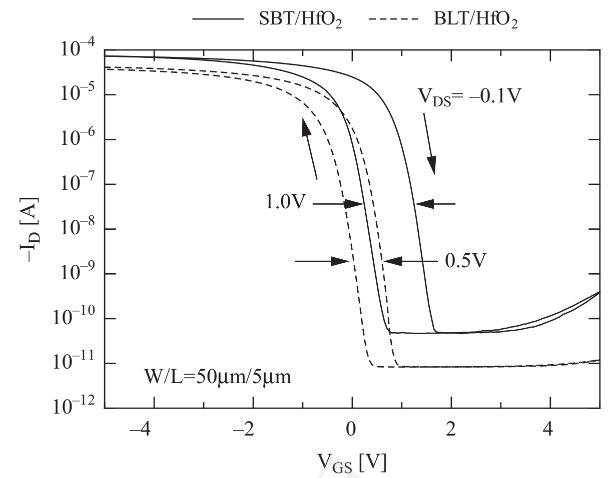

Fig. 11. I_D–V_{GS} characteristics of FeFETs with SBT/HfO_2 and BLT/HfO_2 gate structures. Reprinted with permission from [22], K. Takahashi, et al., *Jpn. J. Appl. Phys.* 44, 6218 (**2005**). © 2005, The Japan Society of Applied Physics.

much larger than 100. These results show that HfO_2 is one of the best buffer layer materials to be inserted between the ferroelectric film and Si substrate and to prevent interdiffusion of constituent elements in MFIS FETs. Recently, it has also been shown in an FeFET with a HfAlO buffer layer that the data retention time is not seriously degraded, even if the operation temperature is increased to 85 °C.[23]

4.3. Cell Array Structures

To increase the packing density of FET-type FeRAMs, it is desirable that each memory cell is composed of a single FeFET. A typical 1T-type cell array is shown in Figure 13, in which Si stripes with a lateral npn structure are placed on an insulating substrate, they are covered with a uniform ferroelectric film, and then metal stripes are placed on the film perpendicular to the Si stripes. Thus, each Si stripe represents a parallel connection of FeFETs and no via hole through the ferroelectric film exists in the array area.[24] Furthermore, since isolation is conducted using an SOI

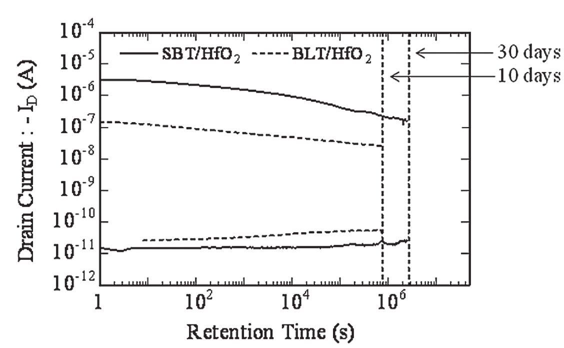

Fig. 12. Data retention characteristics of FeFETs with SBT/HfO_2 and BLT/HfO_2 gate structures. Reprinted with permission from [22], K. Takahashi, et al., *Jpn. J. Appl. Phys.* 44, 6218 (**2005**). © 2005, The Japan Society of Applied Physics.

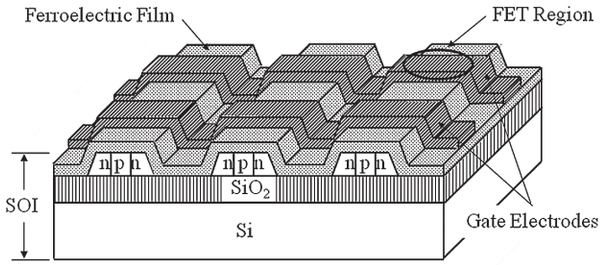

Fig. 13. A cell array of 1T-type FeRAMs formed on an SOI structure.

(silicon-on-insulator) structure, the cell area is expected to be much smaller than that formed in a bulk Si wafer using a double well structure.

In this 1T-type cell array, the stored data in non-selected cells are often reversed unintentionally by repetition of "write/read" operations. Thus, the "write/read" method to minimize the data disturbance phenomenon is important. A typical method to write a datum in a selected cell in the array is the so-called V/3 rule, in which V and V/3 are applied to the selected and non-selected metal electrodes, respectively, while 0 and 2 V/3 are applied to the selected and non-selected Si stripes. In this method, the magnitude of the disturbance voltage generated in the non-selected cells is 1/3 of the "write" voltage applied to the ferroelectric film in the selected cell. However, this voltage ratio is not necessarily sufficient in practical applications and thus a compensation operation to further decrease the disturbance phenomenon has also been proposed.[25]

A NAND-type array called the FeNAND (ferroelectric NAND) has also been proposed and fabricated.[26] The operation principle of the FeNAND is similar to that of a NAND flash memory composed of floating-gate-type FETs, but the FeNAND has such advantages that the "write" voltage is lower (7.5 V) and the "rewrite" endurance is higher (10^8 cycles) than those in the NAND flash memory. Operation of a 64 kbit cell array fabricated using 5-μm-rule has been reported.[27]

5. SUMMARY

History and current status of ferroelectric random access memory (FeRAM) were reviewed. First, it was described that two types of FeRAMs (capacitor-type and FET-type) exist and only the capacitor-type FeRAM is now commercially available. In chapter 2, properties of ferroelectric films were discussed from a viewpoint of FeRAM application, in which particular attention was paid to those of $Pb(Zr,Ti)O_3$, $SrBi_2Ta_2O_9$, and $BiFeO_3$. Then, cell structures and operation principle of the capacitor-type FeRAMs were discussed in chapter 3. It was described that the stacked technology of ferroelectric capacitors was important for fabricating high-density memories. Finally, in chapter 4, the optimized gate structure in FeFET was discussed and experimental results showing excellent data retention characteristics were presented.

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REVIEW