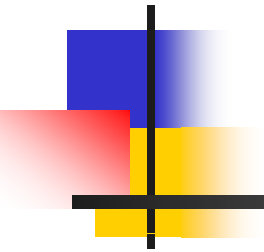
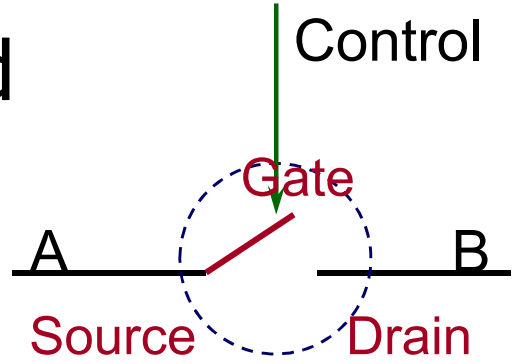


# Lecture 7: CẤU TRÚC MOS

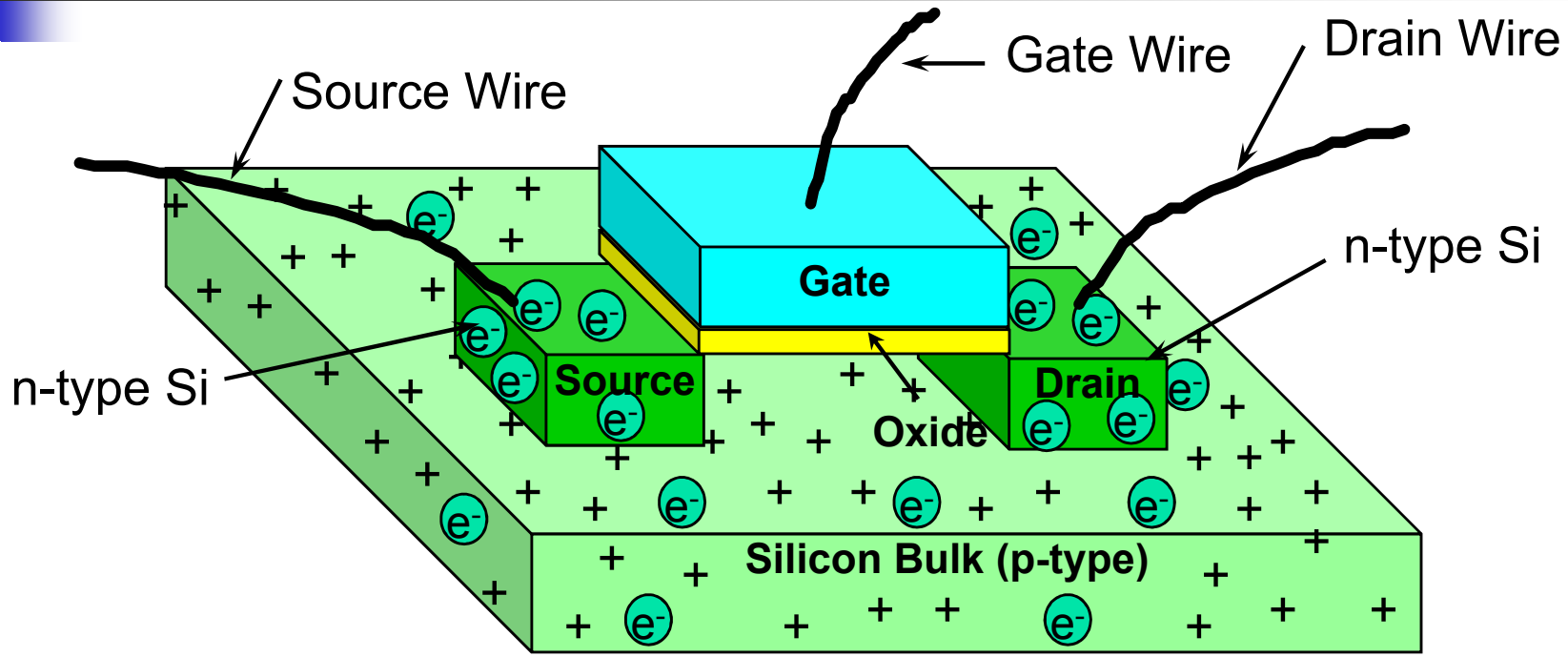
Biên soạn:Th.S Bùi Quốc Bảo

(Base on Floyd, Pearson Ed.)

- Để thực hiện mạch logic, ta cần các switch điều khiển được
  - Control input = 1 → Switch is closed
  - Control input = 0 → Switch is open




- **Ta có thể dùng relay cơ khí**
  - Lớn, tiêu tán năng lượng, đáp ứng chậm
- **Transistors là lựa chọn tốt hơn**
  - Nhỏ, hiệu suất cao, nhanh.



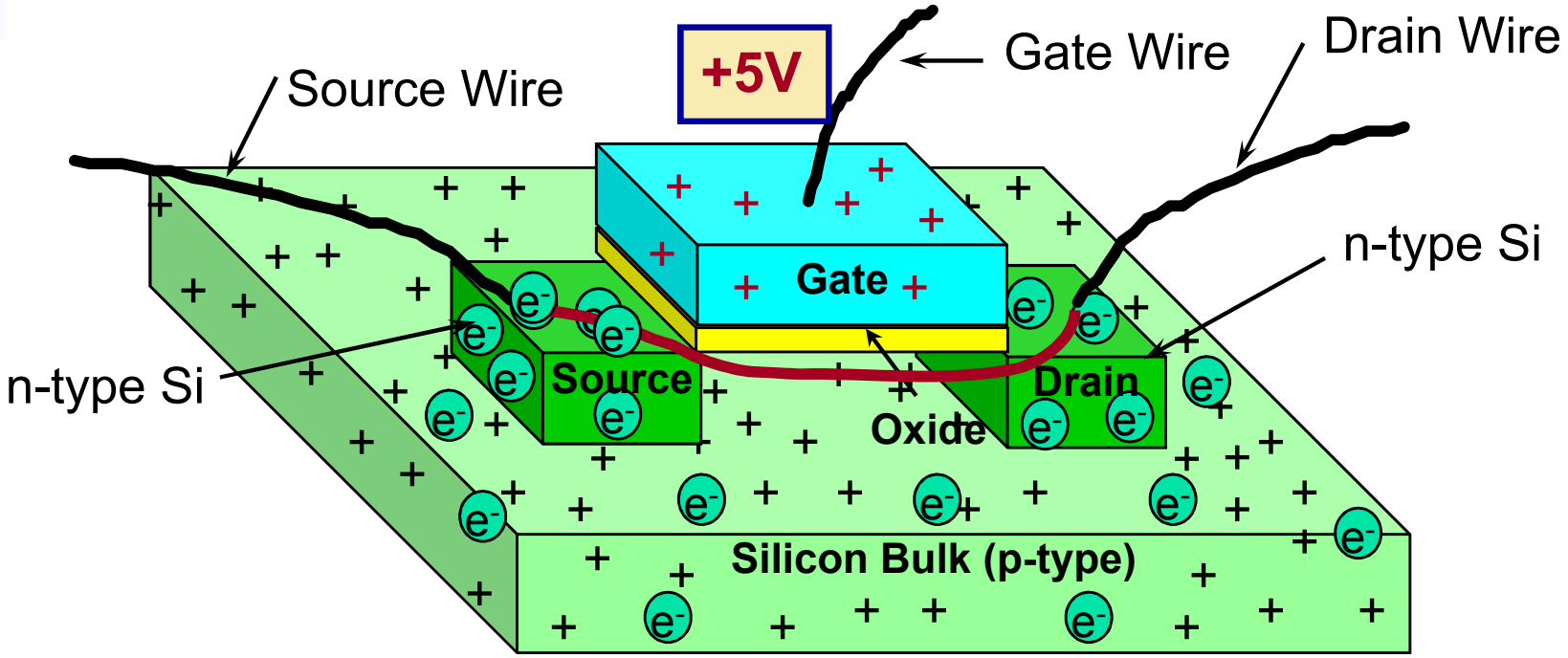

P-type silicon: Excess positive charges (electron holes)

N-type silicon: Excess negative charges (electrons)

Oxide: Insulator

Gate: Metal pad

In this state, current (electrons) cannot flow between source and drain – switch is OPEN

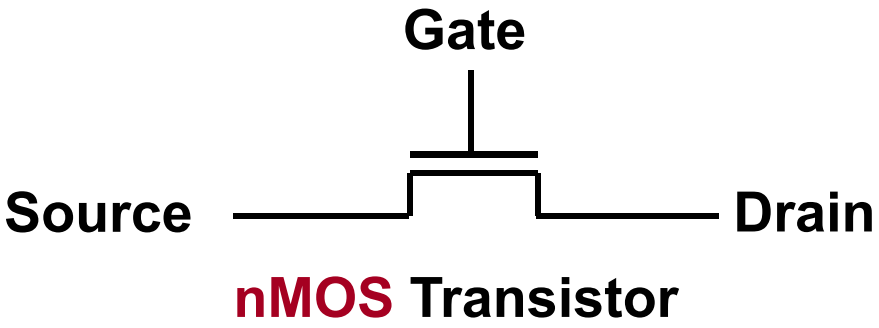



Place a positive charge on the gate wire (gate = +5V)

The gate's positive charge attracts negatively-charged electrons

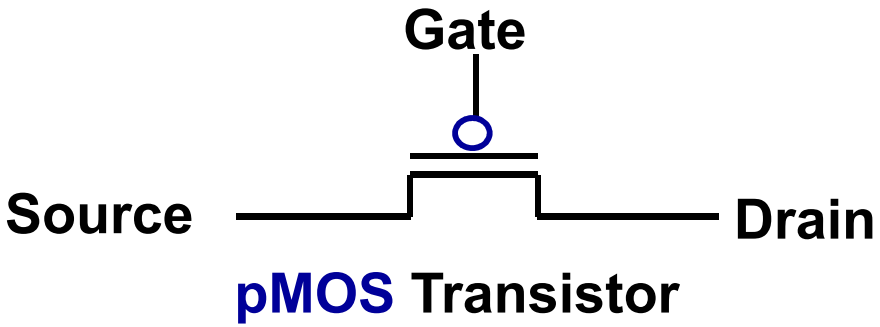
This row of electrons forms a channel connecting the Source and Drain – Current can flow – Switch is CLOSED

# CẤU TRÚC MỘT SỐ CỔNG




**nMOS Transistor**

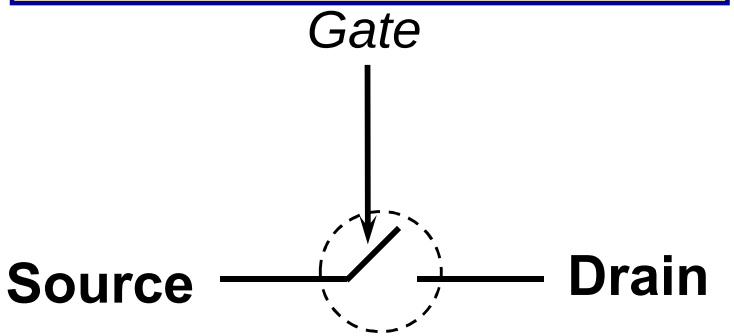
nMOS: Good connector to GND
Poor connector to +5



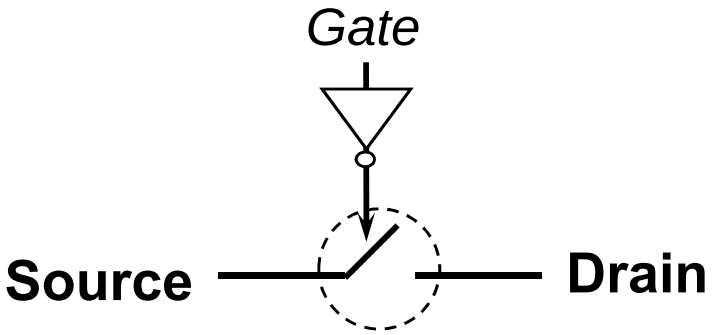

**pMOS Transistor**

pMOS: Poor connector to GND
Good connector to +5

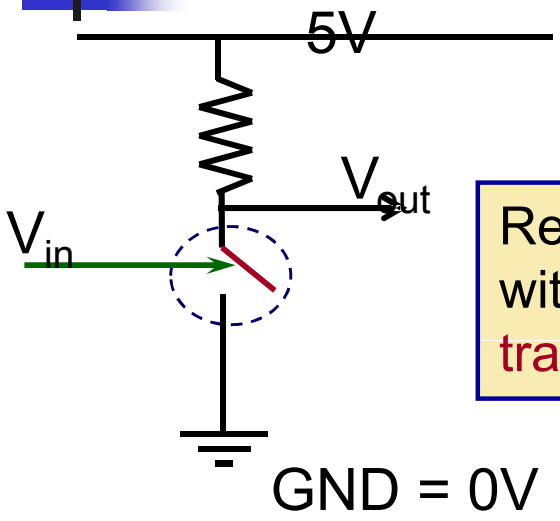
Logic 1 on gate:
Source and Drain connected



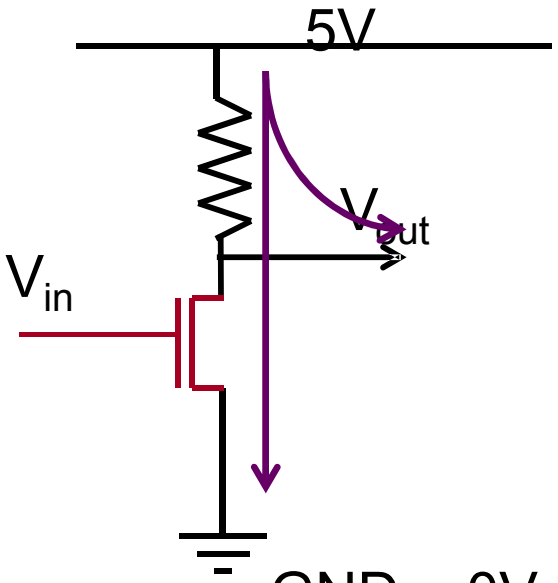

Logic 0 on gate:
Source and Drain connected



# NMOS INVERTER (CỔNG NOT)



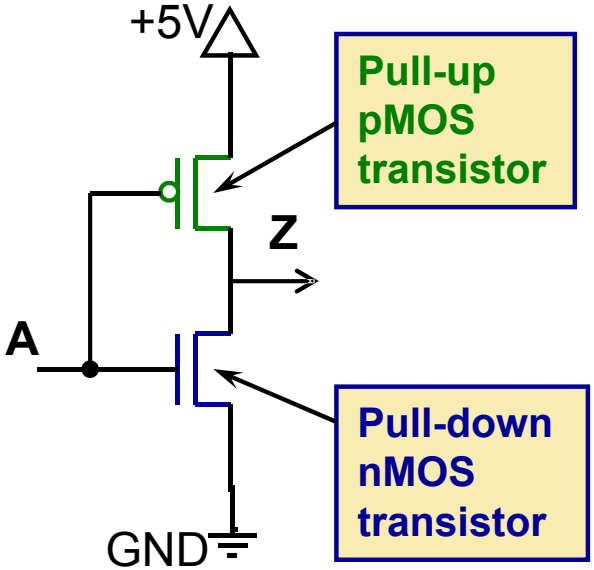

Replace the switch with an NMOS transistor

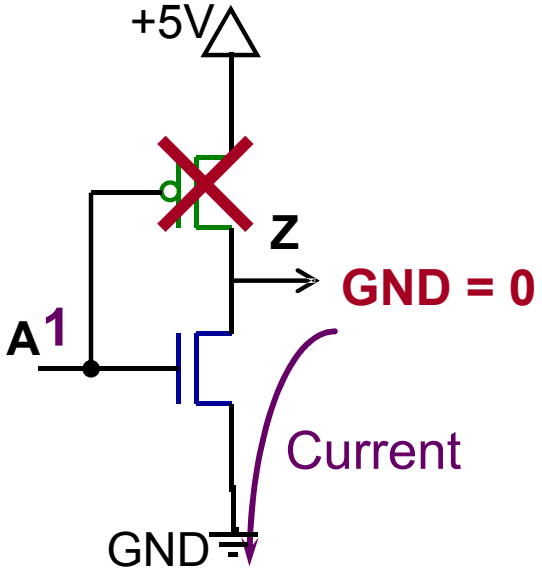


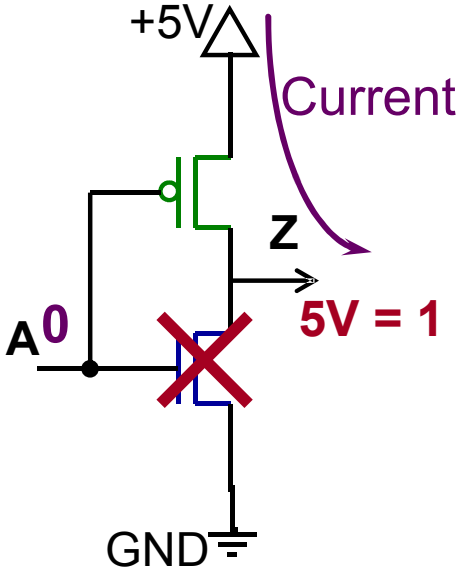

- Hoạt động:
  - Khi Transistor đóng, có dòng điện đi qua R xuống GND
    - Mất năng lượng, tỏa nhiệt

- Khi transistor mở, có dòng qua R đi ra ngoài
  - Mất năng lượng, tỏa nhiệt

# MOS INVERTER



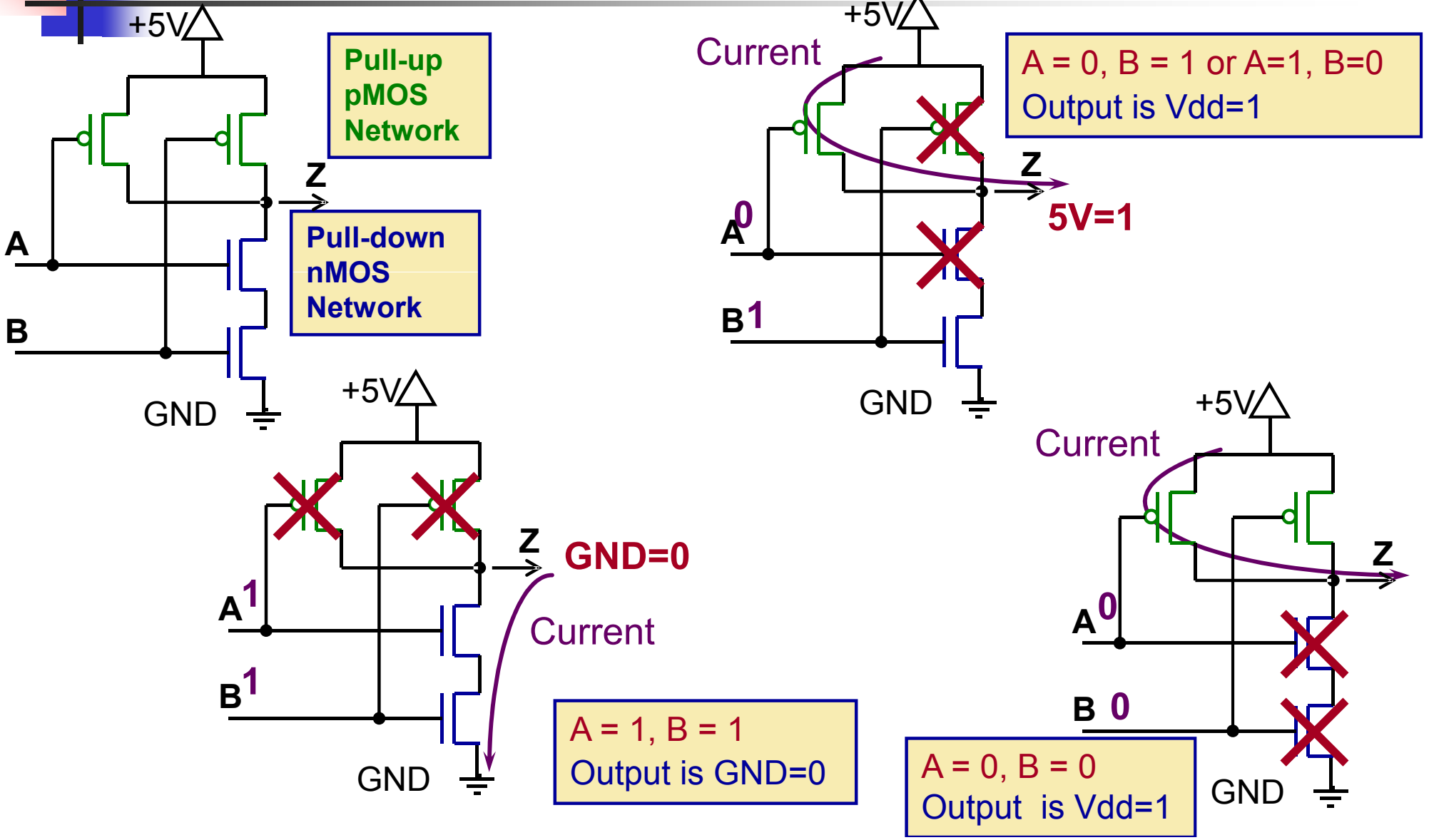



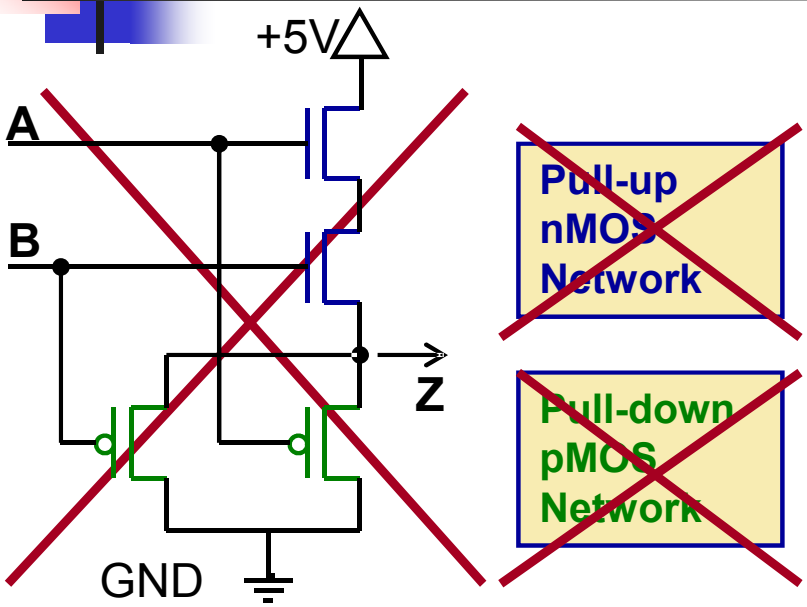

Input is 1
Pull-up does not conduct
Pull-down conducts
Output connected to GND

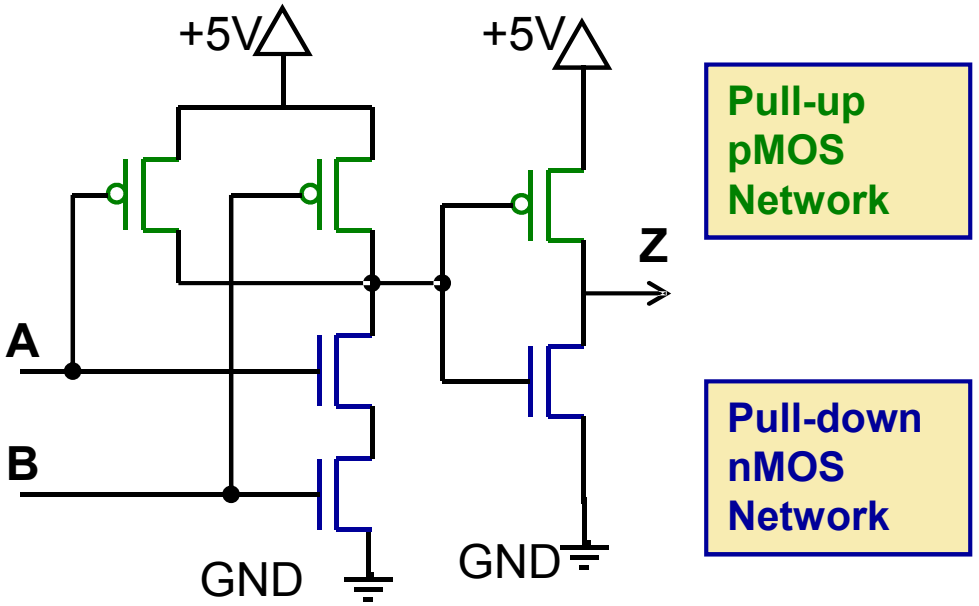
Input is 0
Pull-up conducts
Pull-down does not conduct
Output connected to Vdd

# MOS NAND GATE



# MOS AND GATE




Build an AND gate by mirroring a NAND gate.

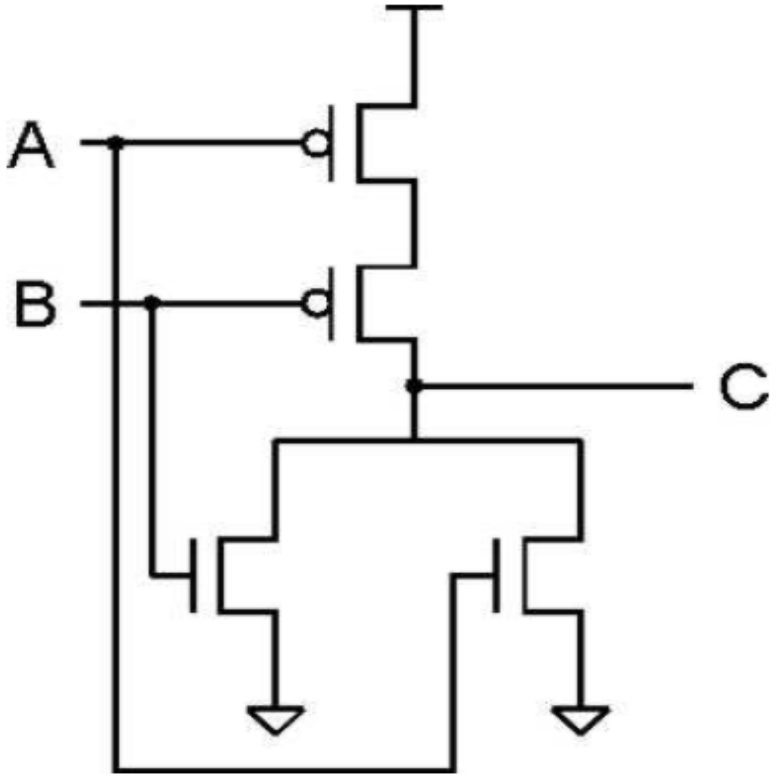
Problem: nMOS is poor at transmitting 5V and pMOS is poor at transmitting GND

Take a NAND gate…

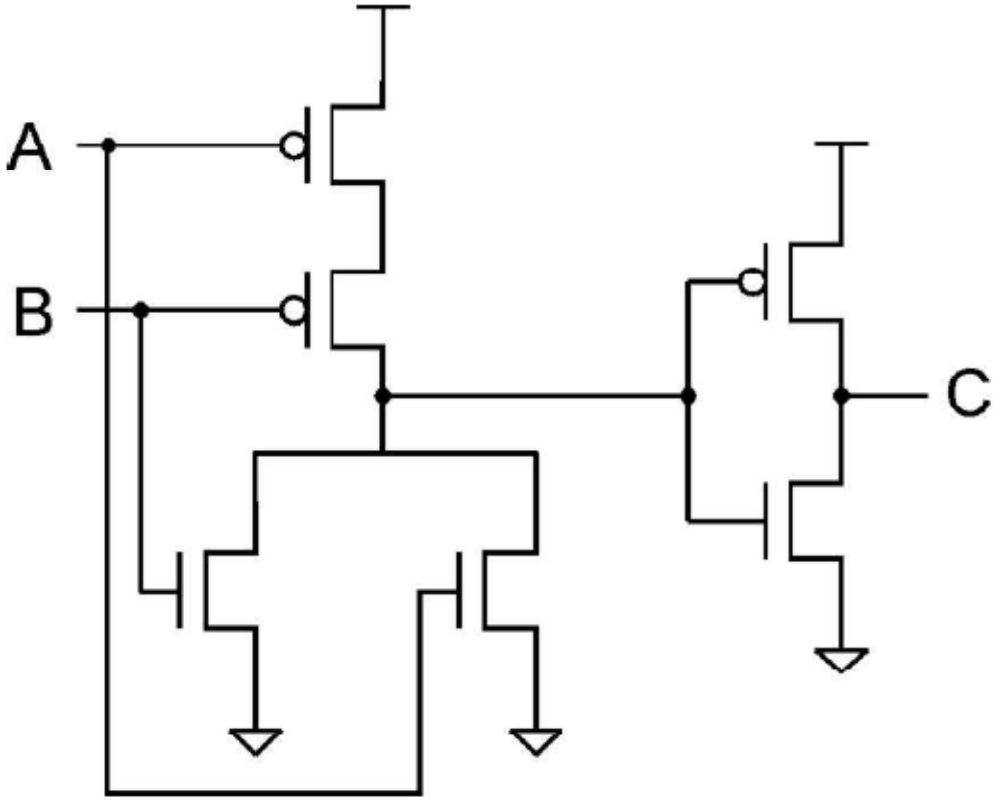
and invert the output

Takes two more transistors, but works! This is the reason that NANDs/NORs are faster than ANDs/ORs

# NOR GATE – OR GATE

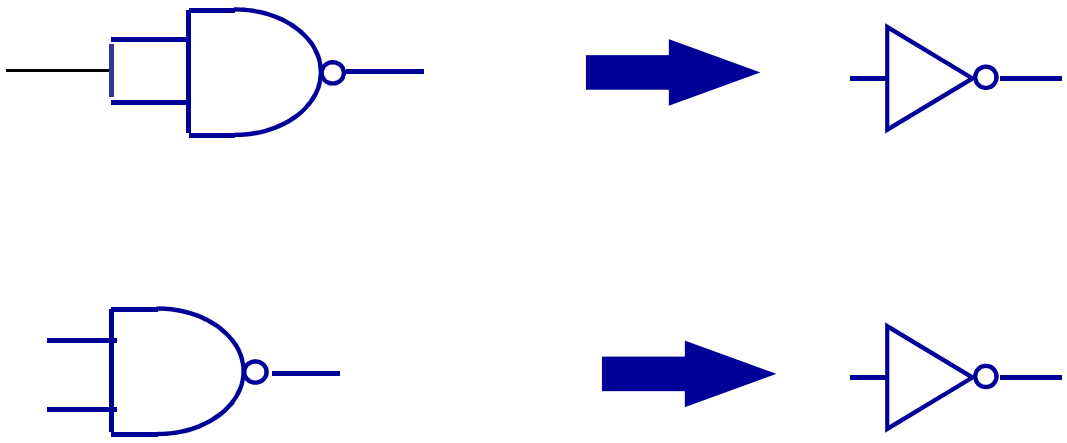



NOR-GATE




OR-GATE

# THỰC HIỆN MẠCH NAND-NAND NOR-NOR



THỰC HIỆN CỔNG NOT TỪ CỔNG NAND, NOR

Dùng định lý De_Morgan để biến đổi về dạng toàn NAND, toàn NOR

$$F(A,B,C) = AB + AC = \overline{\overline{AB} \cdot \overline{AC}}$$

$$F(A,B,C) = (A+B)(A+C) = \overline{\overline{(A+B)}\,\overline{(A+C)}}$$

Nếu hàm ở dạng SOP, kết quả là dạng toàn NAND
Nếu hàm ở dạng POS, kết quả là dạng toàn NOR