Exercise 4.1

Different instructions utilize different hardware blocks in the basic single-cycle implementation. The next three problems in this exercise refer to the following instruction:

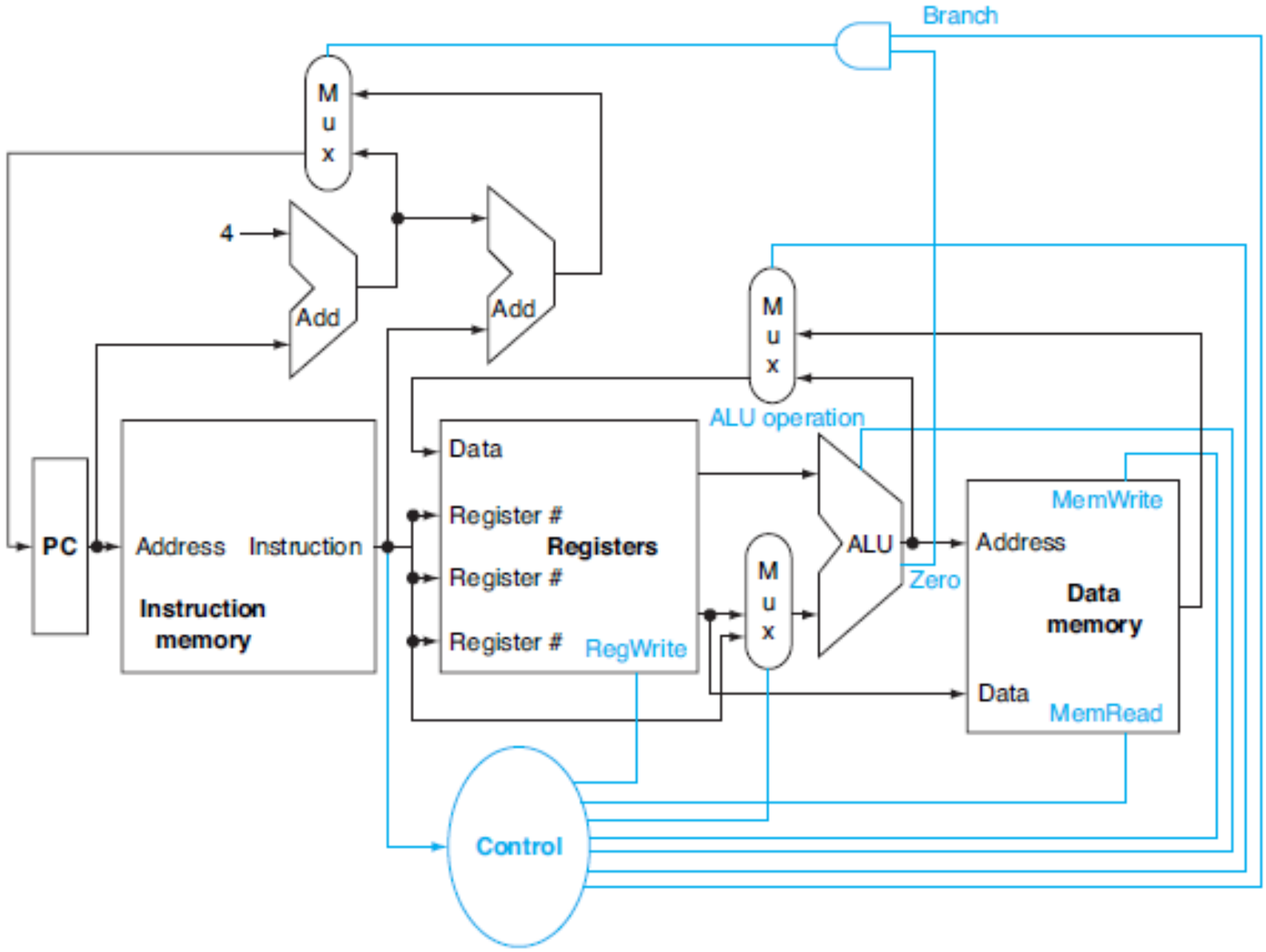
a. AND Rd,Rs,Rt → Reg[Rd] = Reg[Rs] AND Reg[Rt]

b. *SW Rt,Offs(Rs) → Mem[Reg[Rs] + Offs] = Reg[Rt]*

4.1.1 [5] <4.1> What are the values of control signals generated by the control in Figure 4.2 for this instruction?

4.1.2 [5] <4.1> Which resources (blocks) perform a useful function for this instruction?

4.1.3 [10] <4.1> Which resources (blocks) produce outputs, but their outputs are not used for this instruction? Which resources produce no outputs for this instruction?


Branch
M
u
x
4
Add
Add
M
u
x
ALU operation
PC
Address
Instruction
Instruction
memory
Data
Register #
Registers
Register #
Register #
RegWrite
M
u
x
ALU
Zero
MemWrite
Address
Data
memory
Data
MemRead
Control

Lời giải 4.1

4.1.1 The values of the signals are as follows:

RegWrite:	?
MemRead:	?
ALUMux:	?
MemWrite:	?
ALUop:	?
RegMux:	?
Branch:	?

Lời giải 4.1

4.1.1 The values of the signals are as follows:

(a): *AND Rd,Rs,Rt* → *Reg[Rd] = Reg[Rs] AND Reg[Rt]*

RegWrite:	1
MemRead:	0
ALUMux:	0
MemWrite:	0
ALUop:	10 (AND)
RegMux:	1
Branch:	0

a. 1 0 0 (Reg) 0 AND 1 (ALU) 0

b. 0 0 1 (Imm) 1 ADD X 0

ALUMux is the control signal that controls the Mux at the ALU input, 0 (Reg) selects the output of the register fi le and 1 (Imm) selects the immediate from the instruction word as the second input to the ALU.

RegMux is the control signal that controls the Mux at the data input to the register fi le, 0 (ALU) selects the output of the ALU, and 1 (Mem) selects the output of memory.

A value of X is a “don’t care” (does not matter if signal is 0 or 1).

Lời giải 4.1

4.1.1 The values of the signals are as follows:

(b) *SW Rt,Offs(Rs)* → *Mem[Reg[Rs] + Offs] = Reg[Rt]*

RegWrite:	0
MemRead:	0
ALUMux:	1 (Imm)
MemWrite:	1
ALUop:	00 (ADD)
RegMux:	X
Branch:	0

ALUMux is the control signal that controls the Mux at the ALU input, 0 (Reg) selects the output of the register fi le and 1 (Imm) selects the immediate from the instruction word as the second input to the ALU.

RegMux is the control signal that controls the Mux at the data input to the register fi le, 0 (ALU) selects the output of the ALU, and 1 (Mem) selects the output of memory.

A value of X is a “don’t care” (does not matter if signal is 0 or 1).

4.1.2 Những khối chức năng tham gia thực thi lệnh:

a. *AND Rd,Rs,Rt* → *Reg[Rd] = Reg[Rs] AND Reg[Rt]*

Tất cả, ngoại trừ Bộ nhớ dữ liệu và bộ Cộng địa chỉ rẽ nhánh

b. *SW Rt,Offs(Rs)* → *Mem[Reg[Rs] + Offs] = Reg[Rt]*

Tất cả, ngoại trừ bộ Cộng địa chỉ rẽ nhánh và cổng ghi thanh ghi

Different execution units and blocks of digital logic have different latencies (time needed to do their work). In Figure 4.2 there are seven kinds of major blocks. Latencies of blocks along the critical (longest-latency) path for an instruction determine the minimum latency of that instruction. For the remaining three problems in this exercise, assume the following resource latencies:

	I-Mem	Add	Mux	ALU	Regs	D-Mem	Control
a.	200ps	70ps	20ps	90ps	90ps	250ps	40ps
b.	750ps	200ps	50ps	250ps	300ps	500ps	300ps

4.1.4 [5] <4.1> What is the critical path for an MIPS AND instruction?

4.1.5 [5] <4.1> What is the critical path for an MIPS load (LD) instruction?

4.1.6 [10] <4.1> What is the critical path for an MIPS BEQ instruction?

4.1.4

Lệnh AND qua các bước: (I-Mem, Regs, Mux, ALU, and Mux)

4.1.5
Lệnh lw qua các bước: : (I-Mem, Regs, Mux, ALU, D-Mem, Mux)