ĐHBK Tp HCM-Khoa Đ-ĐT
BMĐT
GVPT: Hồ Trung Mỹ
Môn học: Dụng cụ bán dẫn

Chương 6

FET

(Field Effect Transistor)

Transistor hiệu ứng trường

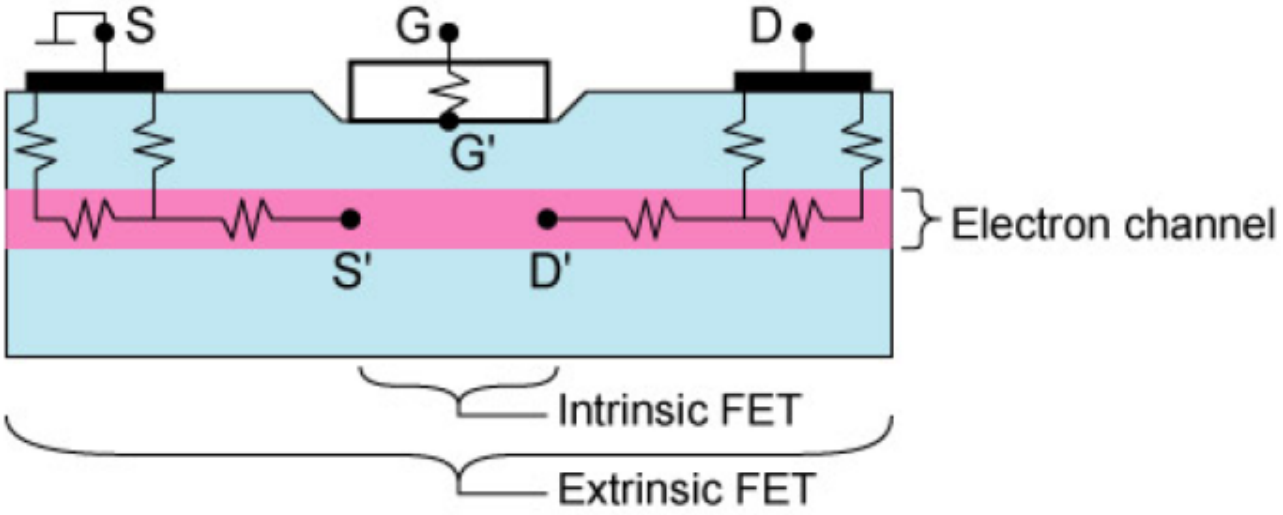
Nội dung

- Giới thiệu
- Cấu tạo và nguyên tắc hoạt động
- Đặc tuyến I-V
- Các hiệu ứng thứ cấp
- Mô hình tín hiệu nhỏ - mạch tương đương tín hiệu nhỏ
- Mô hình tín hiệu nhỏ ở tần số cao
- Các ứng dụng của JFET: KĐ, KĐ chopper, khóa analog, nguồn dòng...

6.5 Mạch tương đương tín hiệu nhỏ

Intrinsic and extrinsic FET

Intrinsic and extrinsic FET

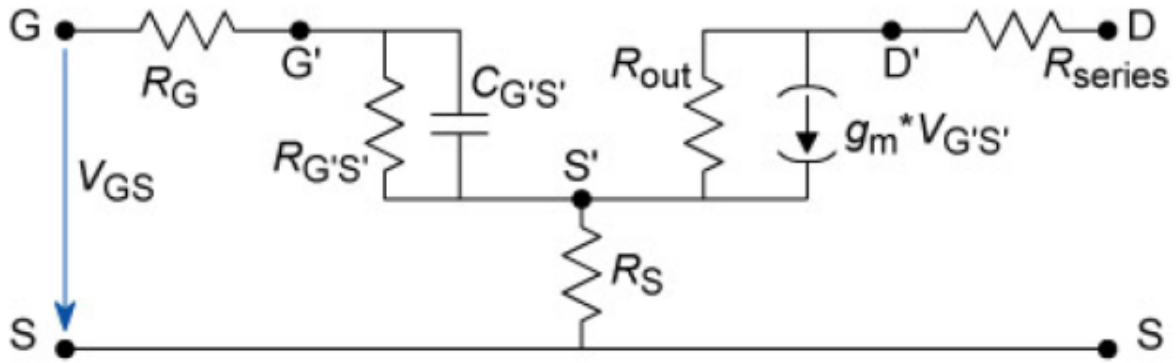


- Extrinsic FET (real FET) has terminals S, G, and D.
- Intrinsic FET has terminals S', G', and D'.
- Intrinsic FET = inner FET = ideal FET
- Intrinsic FET + Parasitics = Extrinsic FET

Equivalent circuit of intrinsic and extrinsic FET

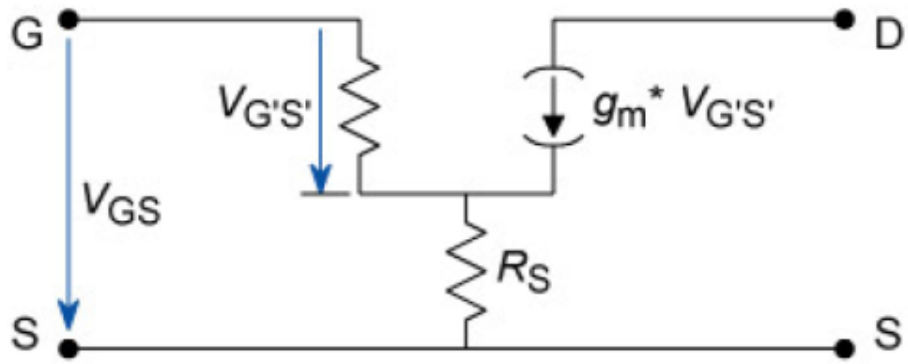
Intrinsic FET

Extrinsic FET



- R_G is very small because the gate is a metal
- $R_{G'S'}$ is very large because of the gate insulator
- R_{out} represents a possible current path through the substrate. R_{out} is very large

Extrinsic and intrinsic transconductance



- R_S = source resistance
- Voltage drop across source resistance = $R_S\, g_m^*\, V_{GS}^*$
- Intrinsic transconductance: $$g_m^* = \frac{dI_D}{dV_{G'S'}}$$
- Extrinsic transconductance: $$g_m = \frac{dI_D}{dV_{GS}}$$

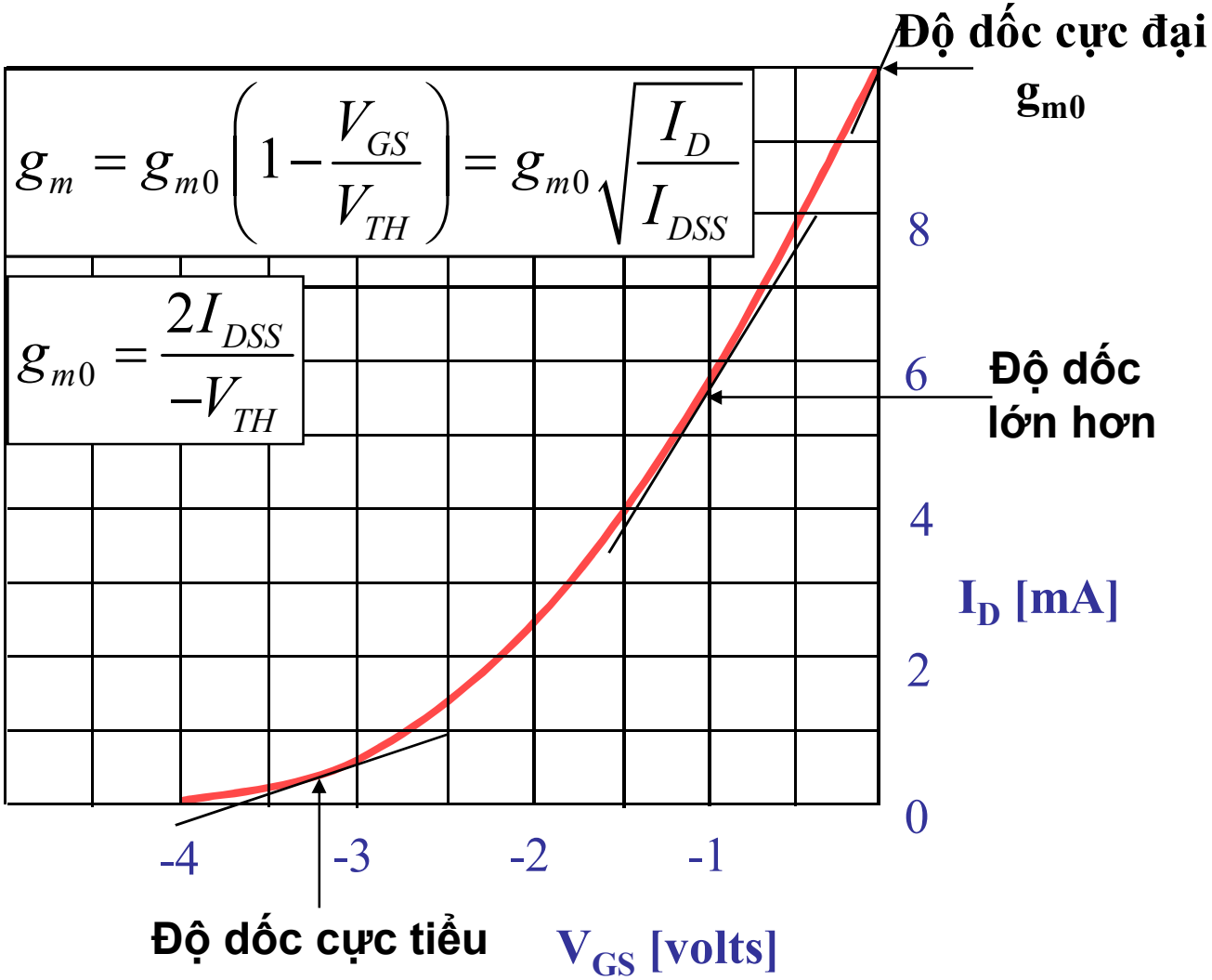
Hỗ dẫn

- Cho biết tác động của điện áp cổng lên dòng máng:

$$g_m = i_d/v_{gs}$$

- Đơn vị của hỗ dẫn là micromho (μmho) hay microsiemen (μS).
- g_m là độ dốc của đường cong hỗ dẫn.
- g_{m0} là giá trị tối đa và xảy ra ở $V_{GS} = 0$.

Hỗ dẫn của N-JFET có $V_{TH} = -4V$



Đặc tuyến g_m

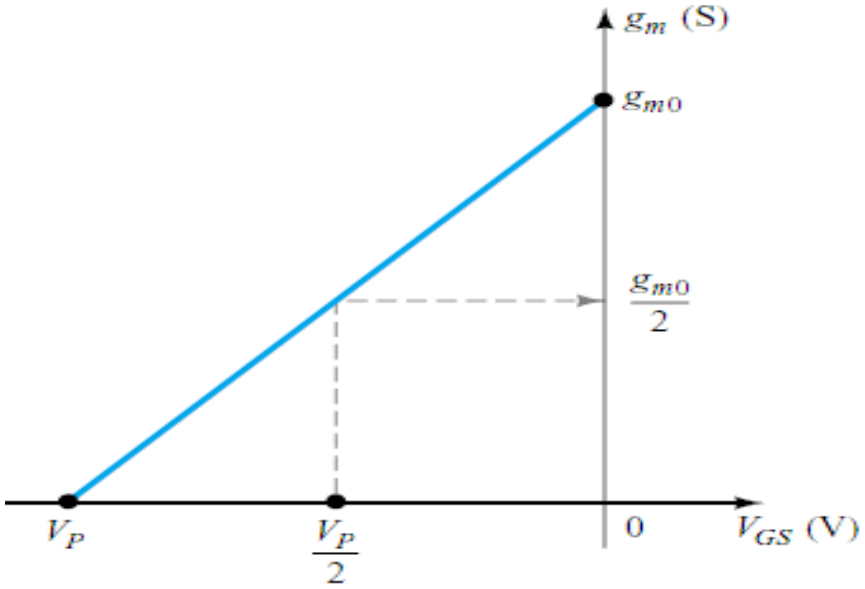
$$1 - \frac{V_{GS}}{V_P} = \sqrt{\frac{I_D}{I_{DSS}}}$$

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_P}\right) = g_{m0}\sqrt{\frac{I_D}{I_{DSS}}}$$

$$I_D = I_{DSS} \Rightarrow g_m = g_{m0}$$

$$I_D = \frac{I_{DSS}}{2} \Rightarrow g_m = \frac{g_{m0}}{\sqrt{2}} = 0,707 g_{m0}$$

$$I_D = \frac{I_{DSS}}{4} \Rightarrow g_m = \frac{g_{m0}}{2}$$



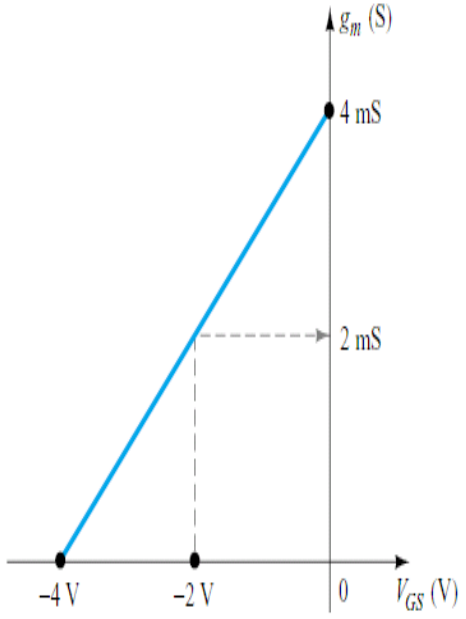
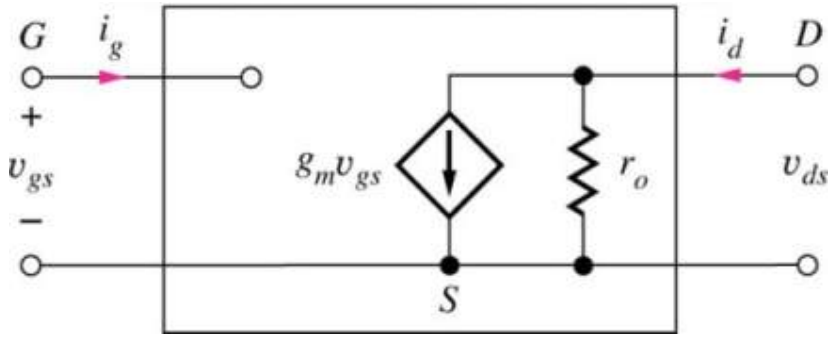


Figure 9.4 Plot of g_m vs. V_{GS} for a JFET with I_{DSS} = 8 mA and V_P = −4 V.

Mô hình tín hiệu nhỏ của N-JFET

(dùng cho JFET trong miền bão hòa)



Để làm việc với tín hiệu nhỏ, giới hạn tín hiệu vào:

$$\left|v_{gs}\right| < 0.2\left(V_{GS} - V_{TH}\right)$$

Vì JFET thường làm việc với tiếp xúc PN G-S được phân cực ngược:

$$I_G \approx 0$$

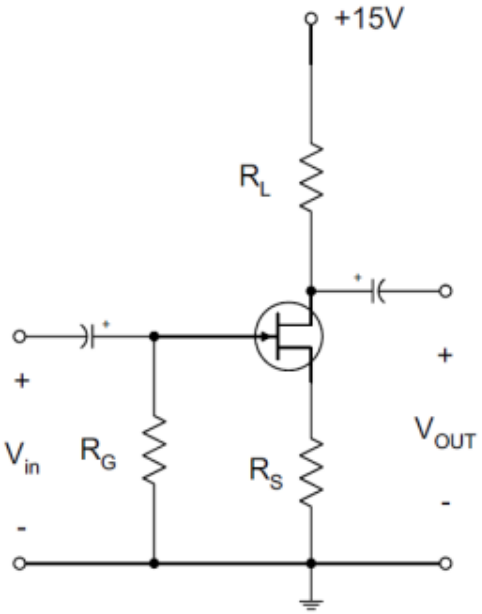
$$r_{gs} = \infty$$

Hệ số khuếch đại nội được cho bởi:

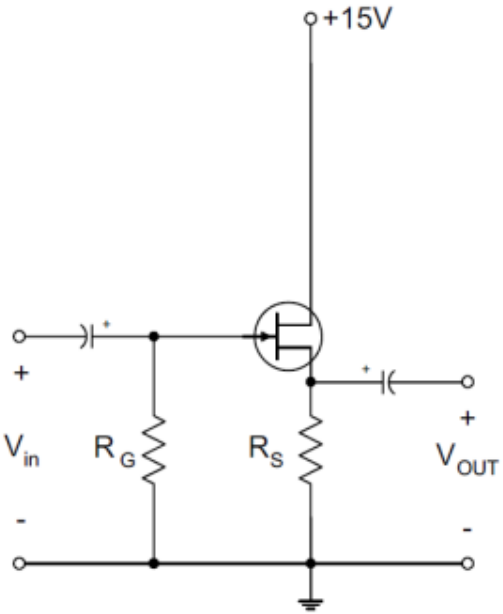
$$\mu_f = g_m r_0 = \frac{2\left(V_A + V_{DS}\right)}{V_{GS} - V_{TH}} \approx \frac{2V_A}{V_{GS} - V_{TH}} = 2\frac{V_A}{-V_{TH}}\sqrt{\frac{I_{DSS}}{I_D}}$$

Mạch KĐ dùng JFET

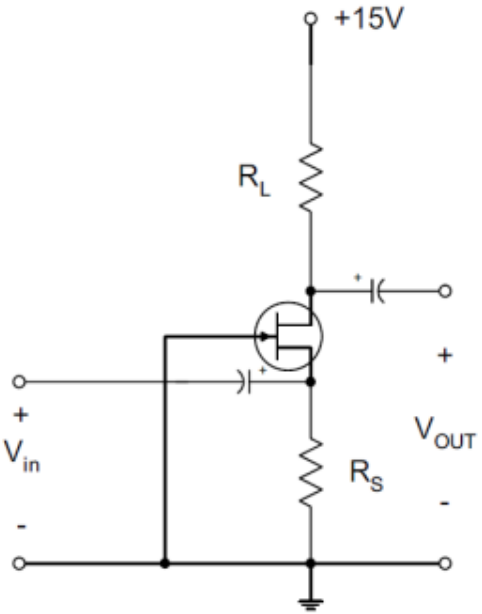
Các cấu hình mạch KĐ dùng N-JFET



[a] Common Source Amplifier



[b] Common Drain [Source Follower] Amplifier



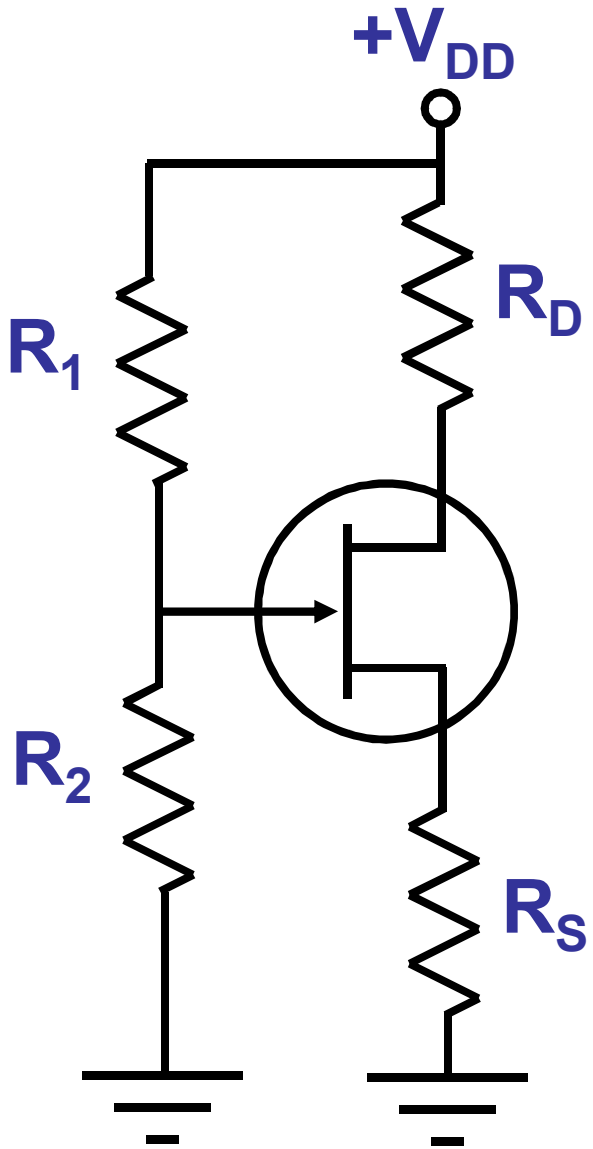
[c] Common Gate Amplifier

Tóm tắt các công thức trong mạch KĐ dùng JFET

Characteristic	Common Source	C Source with R_S	Common Drain [Source Follower]	Common Gate
Voltage Gain [if $r_{ds} >> R_L$]	$A_v = -g_m R_L$	$A_v = \frac{-g_m R_L}{1 + g_m R_S}$	$A_v = \frac{g_m R_S}{1 + g_m R_S}$	$A_v = \frac{g_m R_L}{1 + g_m R_i + \frac{R_i}{R_S}}$ R_i = generator resistance
Current Gain	$\frac{I_D}{I_S}$ Very large!	$\frac{I_D}{I_S}$ Very large!	$\frac{I_D}{I_S}$ Very large!	$A_i = \frac{g_m R_S}{g_m R_S + 1}$
Input Impedance	R_G	R_G	R_G	$\frac{R_S}{g_m R_S + 1} = \frac{1}{g_m} // R_S$
Output Impedance	R_L [if $r_{ds} >> R_L$]	R_L [if $r_{ds} >> R_L$]	$\frac{R_S}{g_m R_S + 1} = \frac{1}{g_m} // R_S$	R_L [if $r_{ds} >> R_L$]
Phase Reversal?	Yes	Yes	No	No

Phân cực JFET trong miền tích cực

Phân cực bằng cầu chia áp



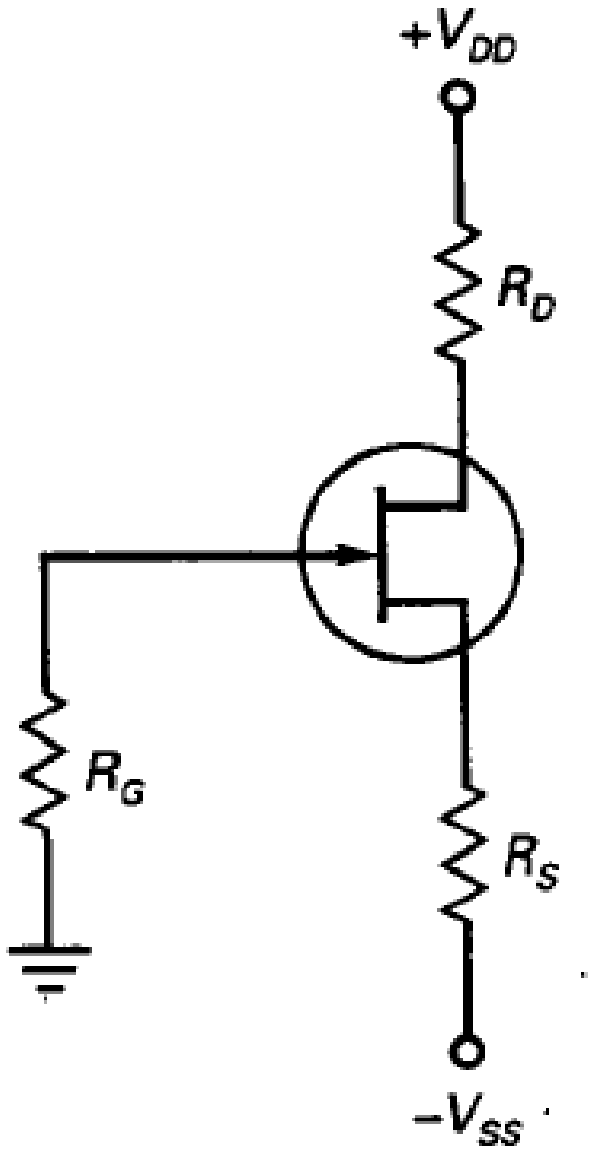
Phân cực cổng không thích hợp cho miền tích cực.

$$I_{D(sat)} = \frac{V_{DD}}{R_D + R_S}$$

$$V_S = V_G - V_{GS}$$

$$I_{DQ} = \frac{V_G - V_{GS}}{R_S}$$

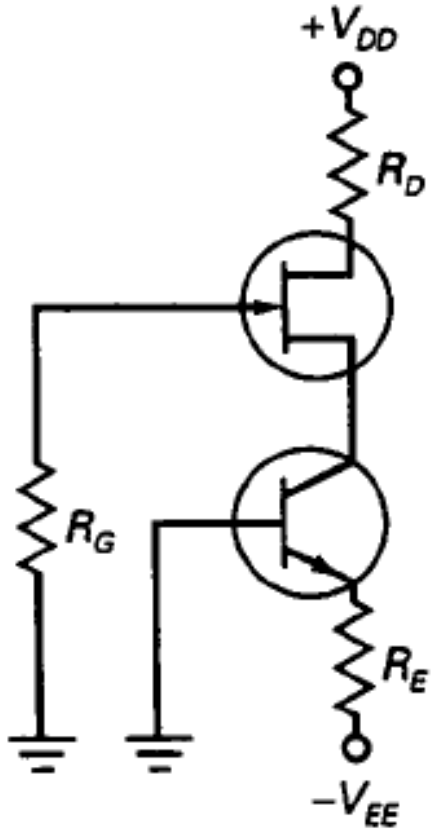
Phân cực nguồn dùng 2 nguồn cấp điện



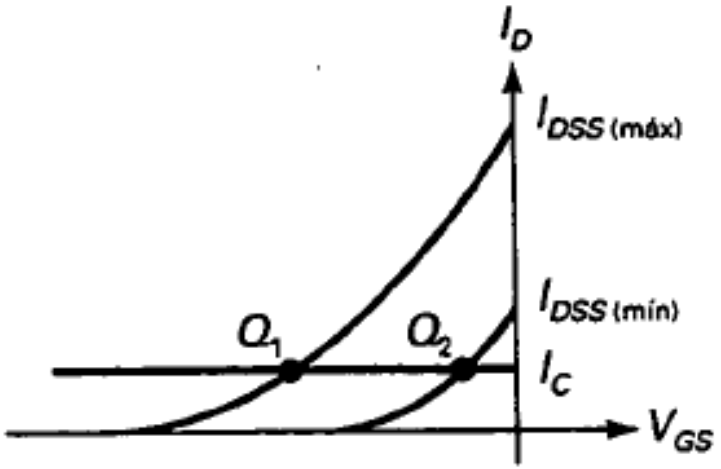
$$I_D = \frac{V_{SS} - V_{GS}}{R_S} \approx \frac{V_{SS}}{R_S}$$

Phân cực bằng nguồn dòng

$$I_D = \frac{V_{EE} - V_{BE}}{R_E}$$

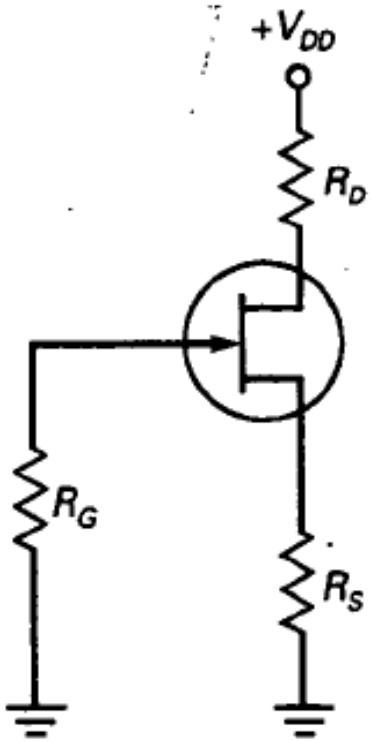


(a)

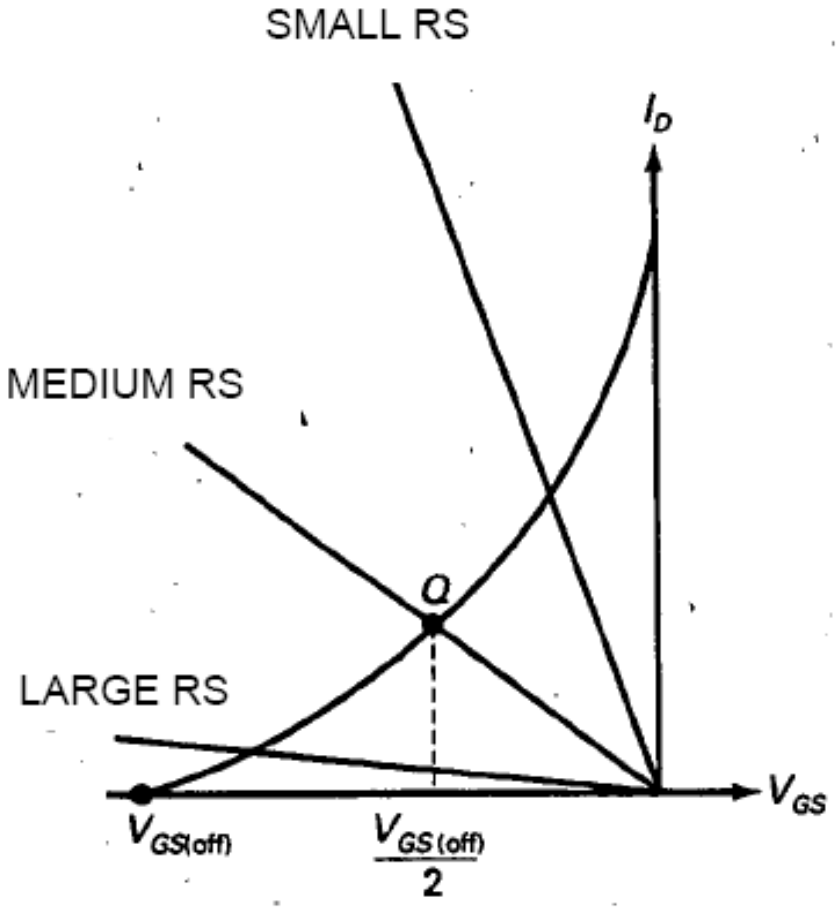


(b)

Tự phân cực



(a)



(b)

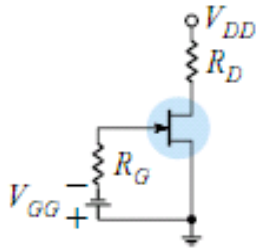
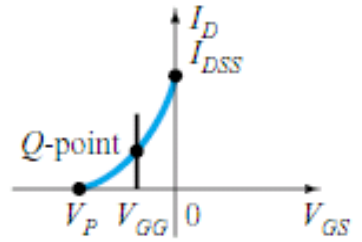
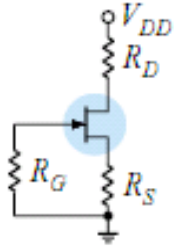
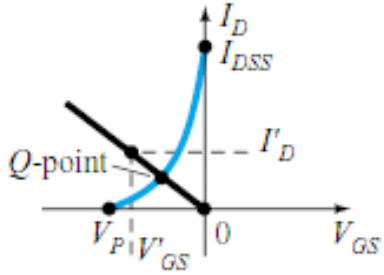
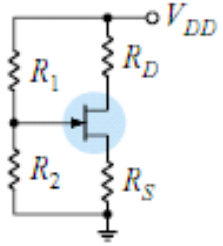
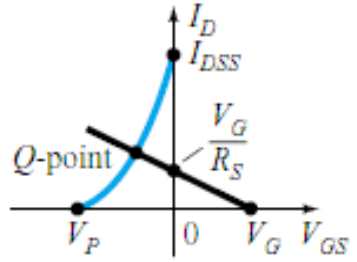
$$V_S = I_D R_S$$

$$V_{GS} = -I_D R_S$$

Với R_S trung bình:

$$R_S \approx R_{DS}$$

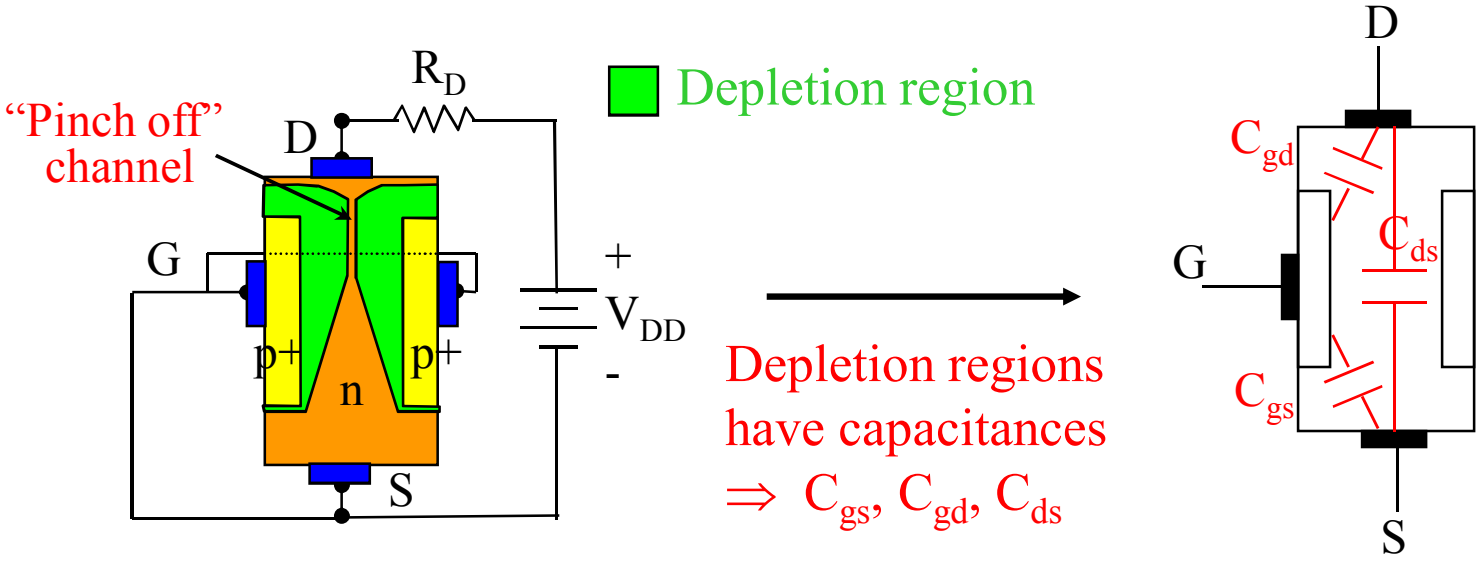
Tóm tắt phân cực JFET kênh N

Type	*Configuration*	*Pertinent Equations*	*Graphical Solution*
JFET Fixed-bias		$V_{GS_Q} = -V_{GG}$ $V_{DS} = V_{DD} - I_D R_S$	
JFET Self-bias		$V_{GS} = -I_D R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	
JFET Voltage-divider bias		$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_D R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	

6.6 Mô hình JFET tín hiệu nhỏ ở tần số cao

FET high-frequency small-signal model

Depletion capacitances and Miller effect



In active region

E.g. C_{gs} = 3pF, C_{ds} = 1pF, C_{gd} = 2.8pF.

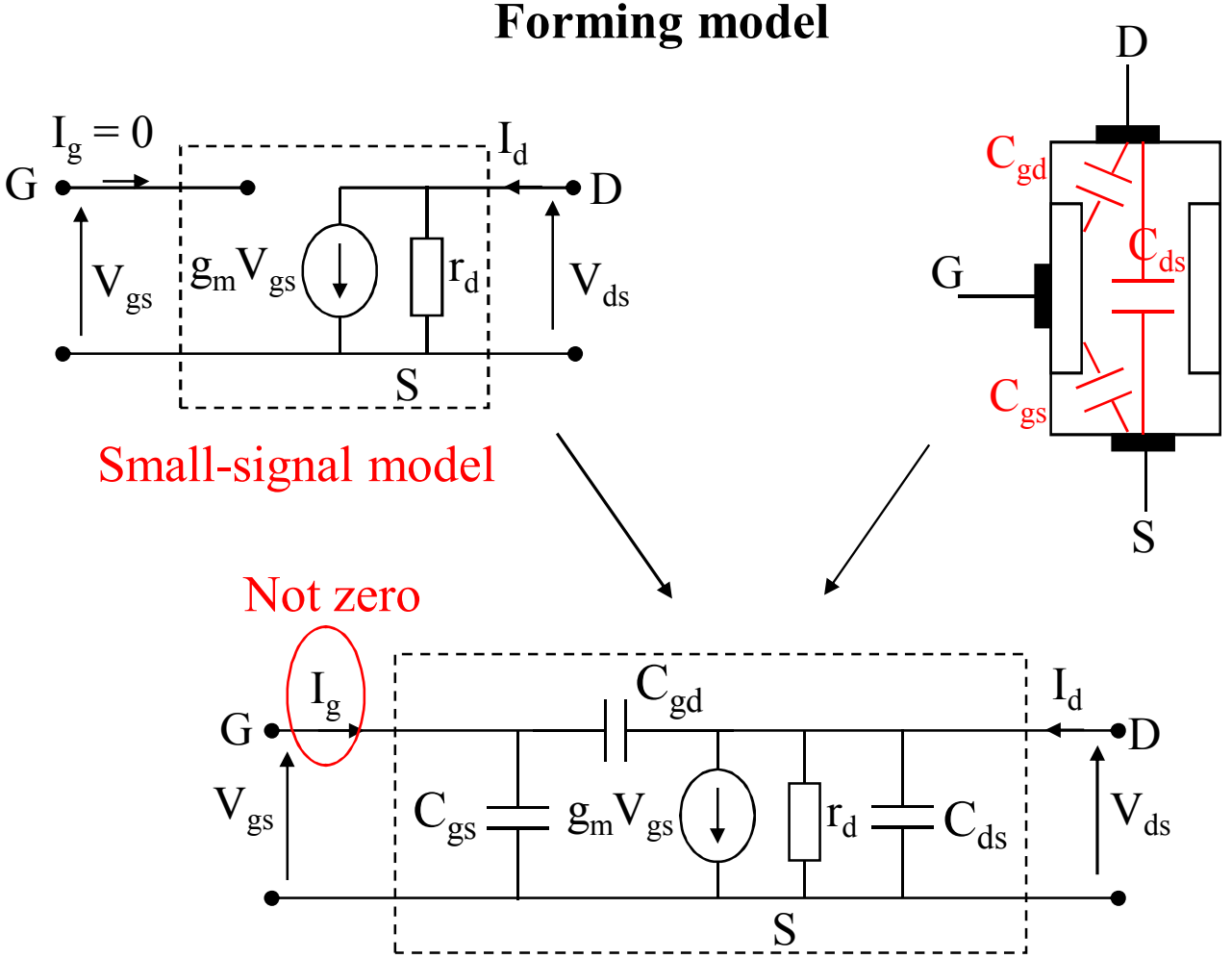
C_{gs} is generally the biggest in all FET devices

BUT $C_A = C_{gd}(1 - A_V)$ gives the largest effect ($C_A >> C_{gs}$)

Hence, this is called Miller capacitance effect or Miller effect.

FET high-frequency small-signal model

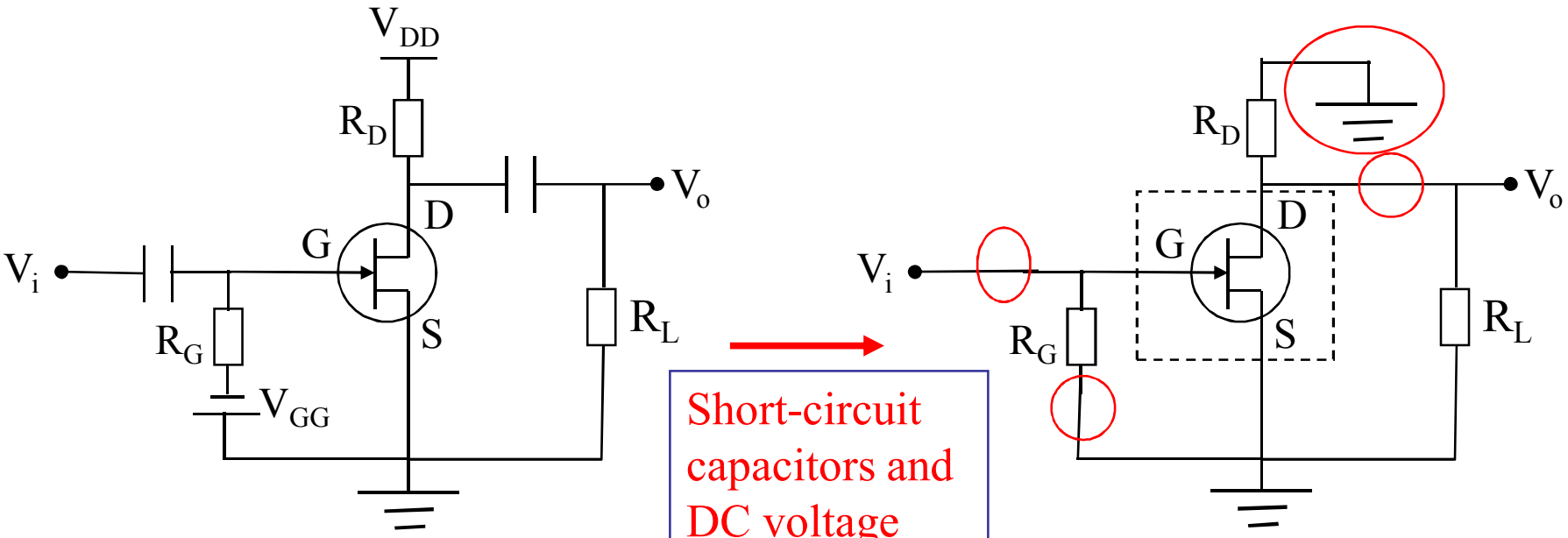
Forming model



High-frequency small-signal model

FET common source amplifier at high frequency

AC equivalent circuit

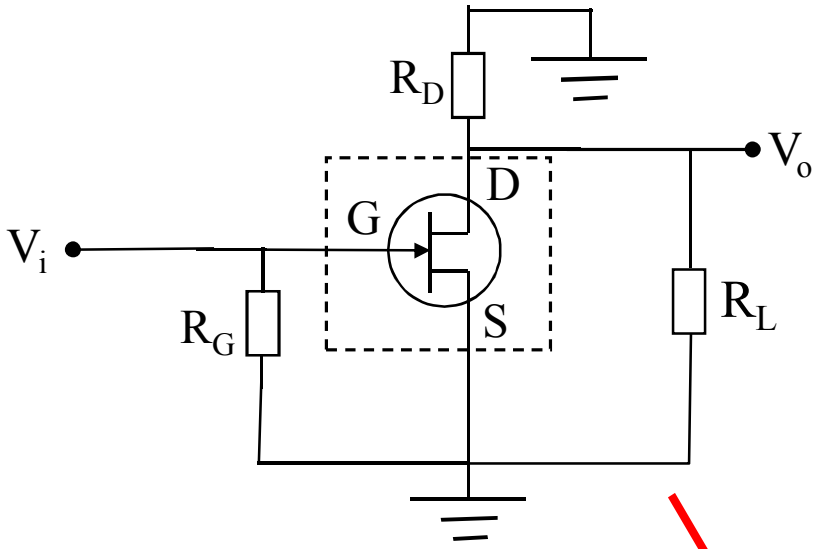


CS amplifier circuit

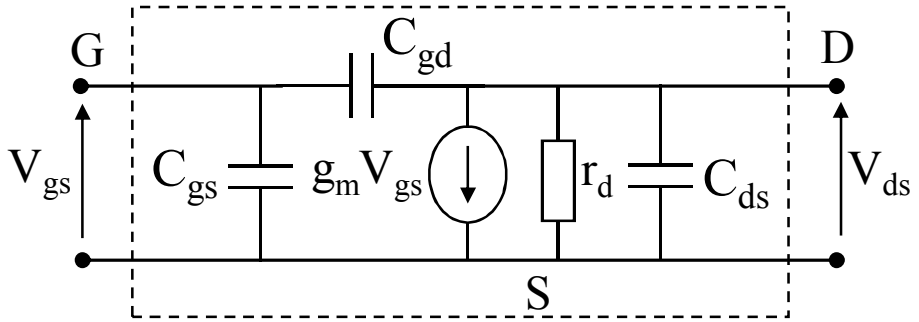
AC equivalent circuit

FET common source amplifier at high frequency

High-frequency small-signal model circuit



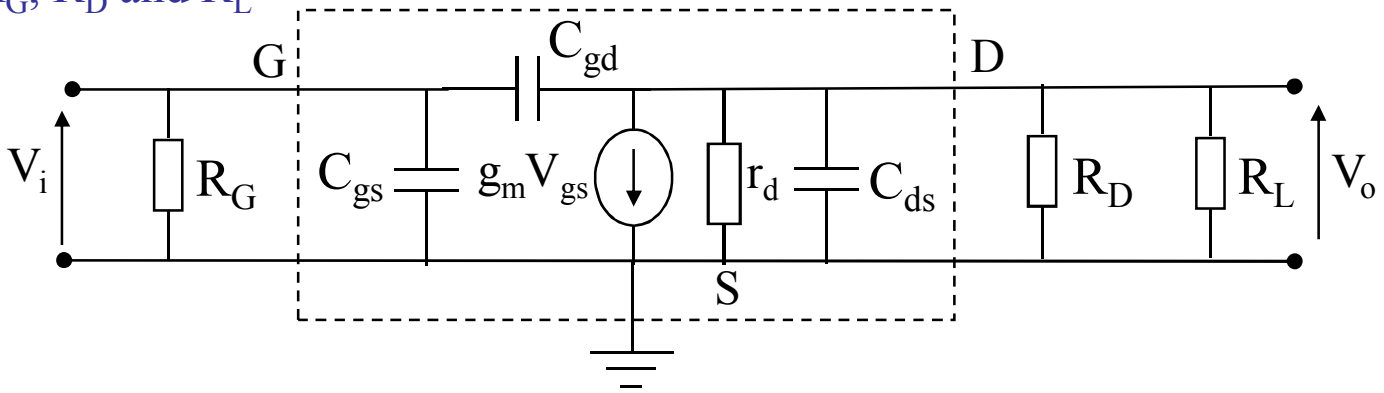
AC equivalent circuit



High-frequency small-signal model

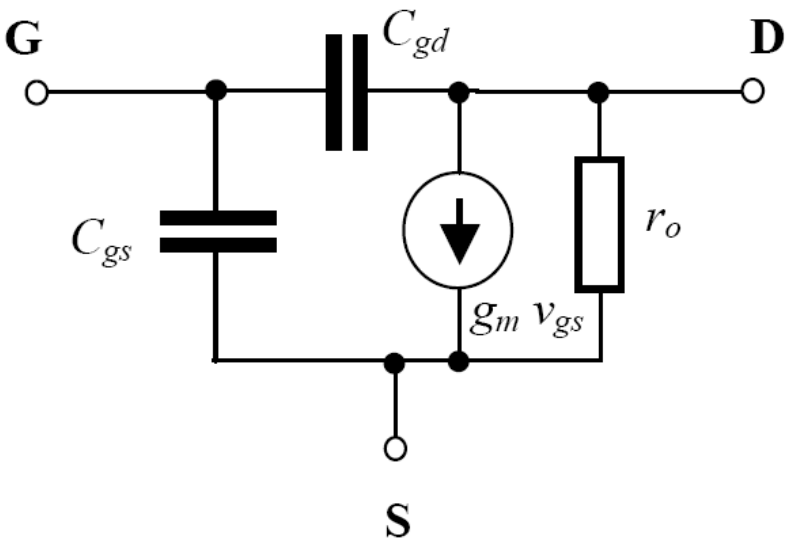
Step 1:
Put down R_G, R_D and R_L

Step 2:
Put down model



High-frequency small-signal model circuit

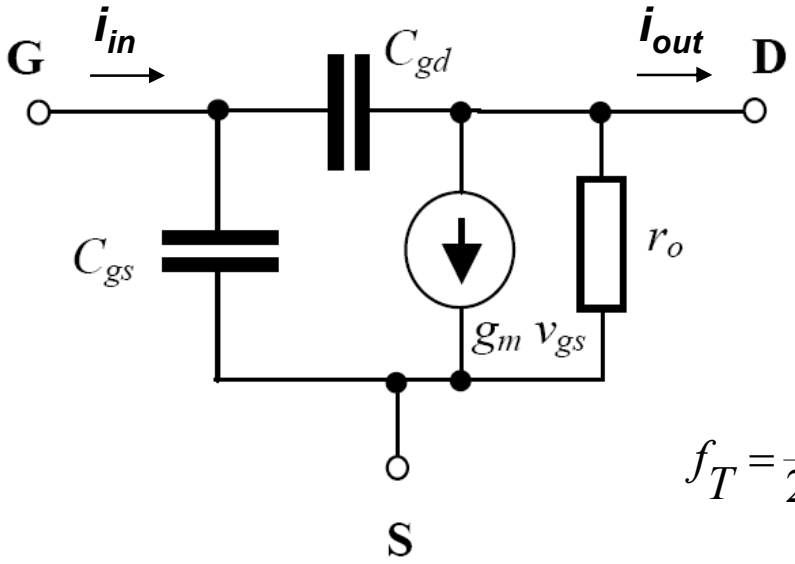
Mô hình JFET tín hiệu nhỏ (được đơn giản hóa) ở tần số cao



- r_o là điện trở ra do sự điều chế chiều dài kênh dẫn (nghĩa là sự phụ thuộc của I_D vào V_{DS}), trị tiêu biểu của r_o = 10KΩ → 1000KΩ
- C_{gs} : điện dung giữa G và S
- C_{gd}: điện dung giữa G và D

Tần số cắt f_T

- Tần số cắt được định nghĩa là tần số mà tại đó hệ số khuếch đại dòng $i_{out}/i_{in} = 1$.



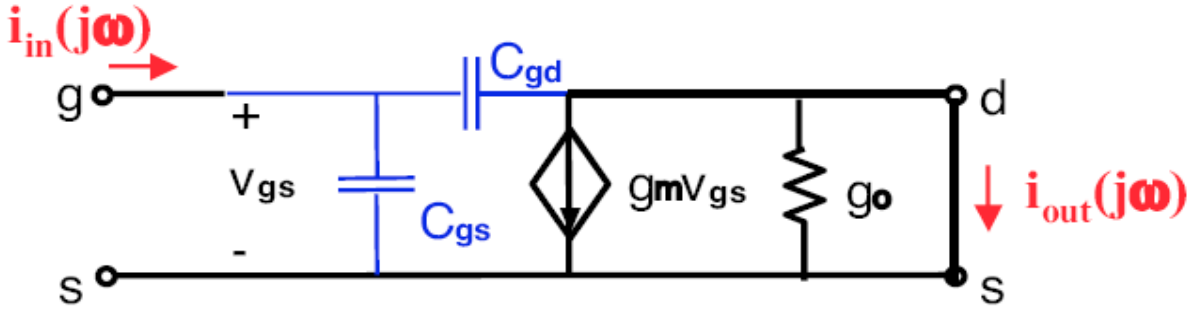
$$i_{in} = 2\pi f C_{gs} v_g$$

$$i_{out} = g_m v_g$$

$$f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})} \approx \frac{g_m}{2\pi C_{gs}} \approx \frac{\mu_n q N_D a^3}{2\pi\varepsilon_s L^2}$$

High frequency models - short circuit current gain

A measure of the high frequency performance of a transistor is obtained by calculating its short circuit current gain, $\beta_{sc}(j\omega)$, and finding the frequency at which its magnitude is 1:



$$\beta_{sc}(j\omega) = \frac{i_{out}(j\omega)}{i_{in}(j\omega)} = \frac{j\omega C_{gd} v_{gs} - g_m v_{gs}}{j\omega\left(C_{gs} + C_{gd}\right)v_{gs}} = \frac{j\omega\left(C_{gd}/g_m\right) - 1}{j\omega\left(C_{gs} + C_{gd}\right)/g_m}$$

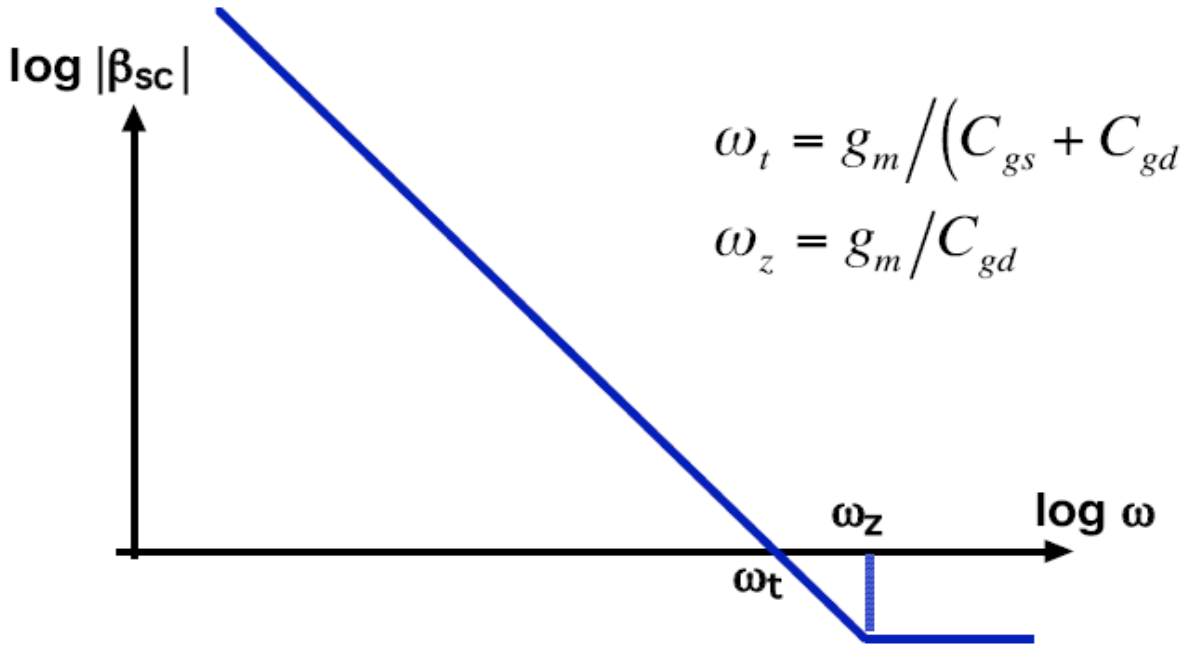
$$\left|\beta_{sc}(j\omega)\right| \approx \frac{g_m}{\omega\left(C_{gs} + C_{gd}\right)} \quad for\ \omega << g_m/C_{gd}$$

$$and\ thus,\ \left|\beta_{sc}(j\omega)\right| = 1\ @\ \omega_t = g_m/\left(C_{gs} + C_{gd}\right)$$

$$Note: C_{gs} >> C_{gd},\ so\ the\ assumption\ is\ valid,\ i.e.,\ \omega_t << g_m/C_{gd}$$

High frequency models - f_t

A useful way to visualize this result is make a log-log plot of the magnitude of the short circuit current gain verses frequency, i.e., log $|\beta_{sc}(j\omega)|$, vs. log ω. This is called a Bode plot:



$$\omega_t = g_m / \left(C_{gs} + C_{gd} \right) \approx g_m / C_{gs}$$

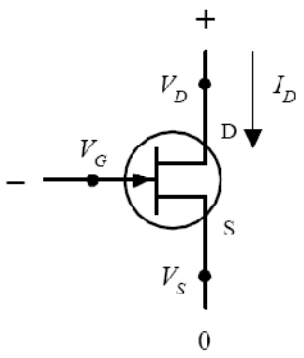
$$\omega_z = g_m / C_{gd}$$

Note: Usually $C_{gs} >> C_{gd}$, so typically $\omega_z >> \omega_t$.

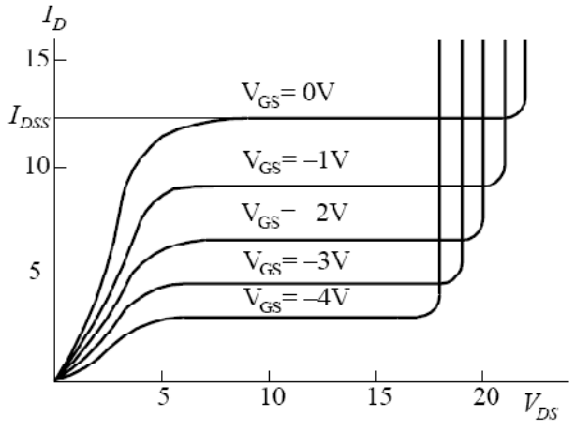
Tóm tắt JFET

Tóm tắt đặc tuyến JFET

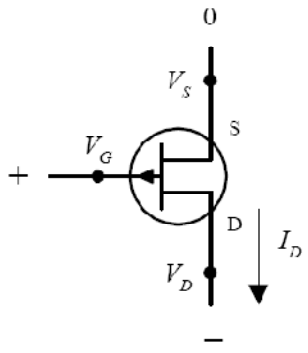
N-CHANNEL JFET



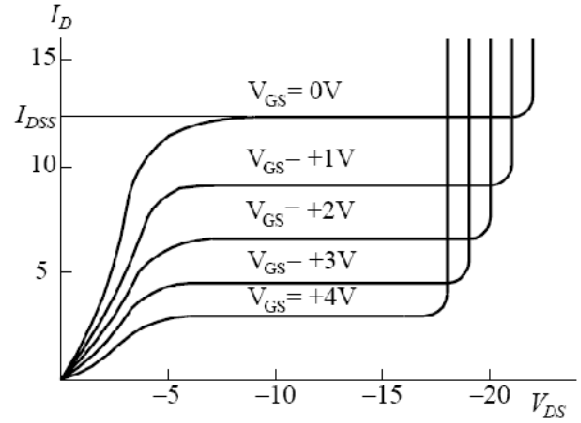
N-CHAN CURVES



P-CHANNEL JFET



P-CHAN CURVES



OHMIC REGION JFET is just beginning to resist. It acts like a variable resistor.

SATURATION REGION JFET is most strongly influenced by gate-source voltage, hardly at all influenced by the drain-source voltage.

CUTOFF VOLTAGE ($V_{GS,off}$) Particular gate-source voltage where JFET acts like an open circuit (channel resistance is at its maximum).

BREAKDOWN VOLTAGE (BV_{DS}) The voltage across the drain and source that caused current to "break through" the JFET's resistive channel.

DRAIN-CURRENT FOR ZERO BIAS (I_{DSS}) Represents the drain current when gate-source voltage is zero volts (or gate is connected to source, $V_{GS} = 0\,V$).

TRANSCONDUCTANCE (g_m) Represents the rate of change in the drain current with the gate-source voltage when the drain-to-source voltage is fixed for a particular V_{DS}. It is analogous to the transconductance ($1/R_{tr}$) for bipolar transistors.

Tóm tắt công thức JFET

DRAIN CURRENT (OHMIC REGION)

$$I_D = I_{DSS}\left[2\left(1 - \frac{V_{GS}}{V_{GS,\text{off}}}\right)\frac{V_{DS}}{-V_{GS,\text{off}}} - \left(\frac{V_{DS}}{V_{GS,\text{off}}}\right)^2\right]$$

DRAIN CURRENT (ACTIVE REGION)

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS,\text{off}}}\right)^2$$

DRAIN-SOURCE RESISTANCE

$$R_{DS} = \frac{V_{DS}}{i_D} \approx \frac{V_{GS,\text{off}}}{2I_{DSS}(V_{GS} - V_{GS,\text{off}})} = \frac{1}{g_m}$$

ON RESISTANCE

$$R_{DS,\text{on}} = \text{constant}$$

DRAIN-SOURCE VOLTAGE

$$V_{DS} = V_D - V_S$$

TRANSCONDUCTANCE

$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS}} = \frac{1}{R_{DS}}$$

$$= g_{m_0}\left(1 - \frac{V_{GS}}{V_{GS,\text{off}}}\right) = g_{m_0}\sqrt{\frac{I_D}{I_{DSS}}}$$

TRANSCONDUCTANCE FOR SHORTED GATE

$$g_{m_0} = -\frac{2I_{DSS}}{V_{GS,\text{off}}}$$

An n-channel JFET's $V_{GS,\text{off}}$ is negative.
A p-channel JFET's $V_{GS,\text{off}}$ is positive.

$V_{GS,\text{off}}$, I_{DSS} are typically the knowns (you get their values by looking them up in a data table or on the package).

Typical JFET values:

I_{DSS}: 1 mA to 1 A

$V_{GS,\text{off}}$:
–0.5 to –10 V (n-channel)
0.5 to 10 V (p-channel)

$R_{DS,\text{on}}$: 10 to 1000 Ω

BV_{DS}: 6 to 50 V

g_m at 1 mA:
500 to 3000 μmho

Một số đặc tính của JFET kênh N thực tế

TABLE 3.1. JFETs

Type	BV_{GSS} (V)	I_{DSS} min (mA)	I_{DSS} max (mA)	$V_{GS(OFF)}$ V_P min (V)	$V_{GS(OFF)}$ V_P max (V)	C_{gs} max (pF)	C_{gd} max (pF)	Comments
n-channel								
2N4117A-	40	0.03	0.09	0.6	1.8	3	1.5	low leakage: 1pA (max)
2N4119A	40	0.24	0.6	2	6	4	1.5	
2N4338	50	0.2	0.6	0.3	1	6	2	0 5fA/√Hz @ 100Hz
2N4416	30	5	15	2.5	6	4	0.8	VHF low noise: <2dB@100MHz
2N4867A-	40	0.4	1.2	0.7	2	25	5	low freq, low noise:
2N4869A	40	2.5	7.5	1.8	5	25	5	10nV/√Hz(max)@10Hz
2N5265-	60	0.5	1	–	3	7	2	series of 6, tight I_{DSS} spec;
2N5270	60	7	14	–	8	7	2	2N5358-64 p-chan complement
2N5432	25	150	–	4	10	30	15	switch: R_{ON}=5Ω(max)
2N5457-	25	1	5	0.5	6	7	3	general purpose;
2N5459	25	4	16	2	8	7	3	2N5460-2 p-chan complement
2N5484-	25	1	5	0.3	3	5	1	low noise RF; inexpensive
2N5486	25	8	20	2	6	5	1	
2SK117	50	0 6	14	0.2	1.5	13[t]	3[t]	ultra low noise: 1nV/√Hz
2SK147	40	5	30	0.3	1 2	75[t]	15[t]	ultra low noise: 0.7nV/√Hz

Một số đặc tính của JFET kênh P thực tế

Type	BV_{GSS} (V)	I_{DSS} min (mA)	I_{DSS} max (mA)	$V_{GS(OFF)}$ V_P min (V)	$V_{GS(OFF)}$ V_P max (V)	C_{gs} max (pF)	C_{gd} max (pF)	Comments
p-channel								
2N5114	30	30	90	5	10	25	7	switch: R_{ON}=75Ω(max)
2N5358-	40	0 5	1	0.5	3	6	2	series of 7, tight I_{DSS} spec;
2N5364	40	9	18	2.5	8	6	2	2N5265-70 n-chan complement
2N5460-	40	1	5	0.75	6	7	2	general purpose;
2N5462	40	4	16	1.8	9	7	2	2N5457-9 n-chan complement
2SJ72	25	5	30	0.3	2	185[t]	55[t]	ultra low noise: 0.7nV/√Hz

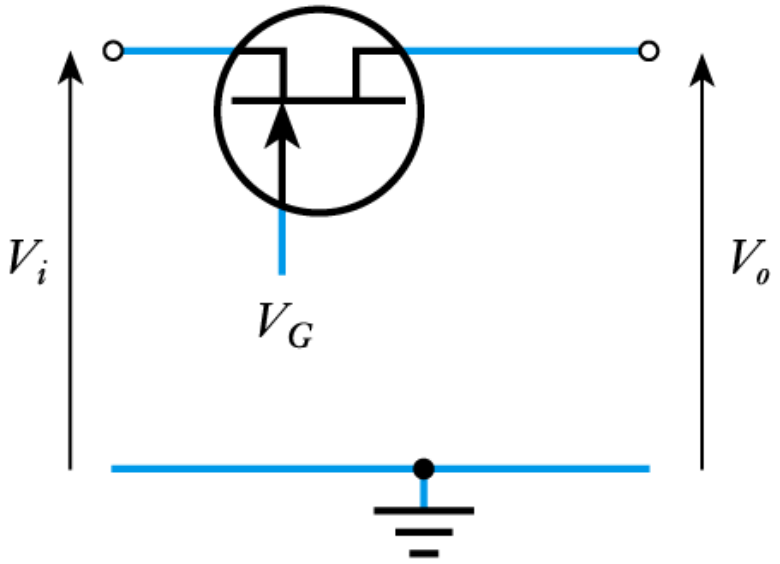
(t) typical.

6.7 Một số ứng dụng của JFET

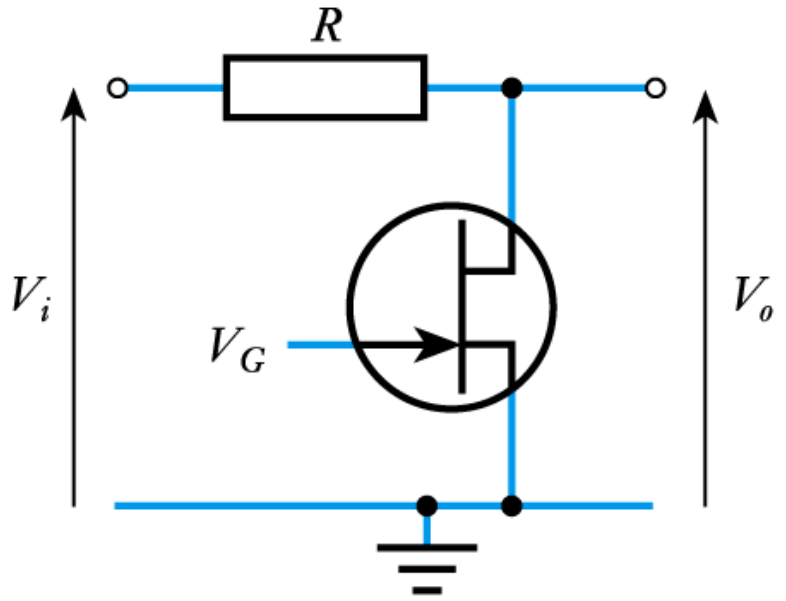
- Khóa điện tử analog (Analog switch)
- Mạch khuếch đại
- Điện trở được điều khiển bằng áp
- Nguồn dòng
- . . .

JFET làm công tắc analog (Analog switch)

- **A FET as an analogue switch**

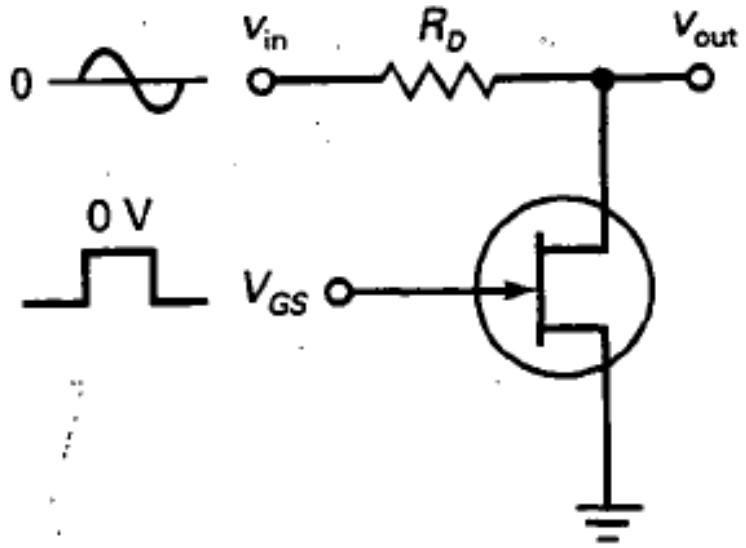


(a) A series switch

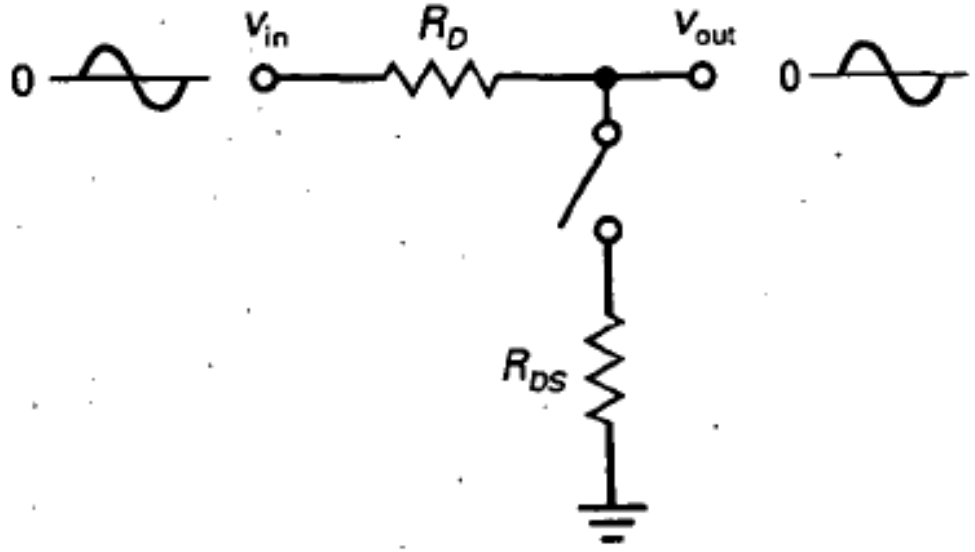


(b) A shunt switch

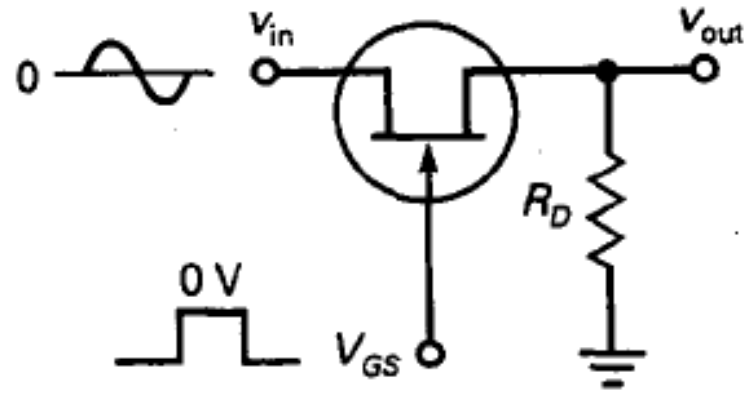
Analog Switch



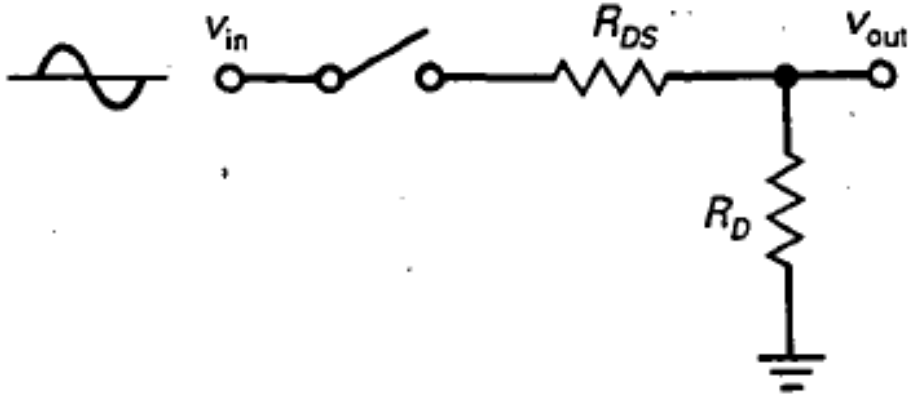
(a)



(b)

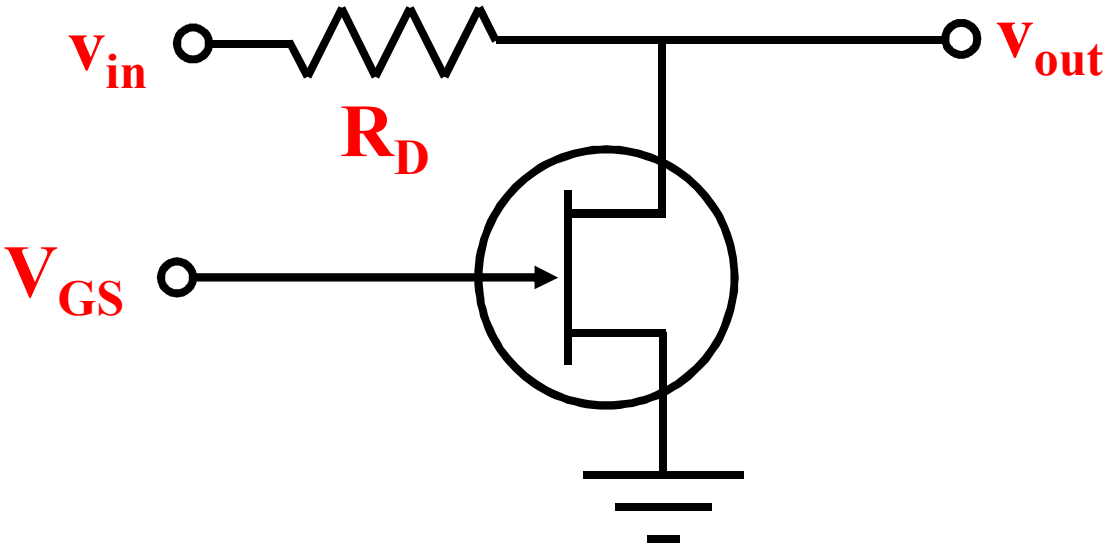


(c)



(d)

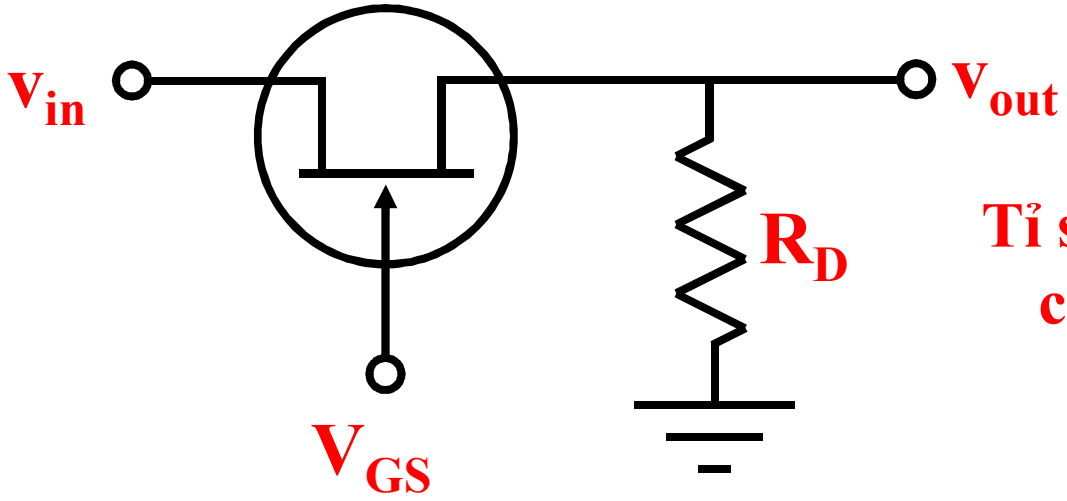
Shunt analog switch



$v_{in} < 100$ mV

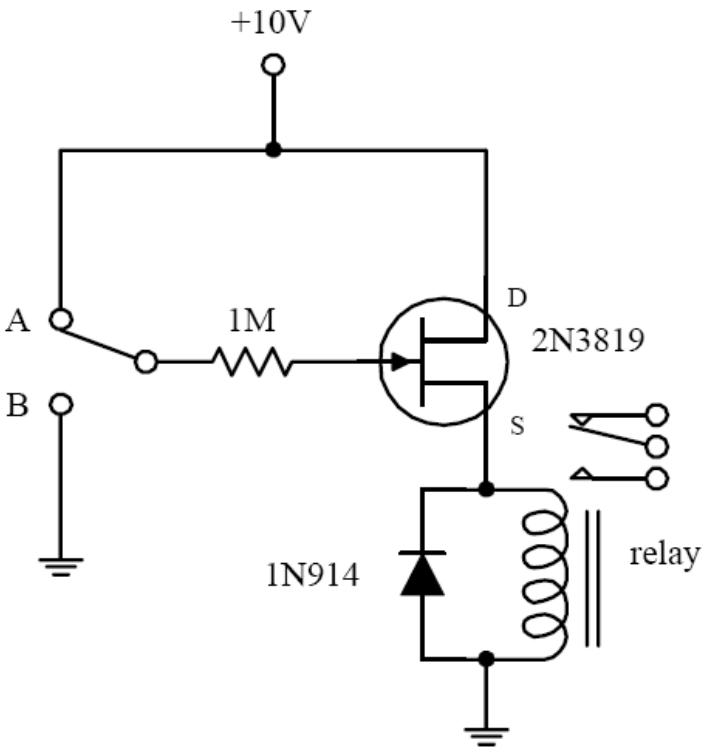
$R_D >> R_{DS}$

Series analog switch



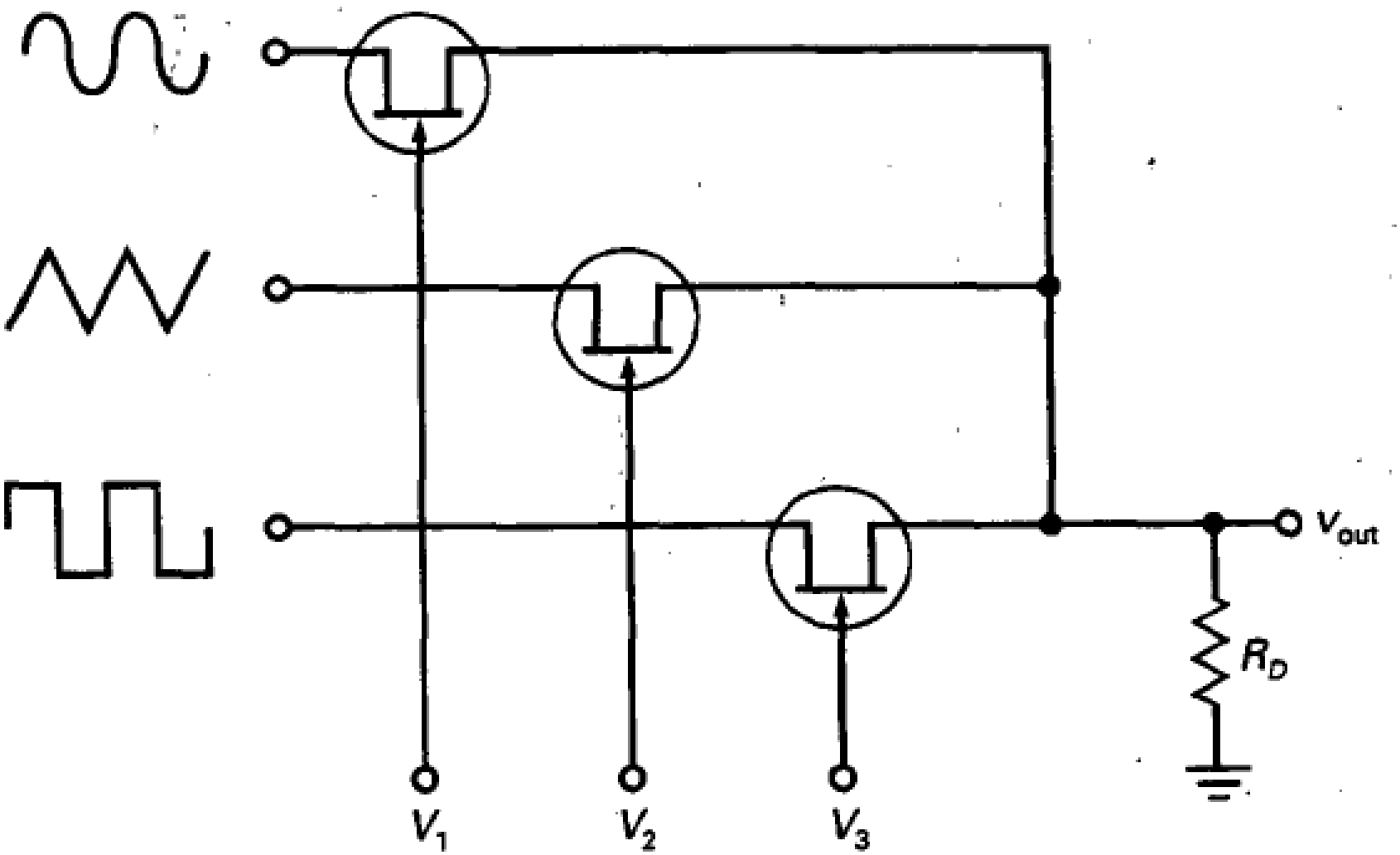
Tỉ số ON-OFF tốt hơn công tắc song song

RELAY DRIVER

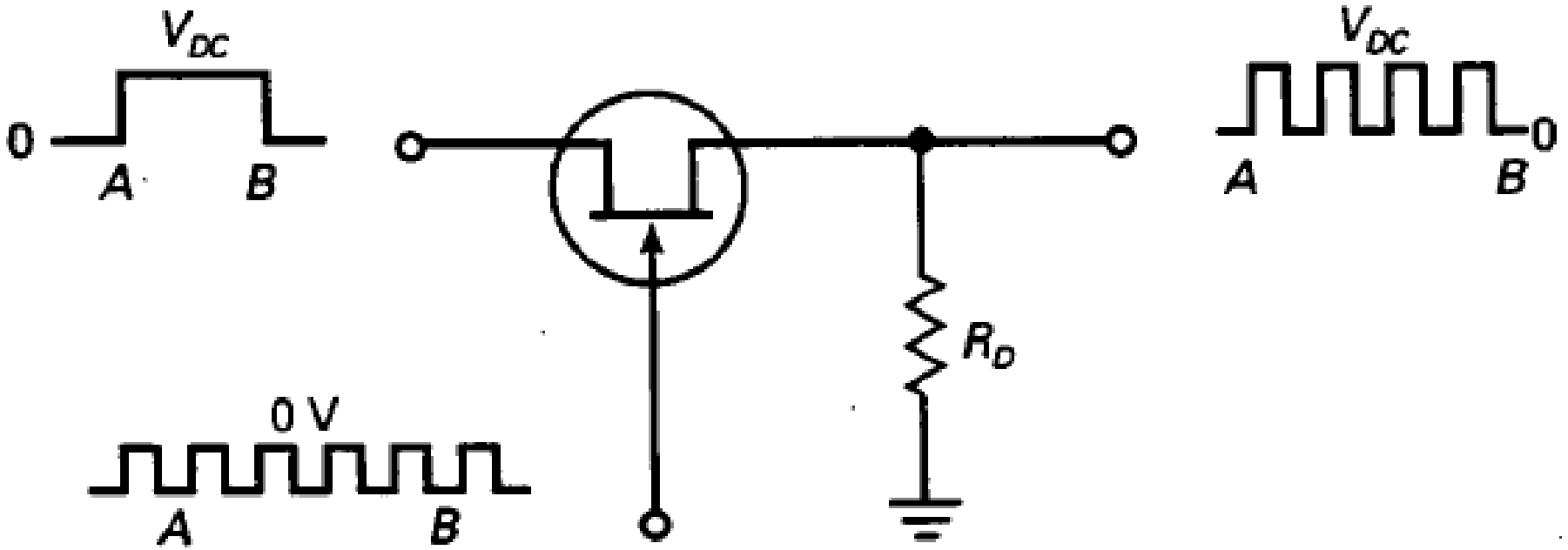


Here, an *n*-channel JFET is used to switch a relay. When the switch is set to position *A*, the JFET is on (gate isn't properly biased for a depletion effect to occur). Current then passes through the JFET's drain-source region and through the relay's coil, causing the relay to switch states. When the switch is thrown to position *B*, a negative voltage—relative to the source—is set at the gate. This in turn causes the JFET to block current flow from reaching the relay's coil, thus forcing the relay to switch states.

Mạch dồn kênh

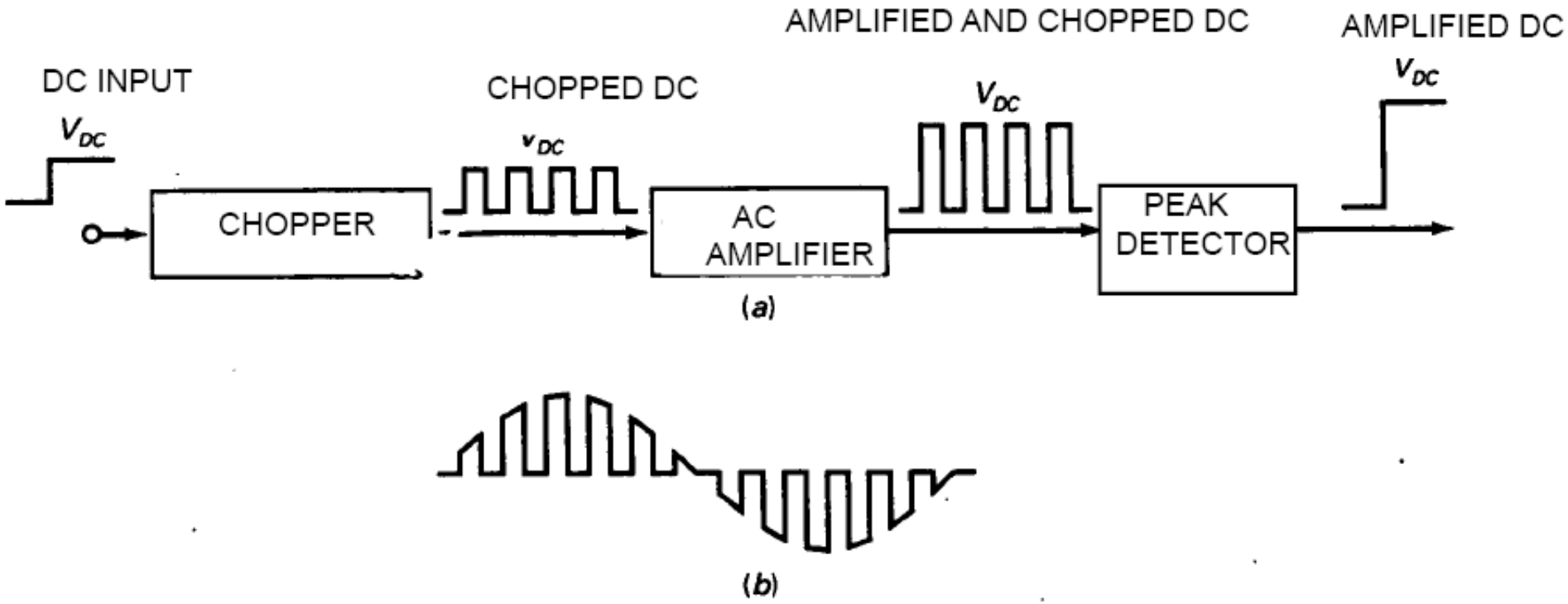


Chopper



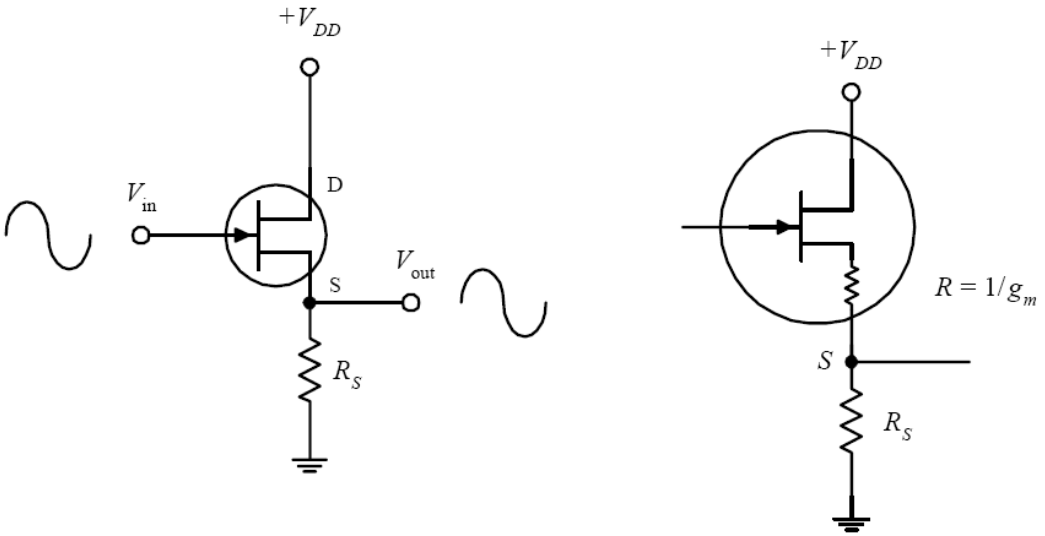
- Chopper có thể dùng công tắc song song hoặc nối tiếp
- Mạch chopper có thể xây dựng mạch KĐ DC

Mạch KĐ chopper



Mạch KĐ

SOURCE FOLLOWER

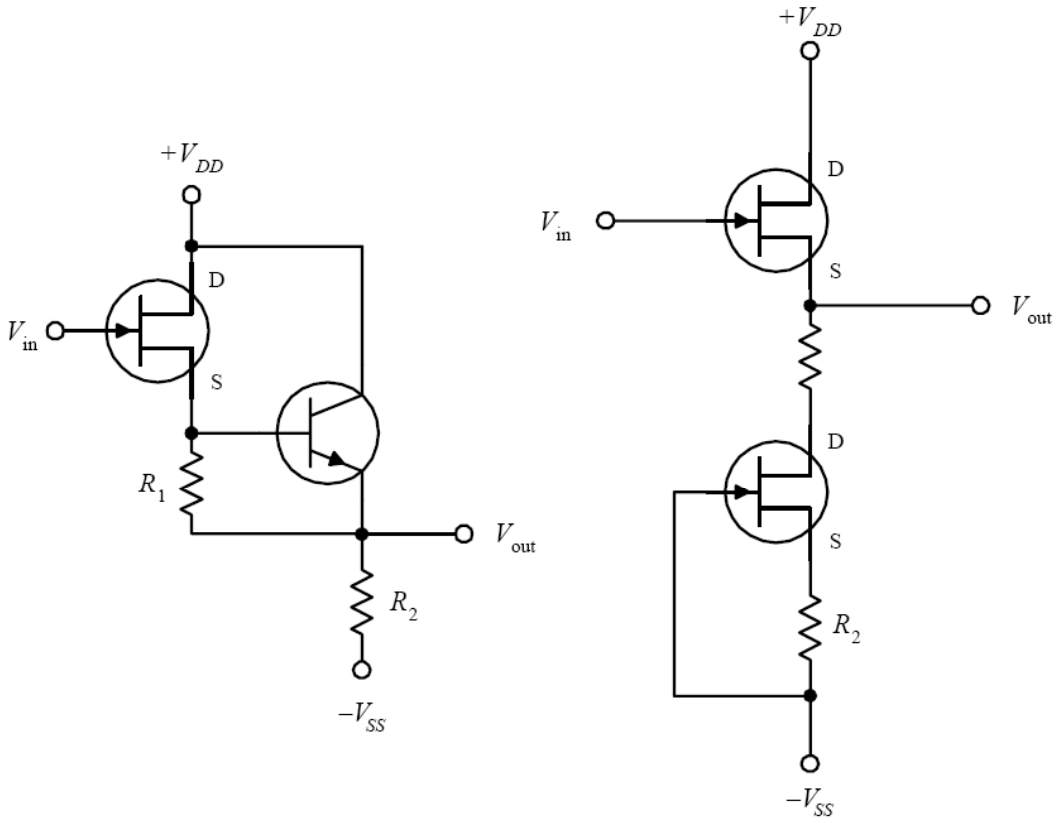


The JFET circuit here is called a *source follower,* which is analogous to the bipolar emitter follower; it provides current gain but not voltage gain. The amplitude of the output signal is found by applying Ohm's law: $V_S = R_S I_D$, where $I_D = g_m V_{GS} = g_m(V_G - V_S)$. Using these equations, you get

$$V_S = \frac{R_S g_m}{1 + R_S g_m} V_G$$

Since $V_S = V_{\text{out}}$ and $V_G = V_{\text{in}}$, the gain is simply $R_S g_m/(1 + R_G g_m)$. The output impedance, as you saw in Problem 2, is $1/g_m$. Unlike the emitter follower, the source follower has an extremely larger input impedance and therefore draws practically no input current. However, at the same time, the JFET's transconductance happens to be smaller than that of a bipolar transistor, meaning the output will be more attenuated. This makes sense if you treat the $1/g_m$ term as being a small internal resistance within the drain-source channel (see rightmost circuit). Also, as the drain current changes due to an applied waveform, g_m and therefore the output impedance will vary, resulting in output distortion. Another problem with this follower circuit is that V_{GS} is a poorly controlled parameter (a result of manufacturing), which gives it an unpredictable dc offset.

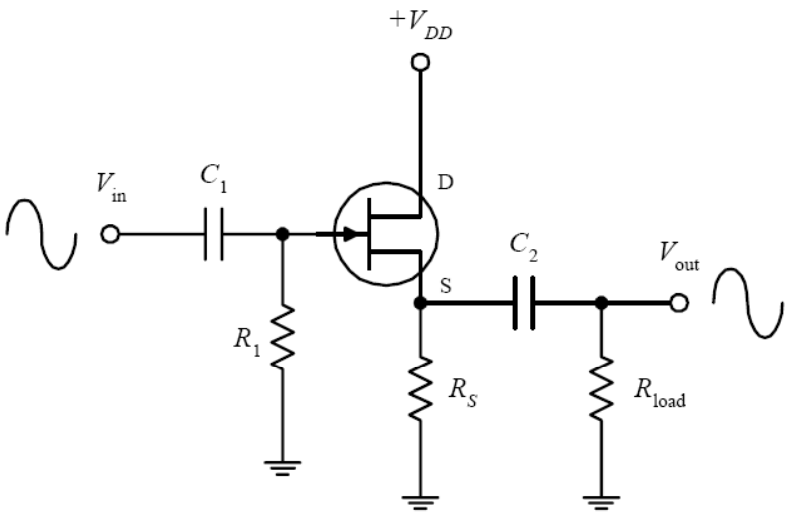
IMPROVED SOURCE FOLLOWER



The source follower circuit from the preceding example had poor linearity and an unpredictable dc offset. However, you can eliminate these problems by using one of the two arrangements shown here. In the far-left circuit, you replace the source resistor with a bipolar current source. The bipolar source acts to fix V_{GS} to a constant value, which in turn eliminates the nonlinearities. To set the dc offset, you adjust R_1. (R_2 acts like R_S in the preceding circuit; it sets the gain.) The near-left circuit uses a JFET current source instead of a bipolar source. Unlike the bipolar circuit, this circuit requires no adjusting and has better temperature stability. The two JFETs used here are matched (matched JFETs can be found in pairs, assembled together within a single package). The lower transistor sinks as much current as needed to make $V_{GS} = 0$ (shorted gate). This means that both JFETs' V_{GS} values are zero, making the upper transistor a follower with zero dc offset. Also, since the lower JFET responds directly to the upper JFET, any temperature variations will be compensated. When R_1 and R_2 are set equal, $V_{out} = V_{in}$. The resistors help give the circuit better I_D linearity, allow you to set the drain current to some value other than I_{DSS}, and help to improve the linearity. In terms of applications, JFET followers are often used as input stages to amplifiers, test instruments, or other equipment that is connected to sources with high source impedance.

JFET AMPLIFIERS

SOURCE-FOLLOWER AMP



Recall the emitter-follower and common-emitter bipolar transistor amplifiers from the last chapter. These two amplifiers have JFET counterparts, namely, the source-follower and the common-source amplifier shown here. (The source-follower amplifier provides current gain; the common-source amplifier provides voltage gain.) If you were to set up the equations and do the math, you would find that the gain for the amplifiers would be

$$\text{Gain} = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{R_S}{R_S + 1/g_m} \qquad \text{(source-follower amp.)}$$

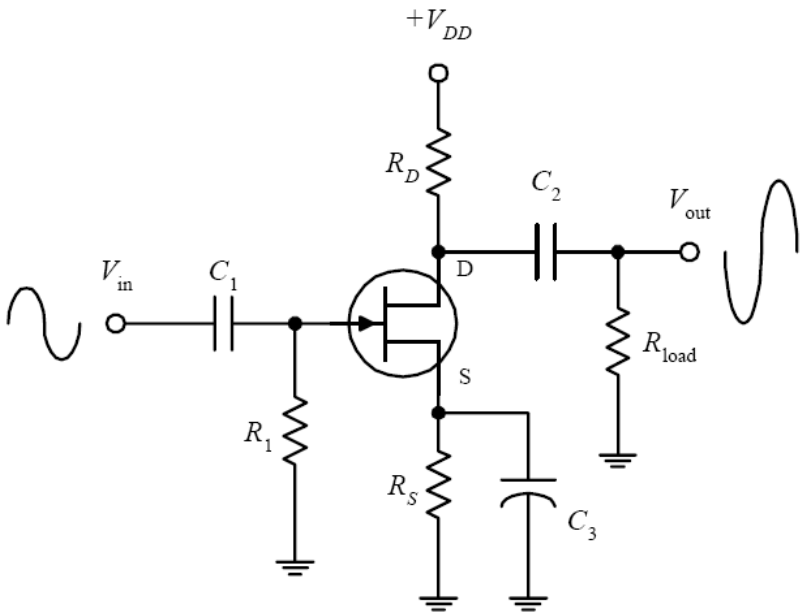
$$\text{Gain} = \frac{V_{\text{out}}}{V_{\text{in}}} = g_m \frac{R_D R_1}{R_D + R_1} \qquad \text{(common-source amp.)}$$

where the transconductance is given by

$$g_m = g_{m_0}\sqrt{\frac{I_D}{I_{DDS}}},\ g_{m_0} = -\frac{2I_{DDS}}{V_{GS,\text{off}}}$$

As with bipolar amplifiers, the resistors are used to set the gate voltages and set the quiescent currents, while the capacitors act as ac couplers/high-pass filters. Notice, however, that both JFET amplifiers only require one self-biasing resistor.

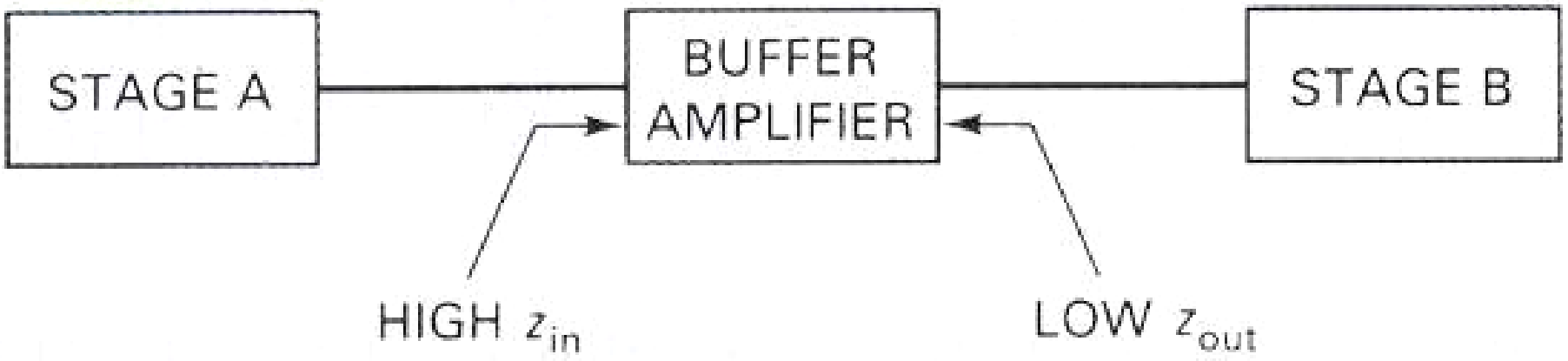
COMMON-SOURCE AMP



Now, an important question to ask at this point is, Why would you choose a JFET amplifier over a bipolar amplifier? The answer is that a JFET provides increased input impedance and low input current. However, if extremely high input impedances are not required, it is better to used a simple bipolar amplifier or op amp. In fact, bipolar amplifiers have fewer nonlinearity problems, and they tend to have higher gains when compared with JFET amplifiers. This stems from the fact that a JFET has a lower transconductance than a bipolar transistor for the same current. The difference between a bipolar's transconductance and JFET's transconductance may be as large as a factor of 100. In turn, this means that a JFET amplifier will have a significantly smaller gain.

Khuếch đại đệm

- Buffer Amp.



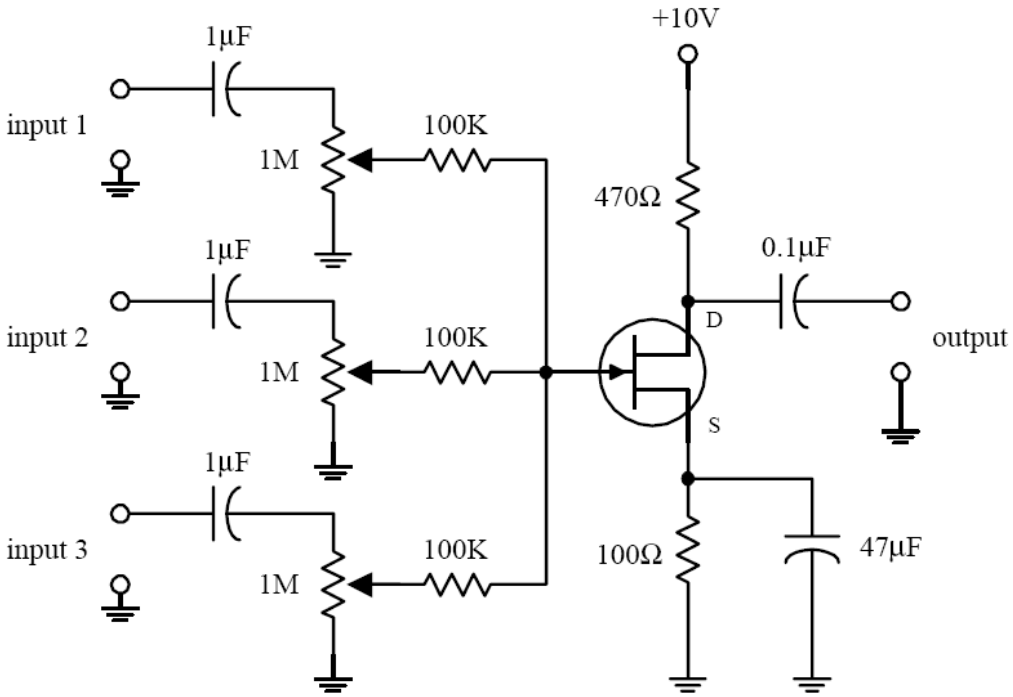
- LNA (Low-Noise-Amplifier)

JFET → Low noise device

→ VHF / VHF amp., mixer, oscillators

Mạch KĐ/trộn âm thanh

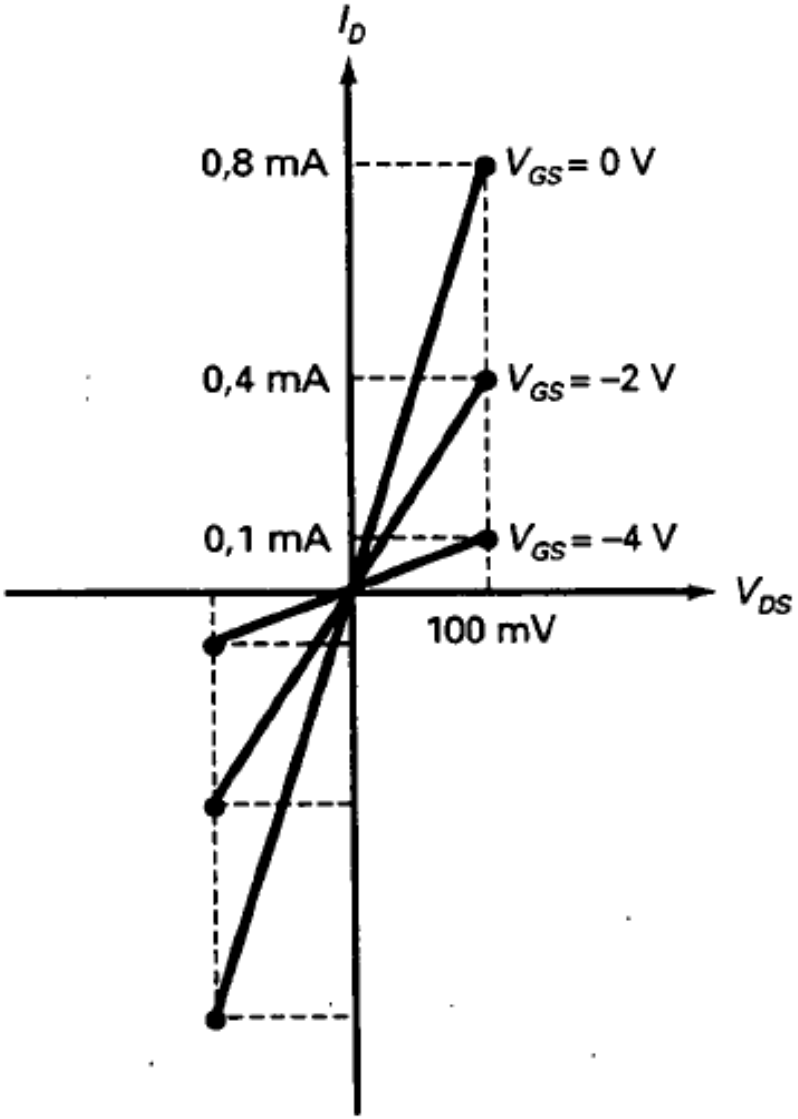
AUDIO MIXER/AMPLIFIER



This circuit uses a JFET—set in the common-source arrangement—to combine (mix) signals from a number of different sources, such as microphones, preamplifiers, etc. All inputs are applied through ac coupling capacitors/filters. The source and drain resistors are used to set the overall amplification, while the 1-MΩ potentiometers are used to control the individual gains of the input signals.

Điện trở được điều khiển bằng áp

Điện trở được điều khiển bằng áp

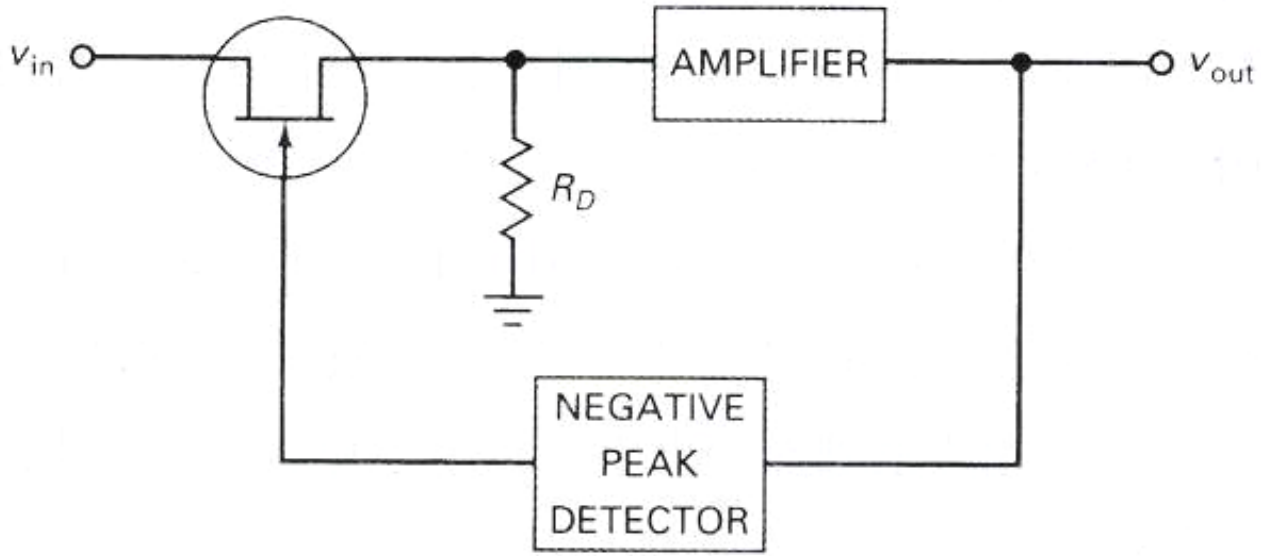


$$r_{ds} = \frac{V_{DS}}{I_D}$$

Điện trở được điều khiển bằng áp

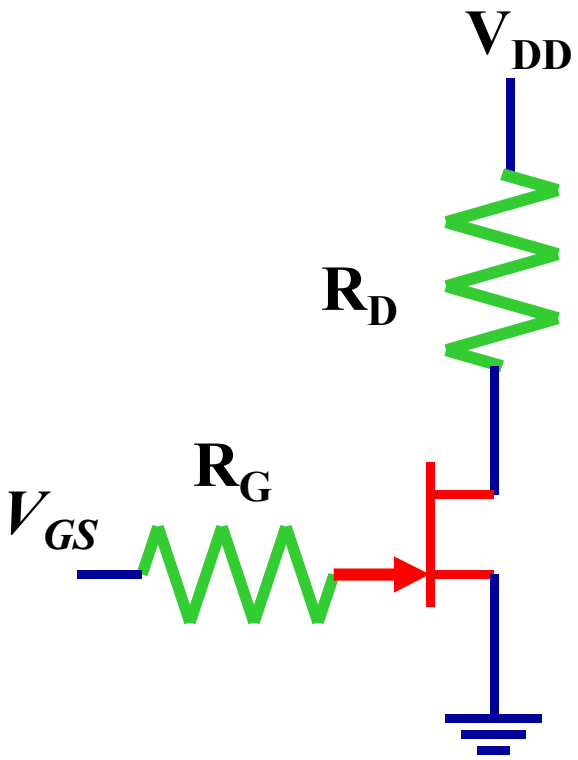
- Hoạt động trong miền Ohm với giá trị V_{GS} giữa 0 và $V_{GS}(off)$.
- Làm việc tốt với tín hiệu AC <=200 mV_{PP}
- Điện trở tín hiệu nhỏ: $r_{ds} = V_{DS}/I_D$
- Khi V_{GS} càng âm, r_{ds} tăng.
- Có thể sử dụng nối tiếp hoặc song song.

- Automatic Gain Control (AGC)

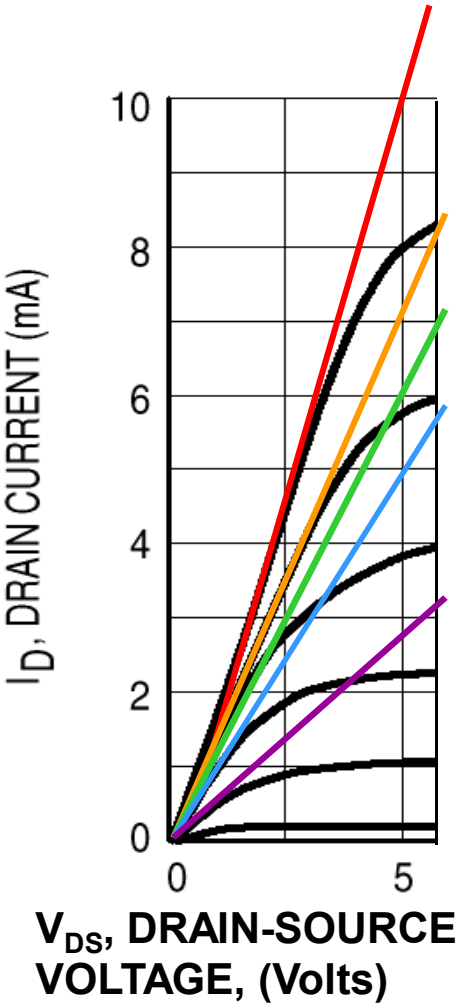


* V_{out} (tăng) → V_{gs} (tăng) → r_{ds} (tăng) → áp vào mạch KĐ nhỏ đi (âm hơn)

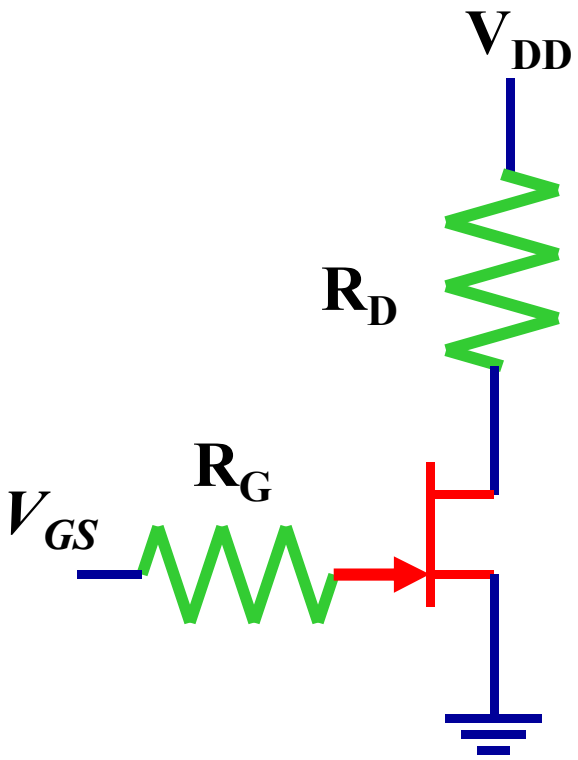
JFET - variable resistor



For the circuit above the family of curves is for changing values of V_{GS} (not labelled in this diagram see slide 3). For low values of V_{DS} the slopes, change from a low effective resistance (~5v/2.7mA~1.9k) to a low resistance (5v/10mA~0.5k). The nice part of this is that the effective resistance is controlled by an input voltage. This makes it possible to have an element in a circuit that can be electronically adjusted.



JFET - variable resistor (2)



Now lets analyze the circuit. In the linear region we had a relationship between I_D and V_{DS}.

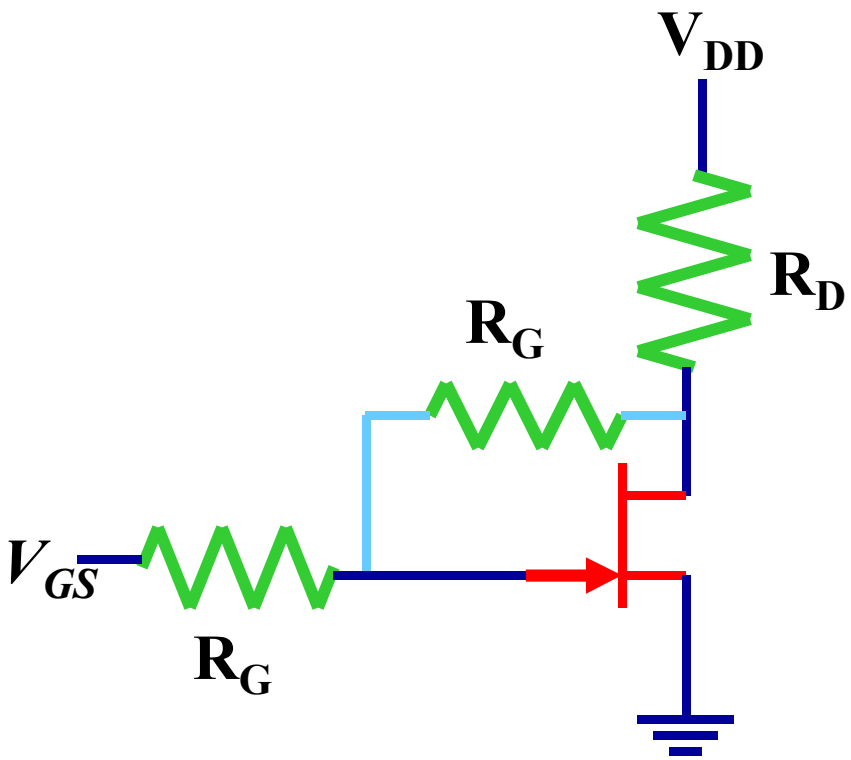
$$I_D = 2k\left[\left(V_{GS} - V_T\right)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

To find the effective resistance this is the voltage across the channel divided by the current through the channel.

$$\frac{1}{R_{DS}} \equiv \frac{I_D}{V_{DS}} = 2k\left[\left(V_{GS} - V_T\right) - \frac{V_{DS}}{2}\right]$$

If it wasn't for the last term, we would have a value of $1/R_{DS}$ that was proportional to V_{GS}, the control voltage and didn't depend on V_{DS} (remember V_T is a constant of the FET, the pinch off voltage). This is like a resistor, and it forms a VOLTAGE DIVIDER with R_D.

JFET - linearized variable resistor

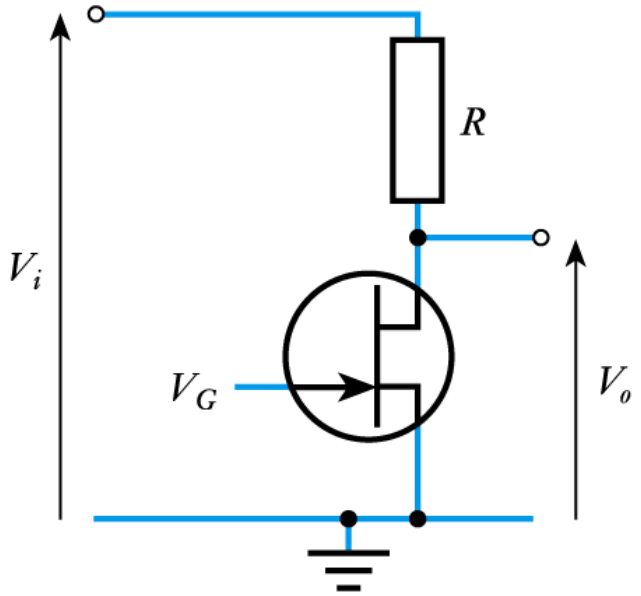


We can make the circuit almost linear by adding a small amount of feedback - that is we 'add' a small amount of current related to V_{DD} that eliminates the last term of the previous expression. We then get a much more linear curve.

In lab we will use a similar circuit, but the feedback will be for AC signals only. How would you do that? (think about adding a cap in the feedback - what would that do?).

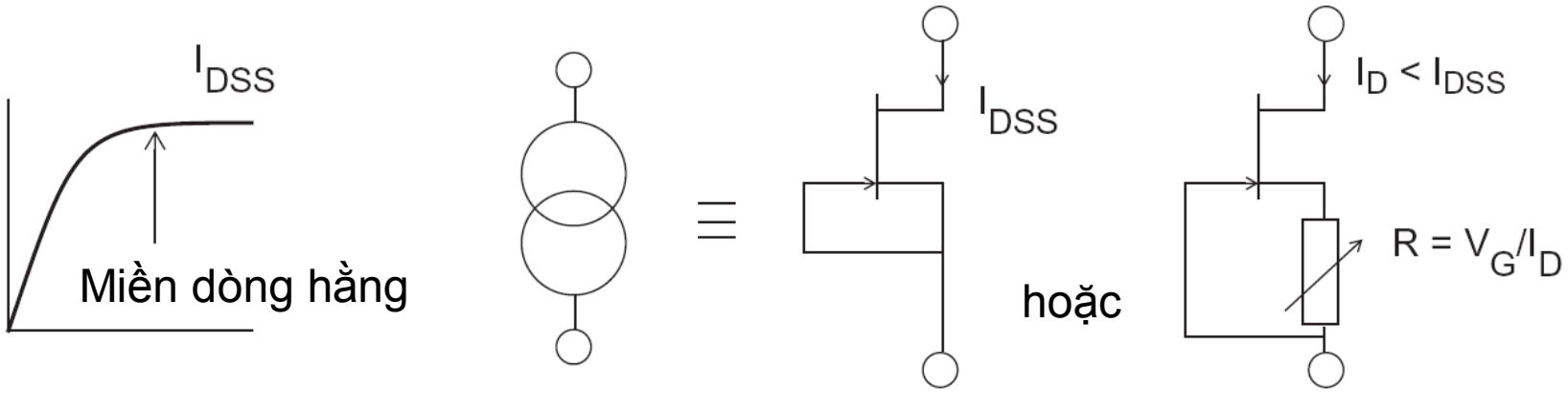
Bộ suy giảm được điều khiển bằng áp

- **A voltage controlled attenuator**
  - for small drain-to-source voltages FETs resemble **voltage-controlled resistors**
  - the gate voltage V_G is used to control this resistance and hence the gain of the potential divider
  - used, for example, in **automatic gain control** in radio receivers

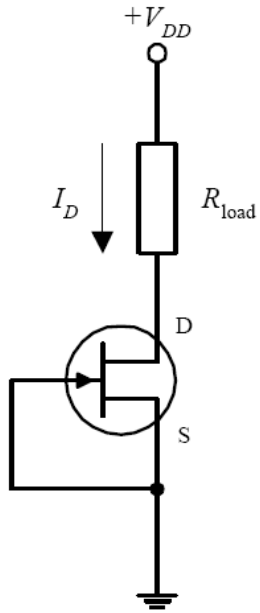


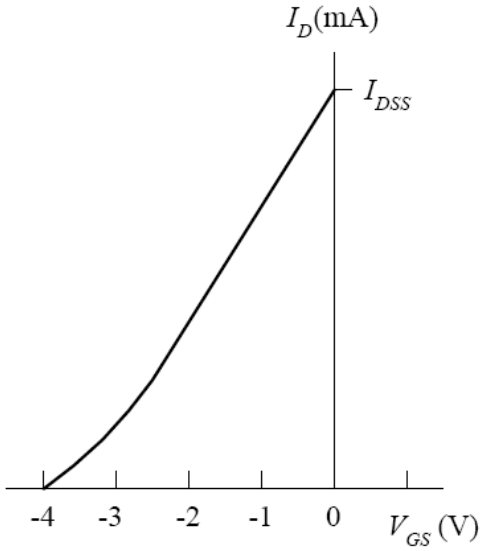
Nguồn dòng

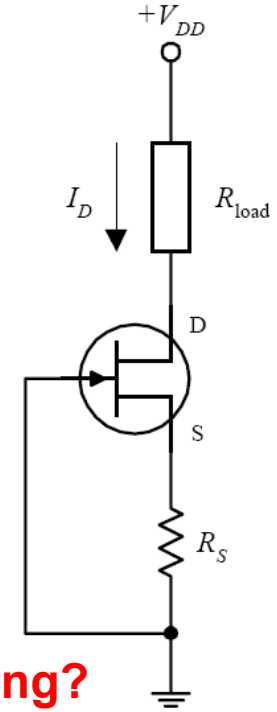
Nguyên tắc cơ bản tạo nguồn dòng bằng JFET



Nguồn dòng cơ bản (JFET hoạt động ở miền bão hòa)

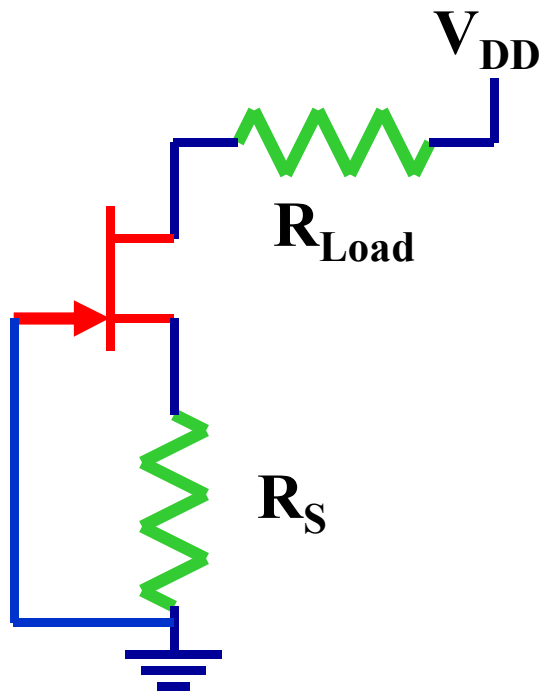


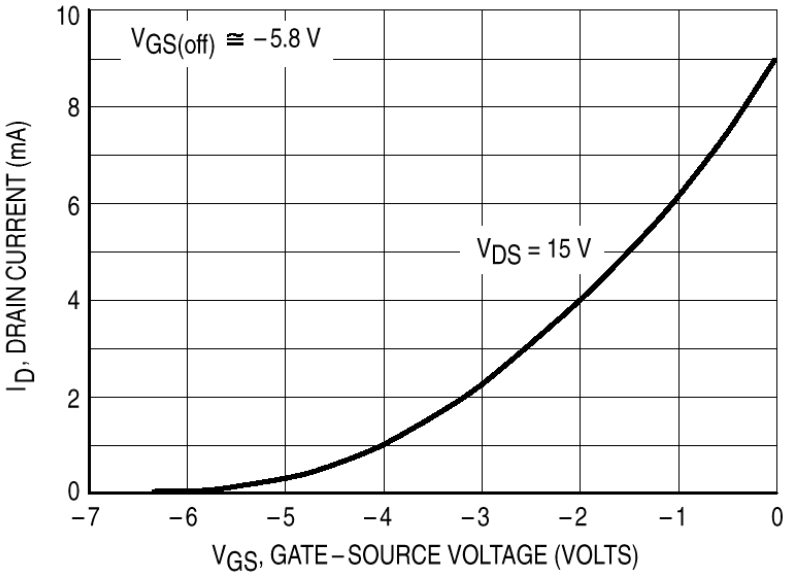




Hãy tìm điều kiện cho JFET và tải để mạch vẫn là nguồn dòng?

Junction FET - current source

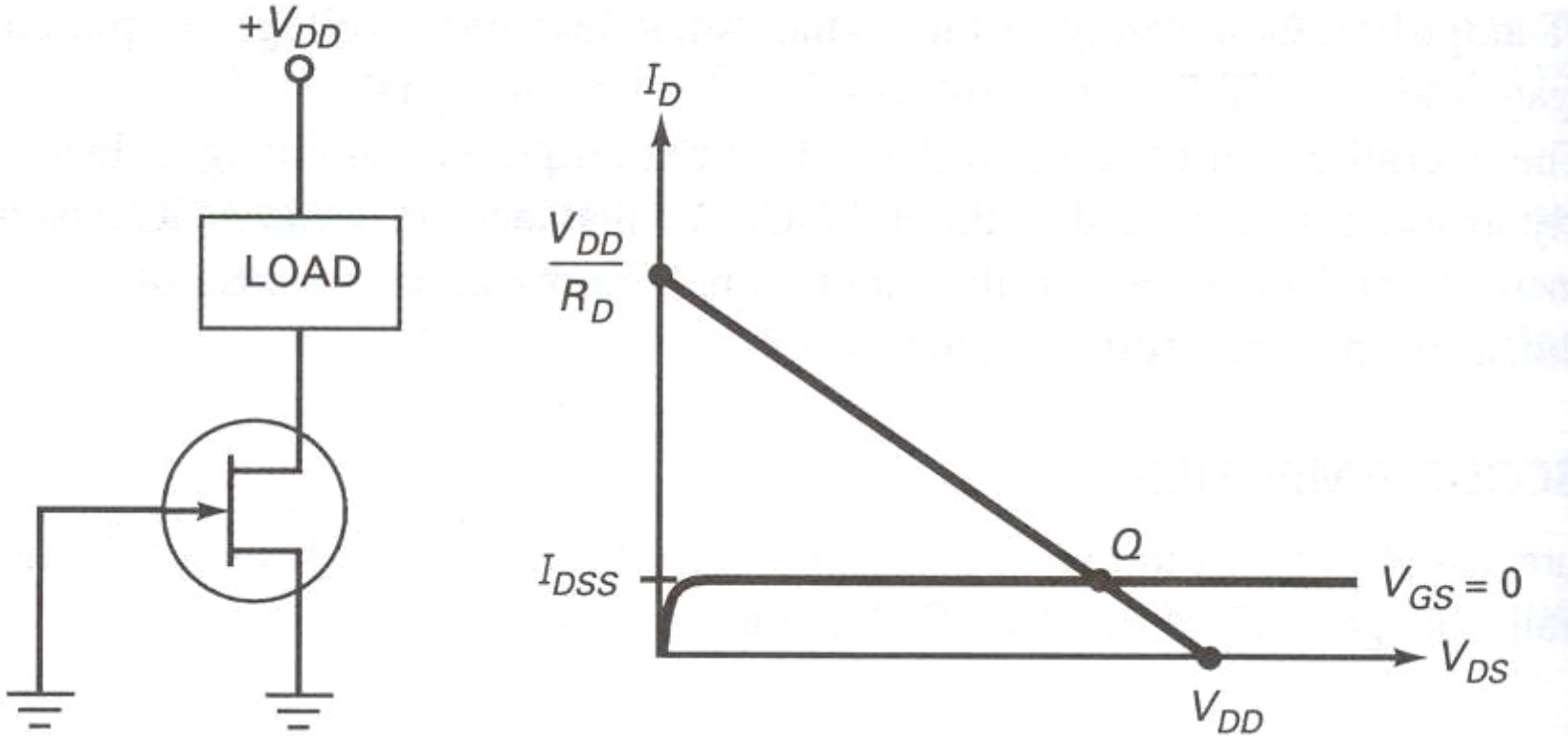




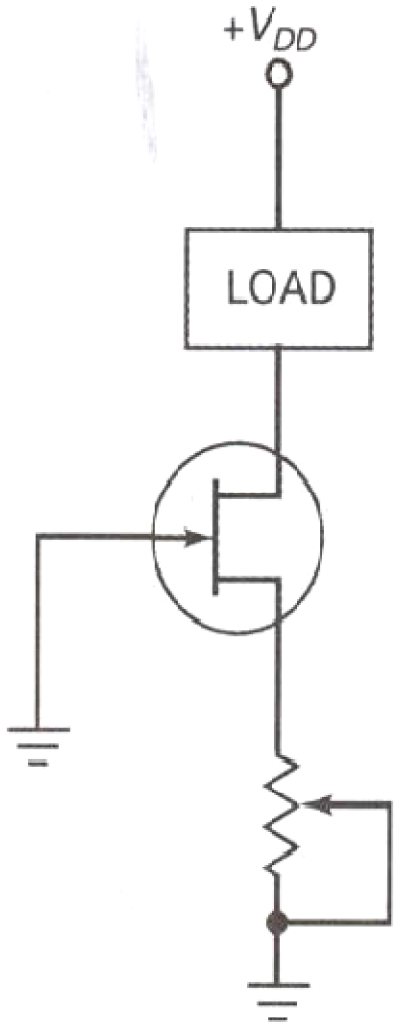
The curve is not effected much by the value of V_{DS} unless it gets too small. This means that we can apply a voltage to the gate and get exactly the same current for very different voltage drops across DS channel. The circuit above is a self-biased voltage controlled current source. If R_S is 4k, then from the plot above 1 mA will flow resulting in V_{GS} = -4 V. Regardless of the value of R_{load} (within the limits of the power supply V_{DD}) exactly 1 mA will be delivered.

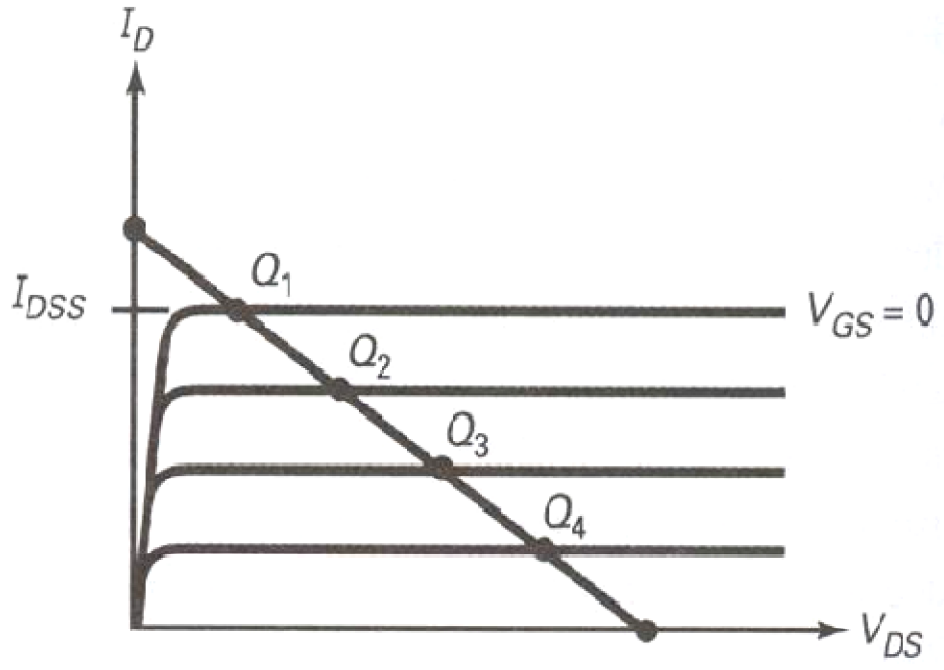
The only downside of this circuit is that the load is not grounded on either end, but that can be fixed.

Nguồn dòng hằng đơn giản

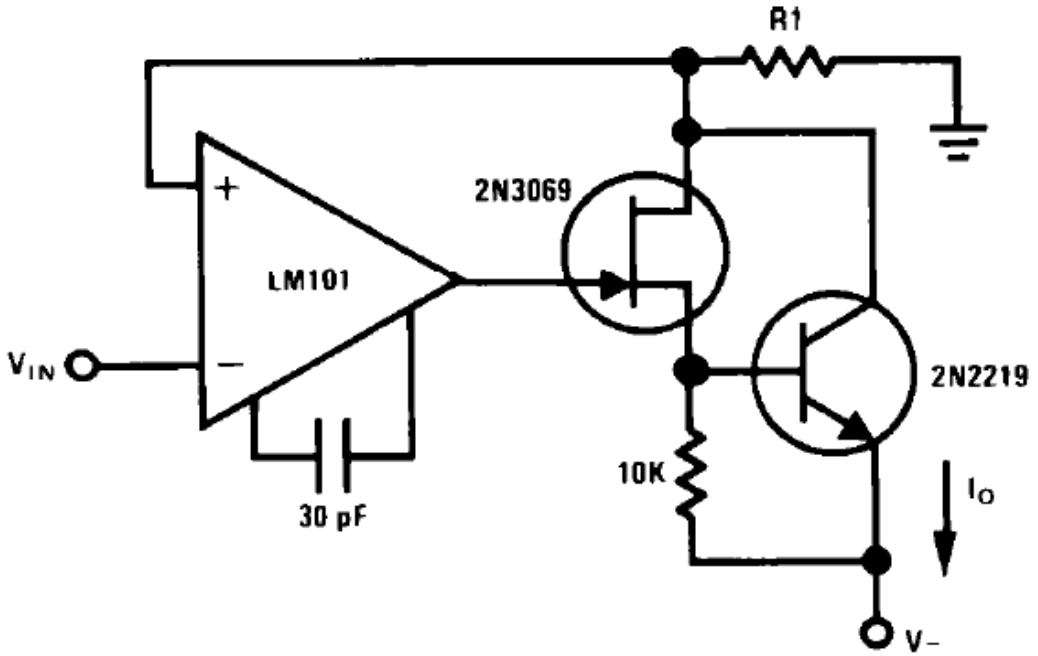


Nguồn dòng hằng đơn giản chỉnh được





Precision Current Source

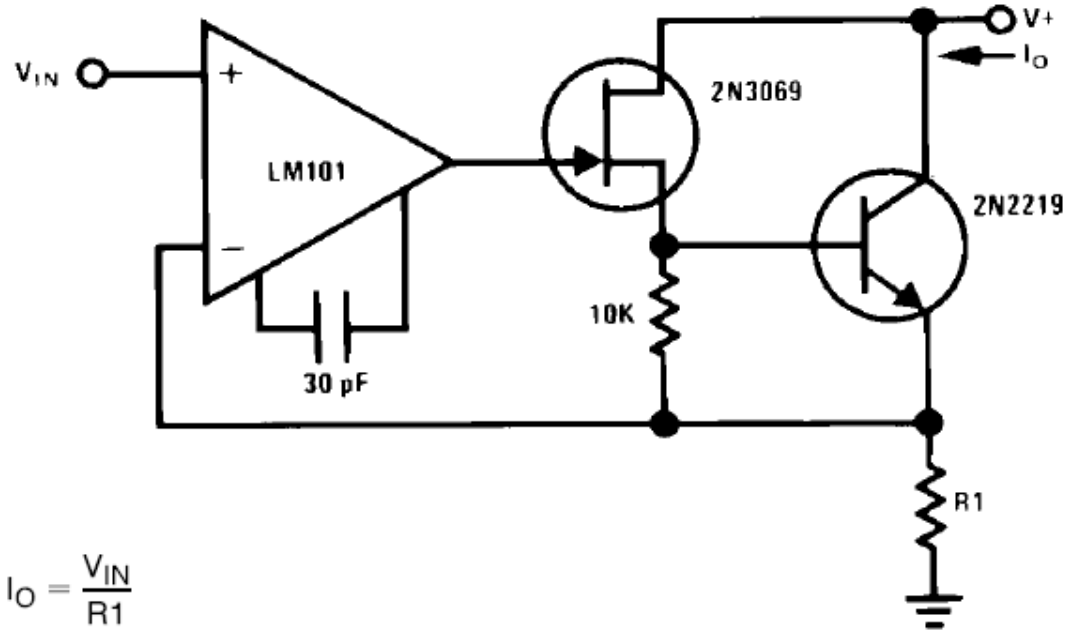


$$I_O = \frac{V_{IN}}{RI} \qquad V_{IN} \leq 0V$$

TL/H/6791–36

Precision Current Source

The 2N3069 JFET and 2N2219 bipolar serve as voltage devices between the output and the current sensing resistor, R_1. The LM101 provides a large amount of loop gain to assure that the circuit acts as a current source. For small values of current, the 2N2219 and 10k resistor may be eliminated with the output appearing at the source of the 2N3069.



$I_O = \frac{V_{IN}}{R1}$

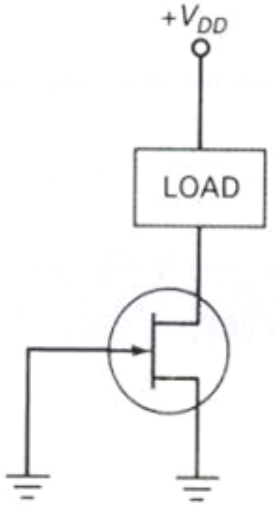
$V_{IN} > 0V$

TL/H/6791–18

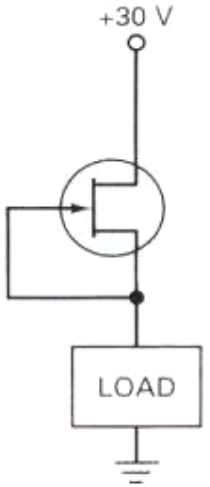
Precision Current Sink

The 2N3069 JFET and 2N2219 bipolar have inherently high output impedance. Using R_1 as a current sensing resistor to provide feedback to the LM101 op amp provides a large amount of loop gain for negative feedback to enhance the true current sink nature of this circuit. For small current values, the 10k resistor and 2N2219 may be eliminated if the source of the JFET is connected to R_1.

Current limiting (giới hạn dòng)



hay

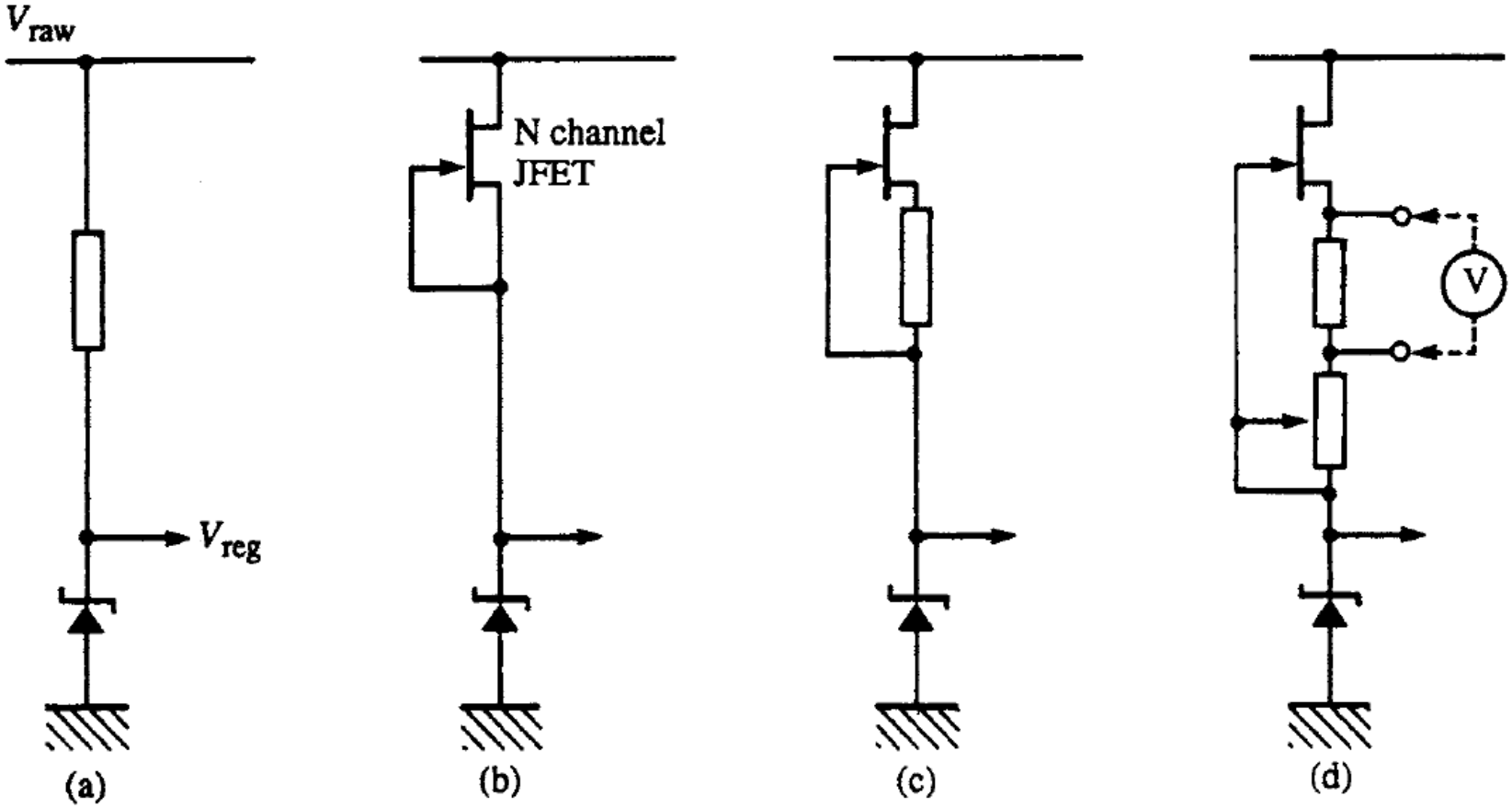


$I_{DSS} = 10mA$ $R_{DS} = 200\Omega$ $V_{DS} = I_{DS} \cdot R_{DS} = 1mA \times 200\Omega = 0.2V$

$(I_{DS} = 1mA)$

* Khi có ngắn mạch ở tải → JFET sẽ giới hạn dòng tối đa là I_{DSS}= 10mA

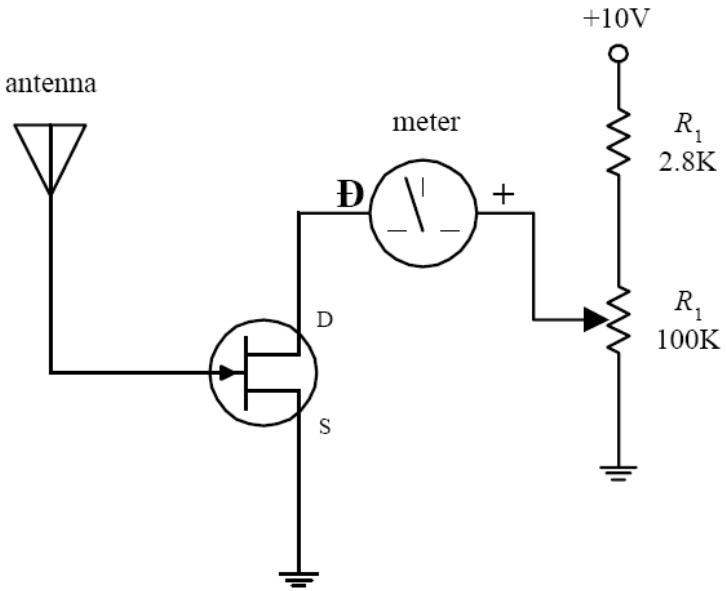
JFET và Zener



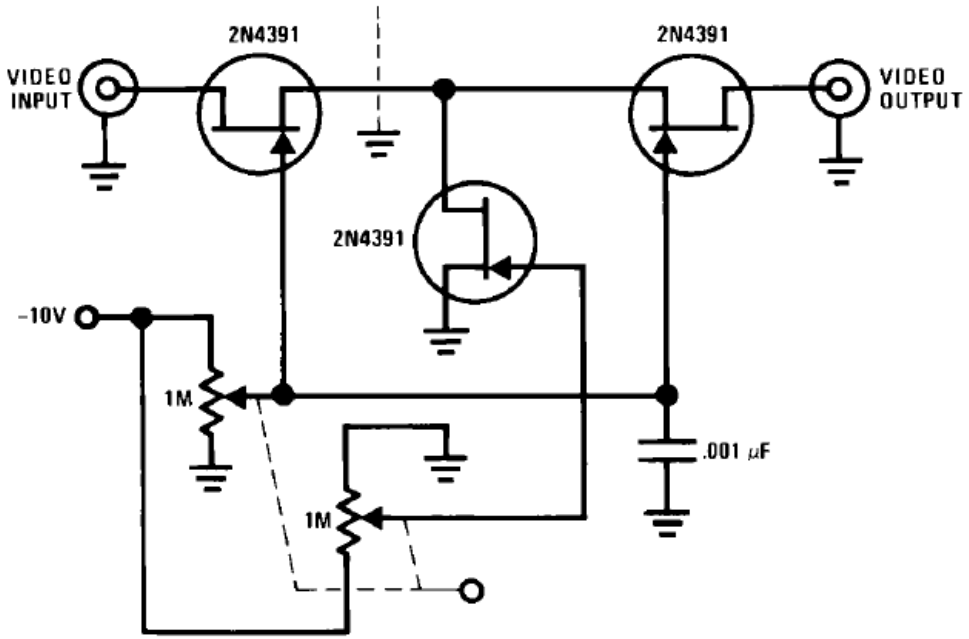
Zener DC voltage references, simple and improved (reproduced by courtesy of *New Electronics*).

Các ứng dụng khác của JFET

ELECTRICAL FIELD METER



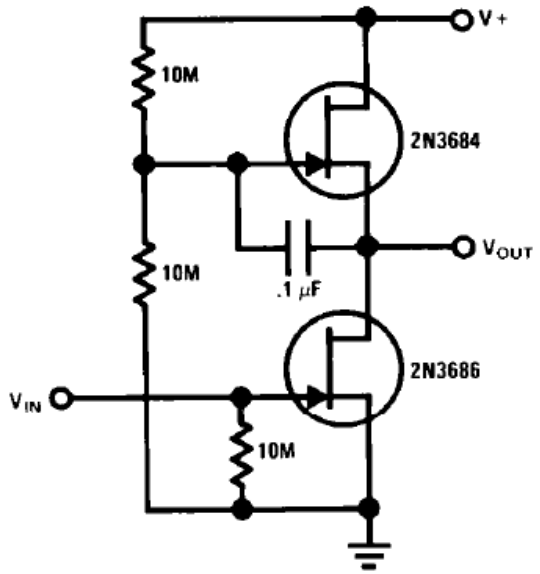
Here, a JFET is used to construct a simple static electricity detector. When the antenna (simple wire) is placed near a charged object, the electrons in the antenna will be draw toward or away from the JFET's gate, depending of weather the object is positively or negatively charged. The repositioning of the electrons sets up a gate voltage that is proportional to the charge placed on the object. In turn, the JFET will either begin to resist or allow current to flow through its drain-source channel, hence resulting in ammeter needle deflection. R_1 is used to protect the ammeter, and R_2 is used to calibrate it.



TL/H/6791–14

Voltage Controlled Variable Gain Amplifier

The 2N4391 provides a low $R_{DS(ON)}$ (less than 30Ω). The tee attenuator provides for optimum dynamic linear range for attenuation and if complete turnoff is desired, attenuation of greater than 100 dB can be obtained at 10 MHz providing proper RF construction techniques are employed.



$$A_V = \frac{\mu}{2} = 500 \text{ TYPICAL}$$

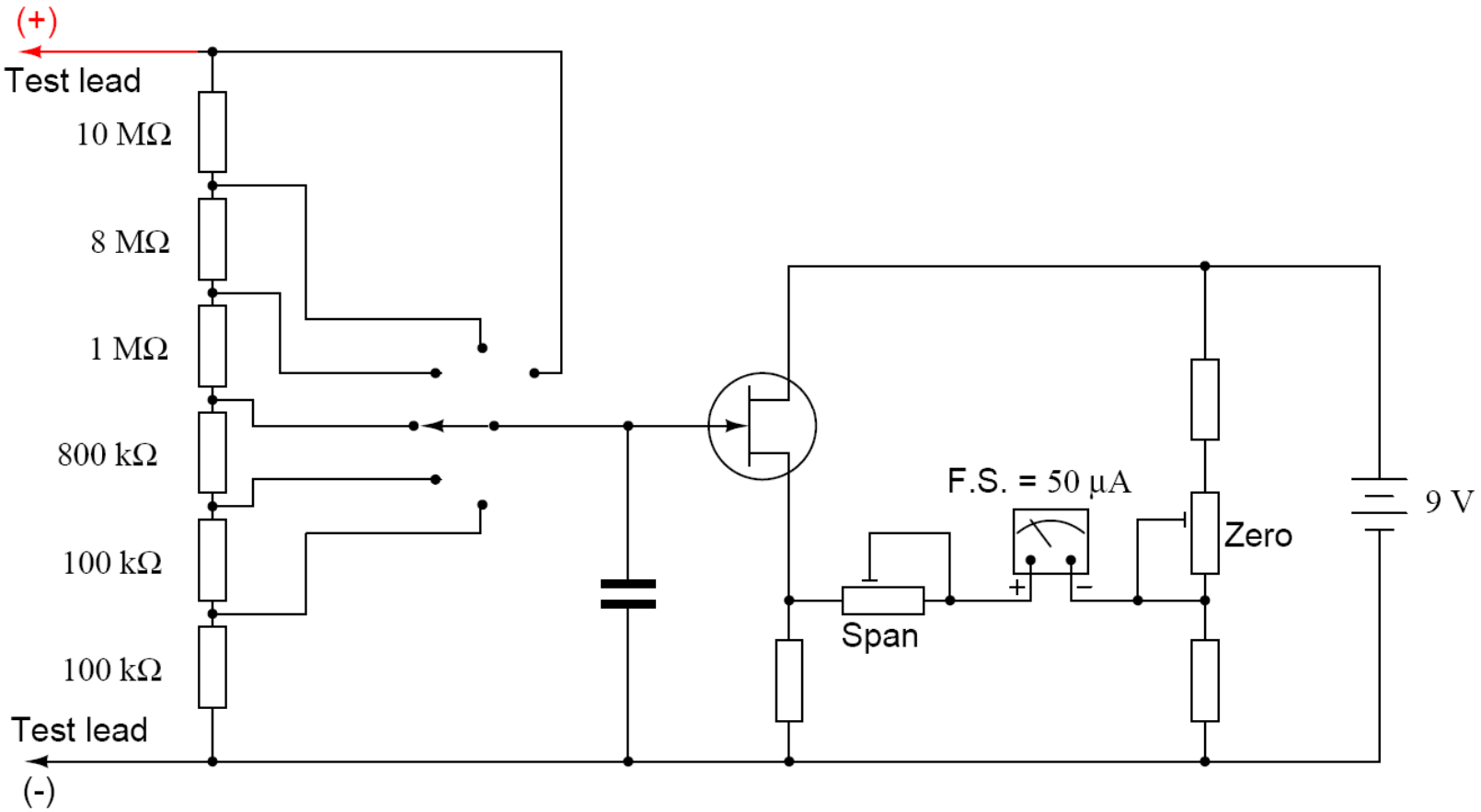
$$\mu = \frac{Y_{fs}}{Y_{os}}$$

TL/H/6791–15

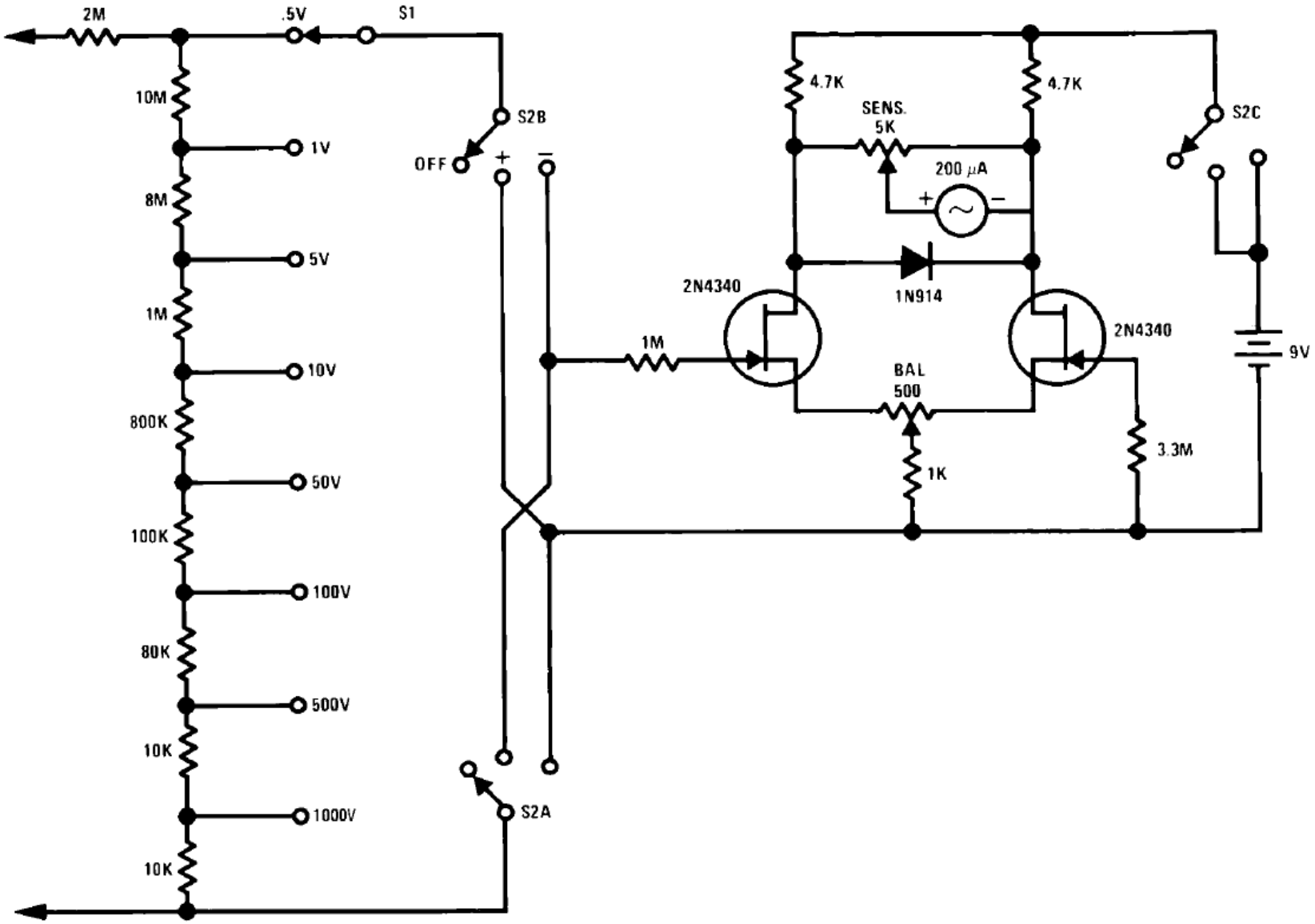
Ultra-High Gain Audio Amplifier

Sometimes called the "JFET" μ amp," this circuit provides a very low power, high gain amplifying function. Since μ of a JFET increases as drain current decreases, the lower drain current is, the more gain you get. You do sacrifice input dynamic range with increasing gain, however.

A precision DC voltmeter



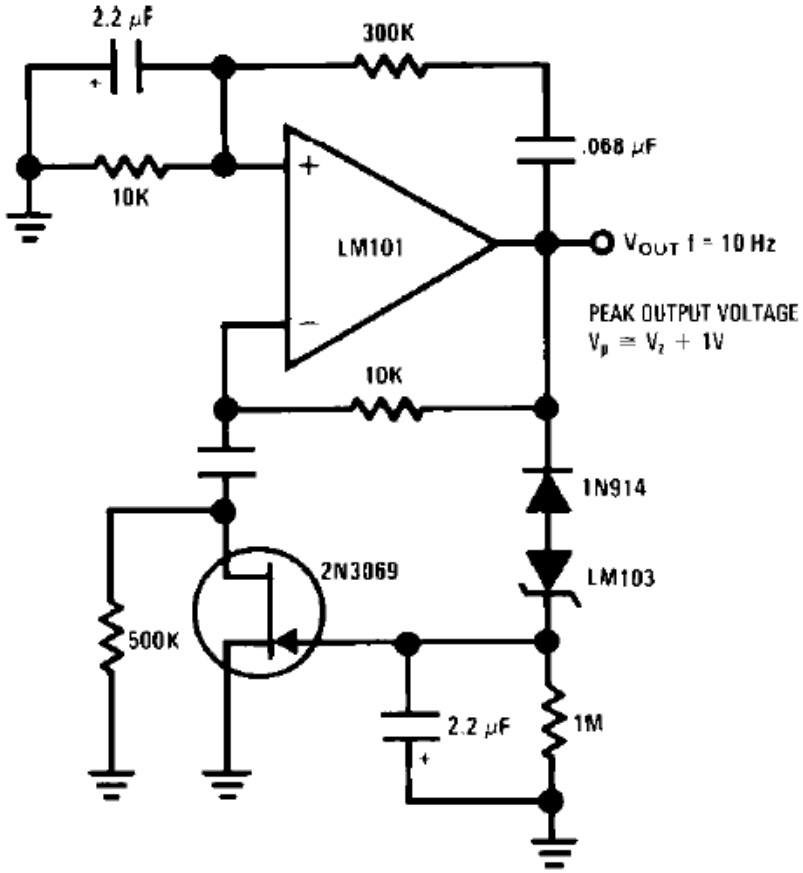
- The voltage ranges for this meter are as follows: 0.1 volts, 0.2 volts, 1.0 volts, 2.0 volts, 10 volts. 20 volts.
- The JFET is being used in the common drain configuration. A reasonable value for the capacitor would be 0.01 µF



TL/H/6791–7

FETVM-FET Voltmeter

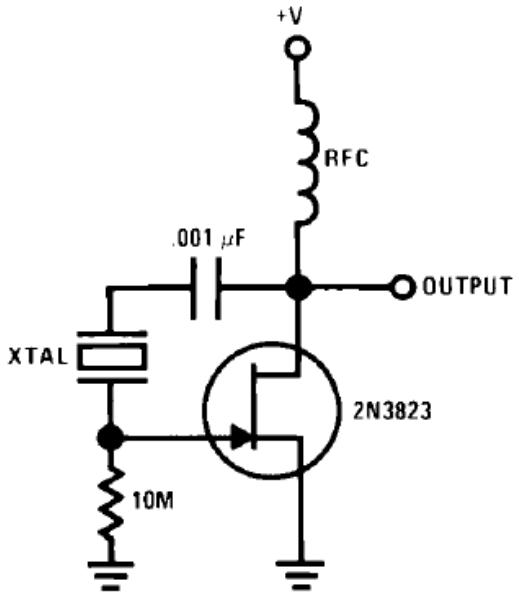
This FETVM replaces the function ot the VTVM while at the same time ridding the instrument of the usual line cord. In addition, drift rates are far superior to vacuum tube circuits allowing a 0.5 volt full scale range which is impractical with most vacuum tubes. The low-leakage, low-noise 2N4340 is an ideal device for this application.



TL/H/6791–21

Wein Bridge Sine Wave Oscillator

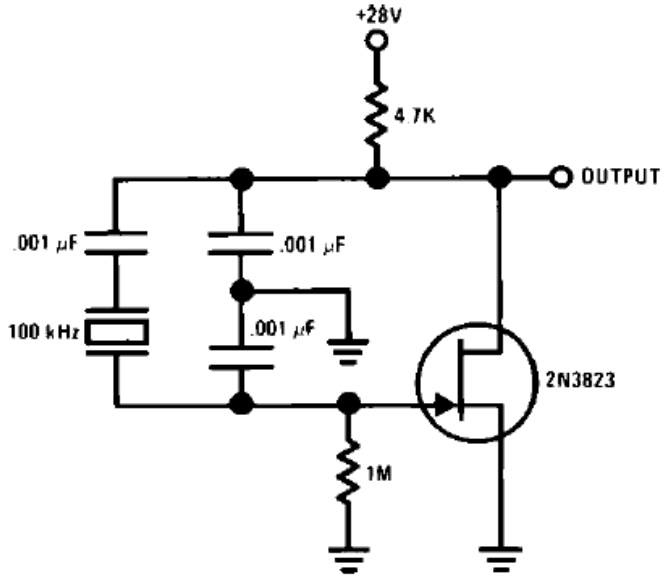
The major problem in producing a low distortion, constant amplitude sine wave is getting the amplifier loop gain just right. By using the 2N3069 JFET as a voltage variable resistor in the amplifier feedback loop, this can be easily achieved. The LM103 zener diode provides the voltage reference for the peak sine wave amplitude; this is rectified and fed to the gate of the 2N3069, thus varying its channel resistance and, hence, loop gain.



TL/H/6791–6

JFET Pierce Crystal Oscillator

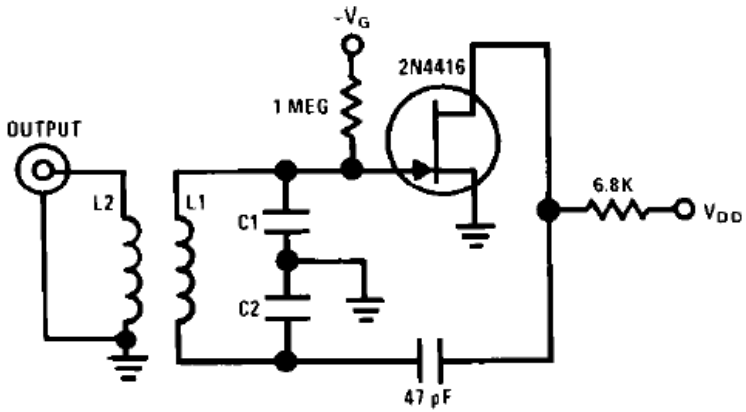
The JFET Pierce crystal oscillator allows a wide frequency range of crystals to be used without circuit modification. Since the JFET gate does not load the crystal, good Q is maintained thus insuring good frequency stability.



TL/H/6791–25

Stable Low Frequency Crystal Oscillator

This Colpitts-Crystal oscillator is ideal for low frequency crystal oscillator circuits. Excellent stability is assured because the 2N3823 JFET circuit loading does not vary with temperature.



20 MHz OSCILLATOR VALUES

C1 ≅ 700 pF L1 = 1.3 μH

C2 = 75 pF L2 = 10T 3/8″ DIA 3/4″ LONG

V_{DD} = 16V I_D = 1 mA

20 MHz OSCILLATOR PERFORMANCE

LOW DISTORTION 20 MHz OSC.

2ND HARMONIC −60 dB

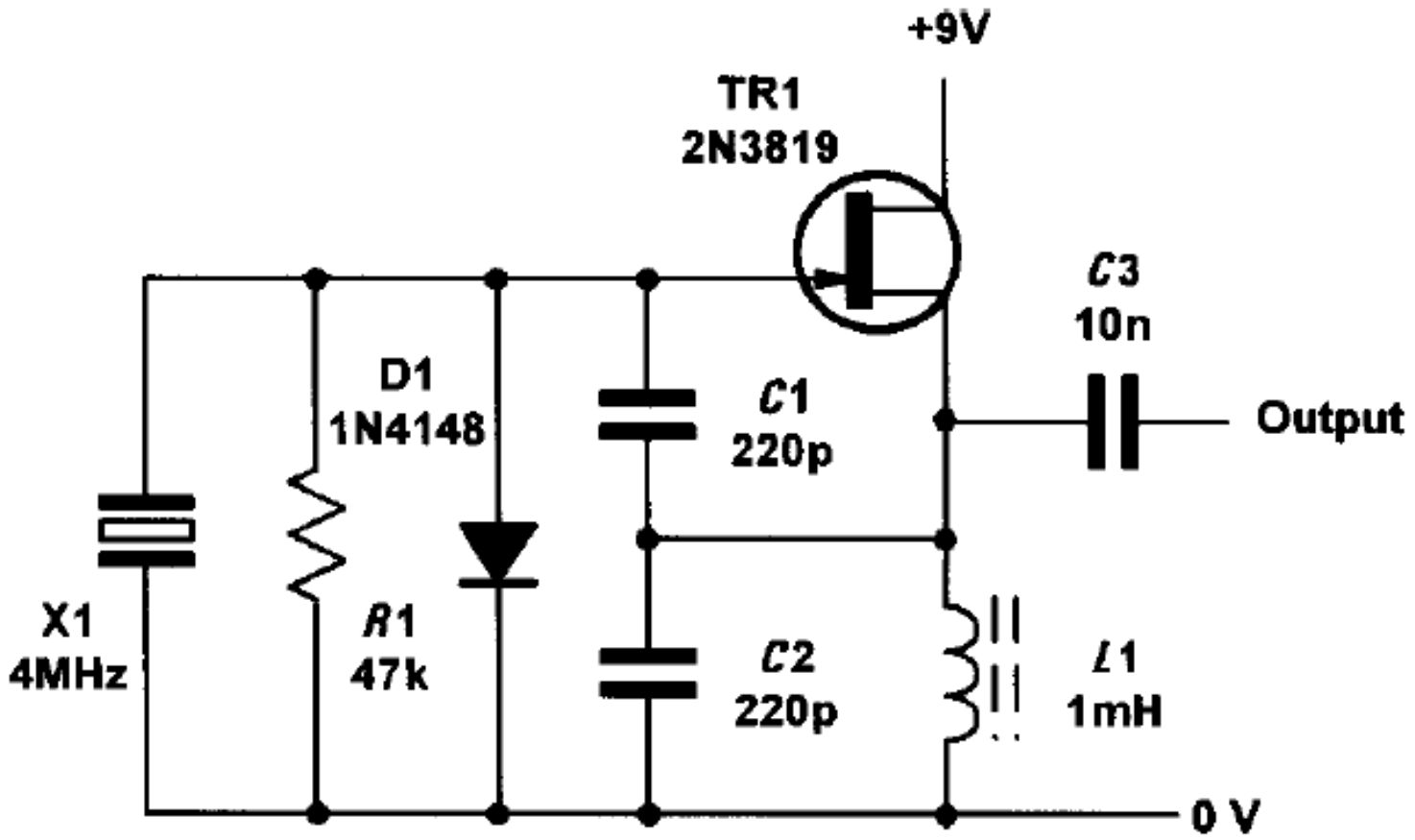
3RD HARMONIC > −70 dB

TL/H/6791–28

Low Distortion Oscillator

The 2N4416 JFET is capable of oscillating in a circuit where harmonic distortion is very low. The JFET local oscillator is excellent when a low harmonic content is required for a good mixer circuit.

A practical high-frequency crystal oscillator



Điều chỉnh ánh sáng

LIGHT DIMMER

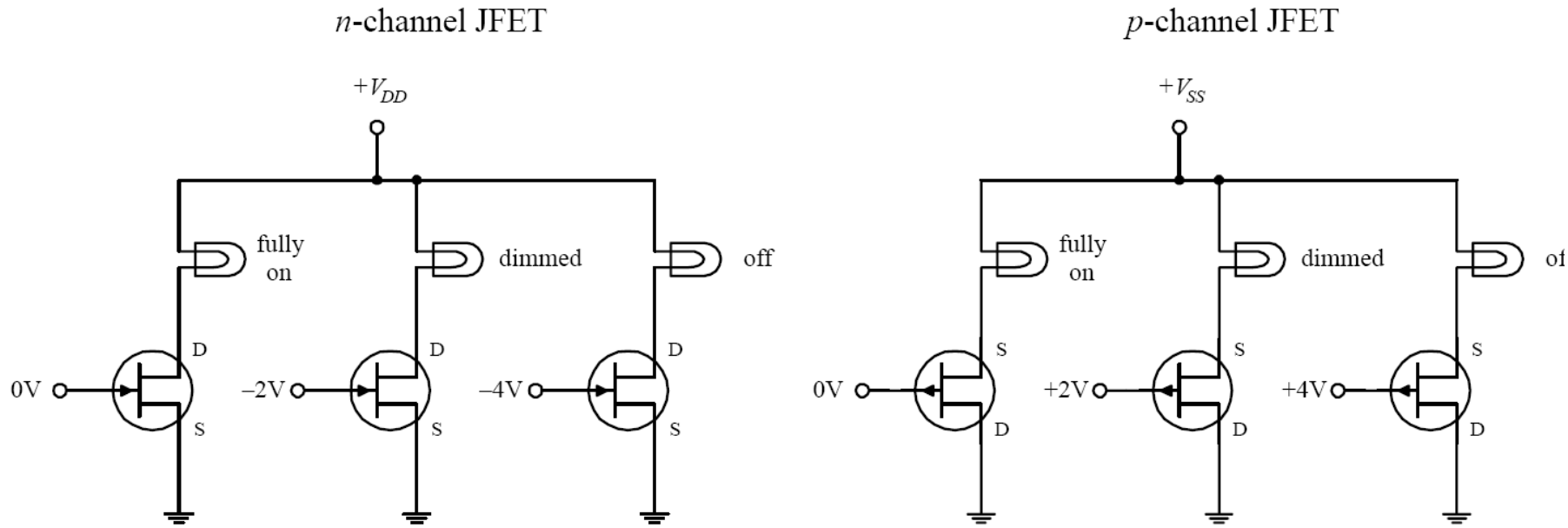


FIGURE 4.53

The two circuits here demonstrate how a JFET acts like a voltage-controlled light dimmer. In the *n*-channel circuit, a more negative gate voltage causes a larger source-to-drain resistance, hence causing the light bulb to receive less current. In the *p*-channel circuit, a more positive gate voltage causes a greater drain-to-source resistance.