ĐHBK Tp HCM-Khoa Đ-ĐT
BMĐT
GVPT: Hồ Trung Mỹ
Môn học: Dụng cụ bán dẫn

Chương 7

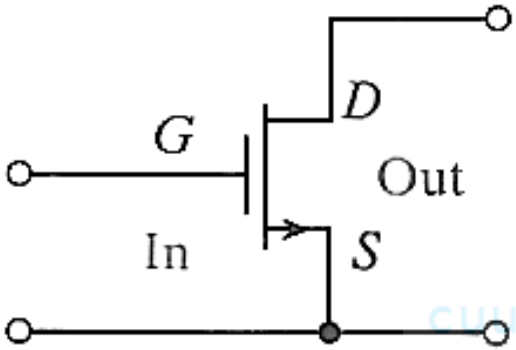
MOSFET

(Metal-Oxide Semiconductor Field Effect Transistor)

MOSFET

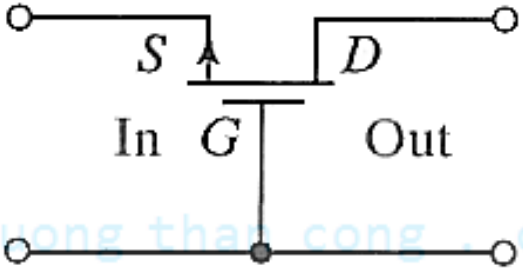
- Giới thiệu
- Khảo sát định tính hoạt động của MOSFET
- Tụ điện MOS
- Hoạt động của MOSFET
- Một số đặc tính không lý tưởng
- Mạch tương đương tín hiệu nhỏ
- Giới thiệu 1 số ứng dụng của MOSFET

Các cấu hình mắc N-EMOS trong mạch



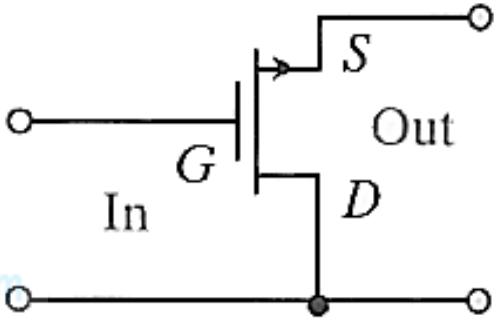
Common source

Nguồn chung (CS)



Common gate

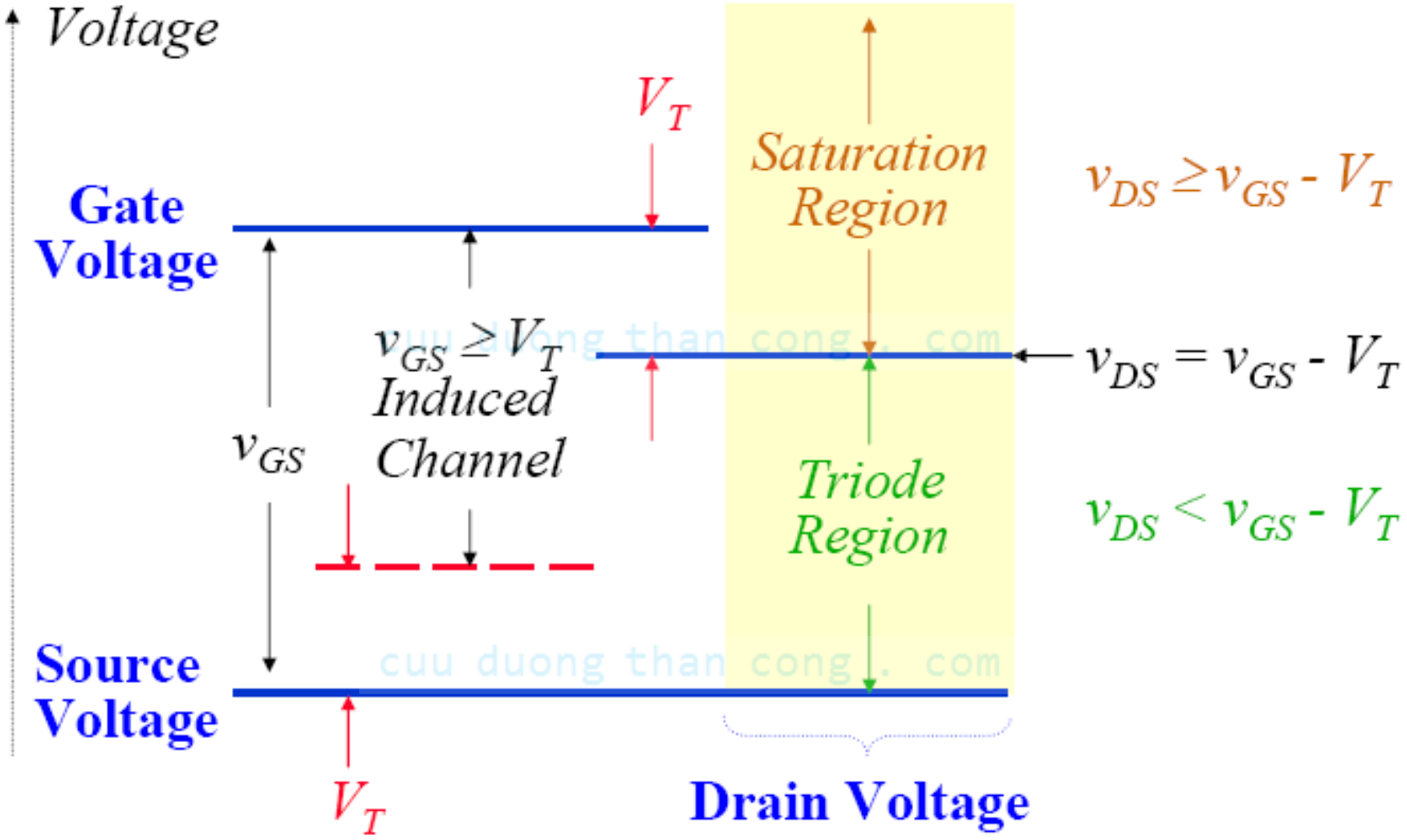
Cổng chung (CG)



Common drain

Máng chung (CG)

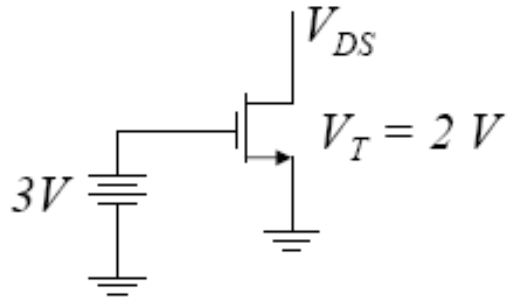
Nhận biết các miền hoạt động của N-EMOS



N-EMOS – Thí dụ 1

Find the modes of operation for

a) $v_{DS} = 0.5V$, *b)* $v_{DS} = 1V$, and *c)* $v_{DS} = 5V$



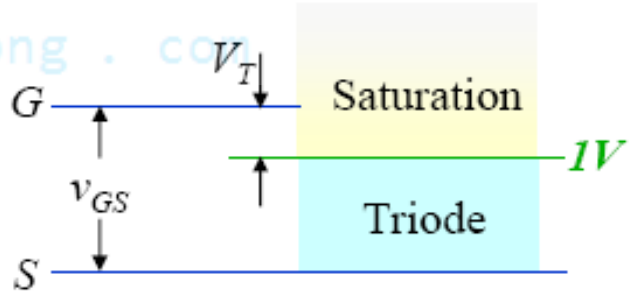
a) Case I ($v_{DS} = 0.5V$)

Since $v_{GS} \geq V_T$ $(3V \geq 2V)$ an *n*-channel is formed!

Boundary condition: $v_{DS} = v_{GS} - V_T$

Triode condition: $v_{DS} \leq v_{GS} - V_T$

Saturation condition: $v_{DS} \geq v_{GS} - V_T$



$\therefore v_{GS} - V_T = 3 - 2 = 1V$ *(Boundary)*

$\Rightarrow v_{DS} = 0.5V \leq 1V$ ***Boundary*** $\Rightarrow$ *Triode Region*

b) Case II ($v_{DS} = 1V$): Since $v_{DS} = 1V = v_{GS} - V_T = 1V \Rightarrow$ *Saturation*

c) Case III ($v_{DS} = 5V$): Since $v_{DS} = 5V > v_{GS} - V_T = 1V \Rightarrow$ *Saturation*

N-EMOS – Thí dụ 2

The key parameters for an NMOS FET are $\mu_n C_{ox} = 20\ \mu A/V^2$, $W = 100\ \mu m$, $L = 10\ \mu m$, and $\lambda = 0$. Using the circuit from the previous example, what is i_D when *a)* $v_{DS} = 0.5V$, *b)* $v_{DS} = 1V$, and *c)* $v_{DS} = 5\ V$?

a) $v_{DS} = 0.5\ V$

$$i_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)\left[2(v_{GS} - V_T)v_{DS} - v_{DS}^2\right]$$

Triode Region

$$= \frac{1}{2}\left(20\frac{\mu A}{V^2}\right)\left(\frac{100\mu m}{10\mu m}\right)\left[2(3-1)0.5 - (0.5)^2\right] = 75\mu A$$

b) $v_{DS} = 1V\ \&\ 5V$

$$i_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(v_{GS} - V_T)^2\left(1 + \cancelto{0}{\lambda}\, v_{DS}\right)$$

Saturation Region

$$= \frac{1}{2}\left(20\frac{\mu A}{V^2}\right)\left(\frac{100\mu m}{10\mu m}\right)(3-1)^2 = 100\mu A$$

N-EMOS – Thí dụ 3

Using an enhancement mode NMOS MOSFET with $V_T = 1.5V$, $v_{GS} = 3.5\ V$, $\mu_n C_{ox}\ (W/2L) = 0.1\ mA/V^2$, and $\lambda = 0.02\ V^{-1}$, find i_D for $v_{DS} = 2\ V$ and $10V$.

For $v_{DS} = 2\ V$: *Mode threshold* $= v_{GS} - V_T = 3.5V - 1.5V = 2V \Rightarrow$ *Saturation*

$$i_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(v_{GS} - V_T)^2(1 - \lambda v_{DS})$$

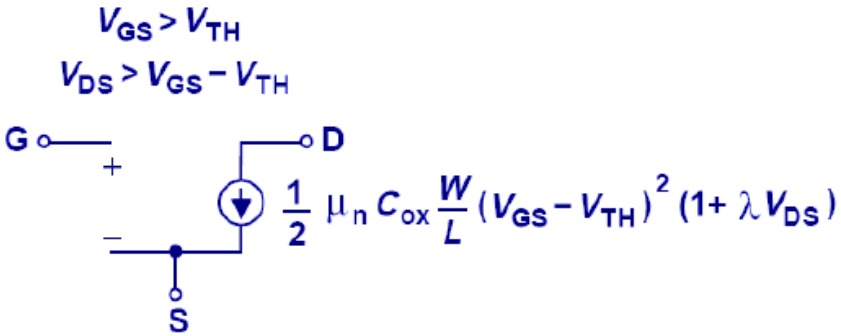
$$= \left(0.1\frac{mA}{V^2}\right)(3.5V - 1.5V)^2[1 + (0.02V^{-1})(2V)] = 416\mu A$$

For $v_{DS} = 10\ V$: *Mode threshold* $= v_{GS} - V_T = 3.5V - 1.5V = 2V \Rightarrow$ *Saturation*

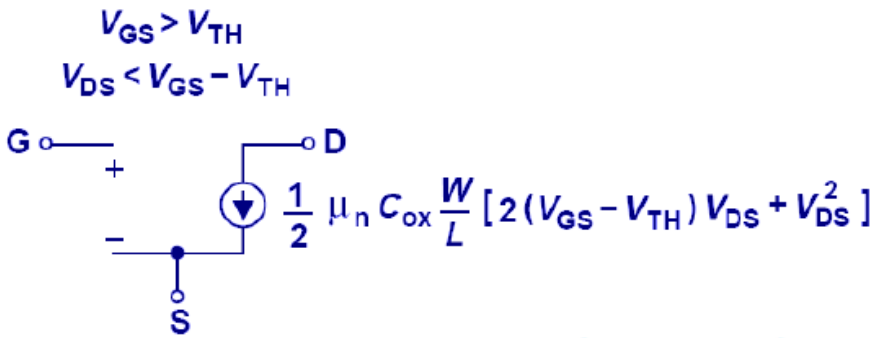
$$i_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(v_{GS} - V_T)^2(1 - \lambda v_{DS})$$

$$= \left(0.1\frac{mA}{V^2}\right)(3.5V - 1.5V)^2[1 + (0.02V^{-1})(10V)] = 480\mu A$$

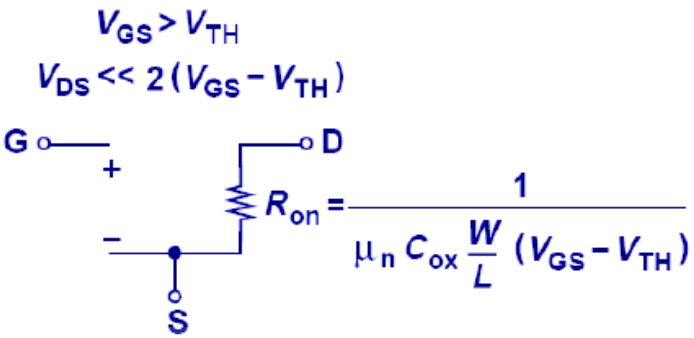
Mô hình tín hiệu lớn của N-EMOS



(a) Miền bão hòa



(b) Miền triode

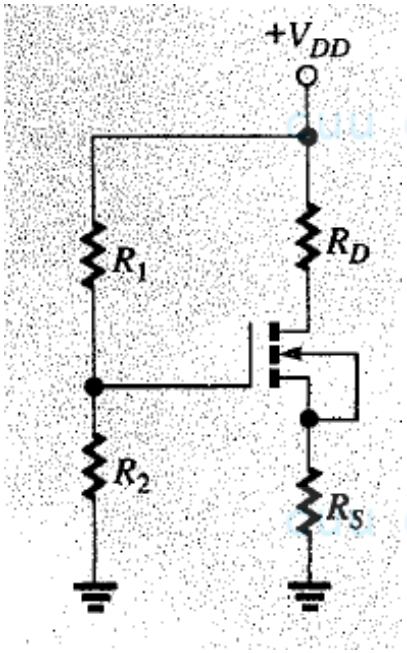


(c) Miền triode hoàn toàn tuyến tính

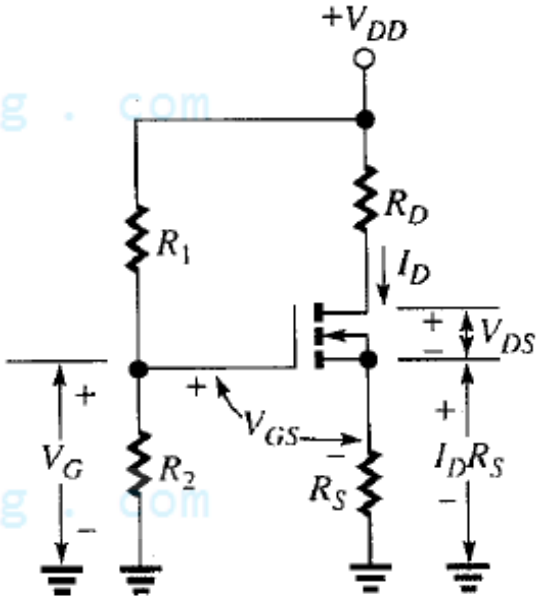
Dựa vào giá trị của V_{DS}, MOSFET có thể được biểu diễn bằng những mô hình tín hiệu lớn khác nhau

Mạch phân cực N-EMOS (1)

- EMOS được dùng nhiều trong IC số (và không cần phân cực trong các ứng dụng này)
- Người ta cũng sử dụng EMOS trong các mạch khuếch đại tín hiệu rời hay IC (cần phân cực trong các ứng dụng này)



Mạch phân cực cho N-EMOS



Các sụt áp trong mạch phân cực

Mạch phân cực N-EMOS (2) – DCLL

- R_S trong mạch phân cực dùng để ổn định phân cực như RE trong mạch BJT, chứ không phải có chức năng tự phân cực.
- R_S càng lớn thì điểm phân cực càng ít nhạy các tham số transistor khi nhiệt độ thay đổi hay thay transistor khác
- Từ mạch phân cực ta tìn được các sụt áp trong mạch như sau

$$V_G = \left(\frac{R_2}{R_1 + R_2}\right)V_{DD}$$

$$V_{GS} = V_G - I_D R_S$$

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

- Suy ra

$$I_D = -(1/R_S)V_{GS} + V_G/R_S$$

- Vẽ đường tải này trên đặc tuyến truyền đạt ta sẽ tìm ra được điểm tĩnh Q (V_{GSQ}, I_{DQ})

Mạch phân cực N-EMOS (3)
Phương pháp đại số

$$|V_G| = \frac{R_2}{R_1 + R_2}|V_{DD}|$$

$$I_D = \frac{-B - \sqrt{B^2 - 4AC}}{2A}$$

với

$$A = R_S^2$$

$$B = -2\left((|V_G| - |V_D|)R_S + \frac{1}{\beta}\right)$$

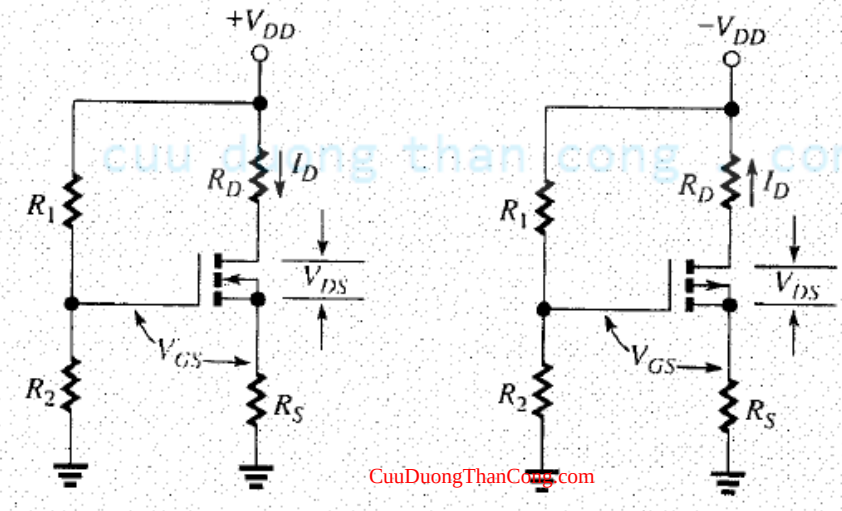
$$C = (|V_G| - |V_t|)^2$$

$$|V_{DS}| = |V_{DD}| - I_D(R_D + R_S) \quad \text{See note 1.}$$

$$|V_{GS}| = |V_G| - I_D R_S \quad \text{See note 2.}$$

Note 1. V_{DS} is positive for an NMOS FET and negative for a PMOS FET.

Note 2. V_{GS} is positive for an NMOS FET and negative for a PMOS FET.



Mạch phân cực N-EMOS (4) – TD

EXAMPLE 5–9

The transfer characteristic of the NMOS FET in Figure 5–40 is given in Figure 5–41 ($\beta = 0.5 \times 10^{-3}$ and $V_T = 2$ V). Determine values of V_{GS}, I_D, and V_{DS} at the bias point (1) graphically and (2) algebraically.

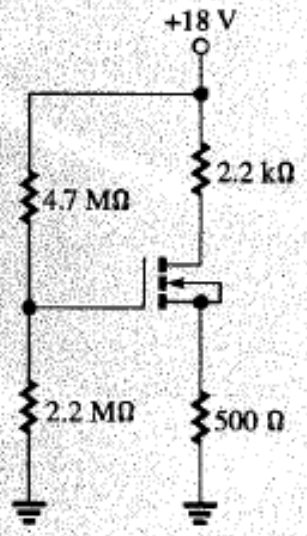


FIGURE 5–40
(Example 5–9).

Solution

1. From equation 5–13,

$$V_G = \left(\frac{22 \times 10^6}{47 \times 10^6 + 22 \times 10^6}\right) 18 \text{ V} = 5.74 \text{ V}$$

Substituting in equation 5–18, we have

$$I_D = -2 \times 10^{-3} V_{GS} + 11.48 \times 10^{-3}$$

This equation intersects the I_D-axis at 11.48 mA and the V_{GS}-axis at $V_G = 5.74$ V. It is shown plotted with the transfer characteristic in Figure 5–41. The two plots intersect at the quiescent point, where the values of I_D and V_{GS} are approximately $I_D = 2.0$ mA and $V_{GS} = 4.6$ V. The corresponding quiescent value of V_{DS} is found from equation 5–16:

$$V_{DS} = 18 - (2.0 \text{ mA})[(2.2 \text{ k}\Omega) + (0.5 \text{ k}\Omega)] = 12.60 \text{ V}$$

In order for this analysis to be valid, the Q-point must be in the saturation region: that is, we must have $V_{DS} > V_{GS} - V_T$. In our example, we have

Mạch phân cực N-EMOS (5) – TD

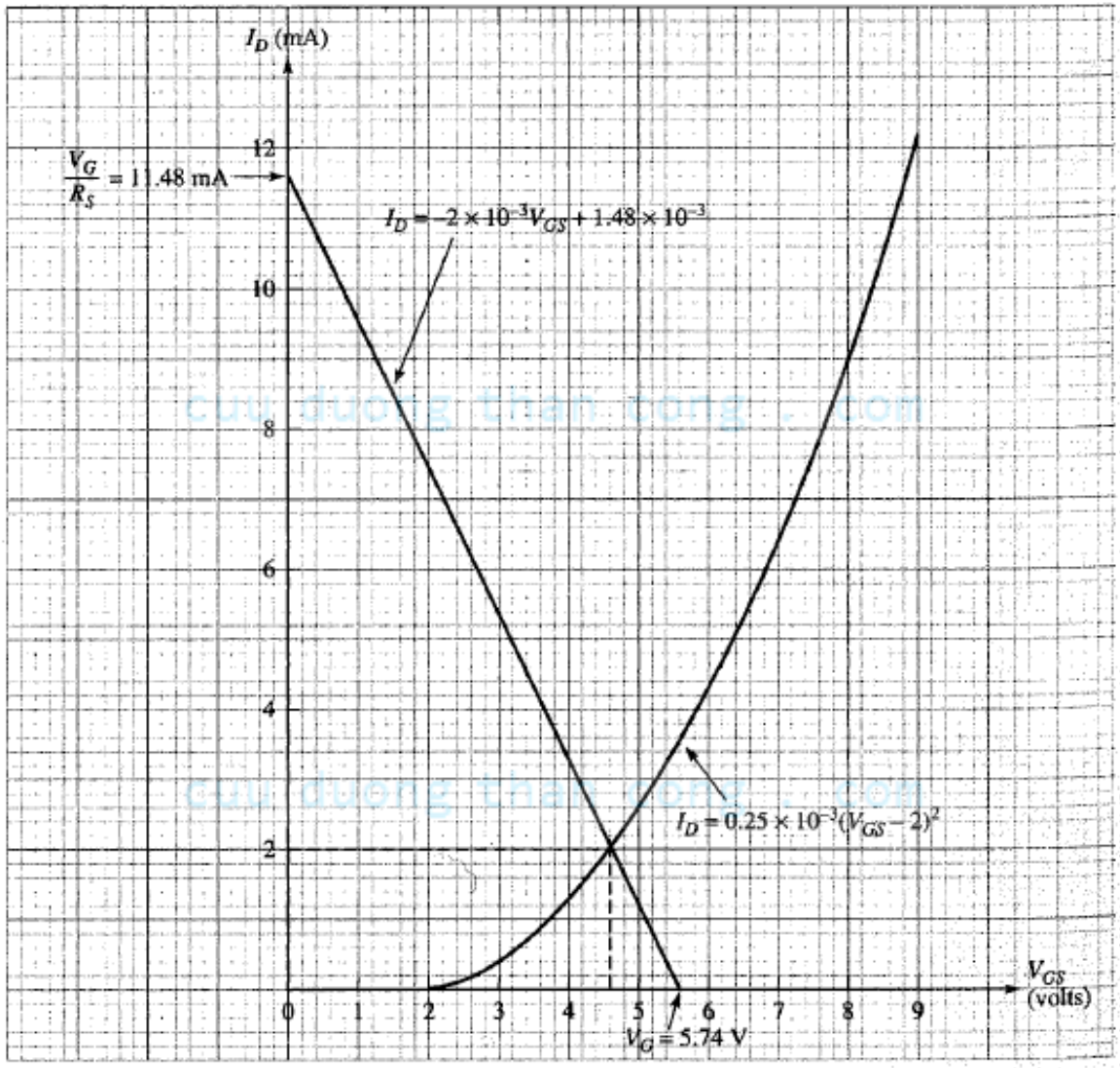


FIGURE 5–41 (Example 5–9)

Mạch phân cực N-EMOS (6) – TD

$V_{DS} = 12.60$ V and $V_{GS} - V_T = 2.6$ V, so we know the results are valid. The validity criterion can be expressed for both NMOS and PMOS FETs as $|V_{DS}| > |V_{GS} - V_T|$.

2. We have already found $V_G = 5.74$ V. Using $R_S = 500\ \Omega$, $R_D = 2.2\ \text{k}\Omega$, $V_{DD} = 18$ V, $V_T = 2$ V, and $\beta = 0.5 \times 10^{-3}$, we have, with reference to equations 5–19.

$$A = (500)^2 = 2.5 \times 10^5$$
$$B = -2[(5.74-2)500 + 1/(0.5 \times 10^{-3})] = -7.74 \times 10^3$$
$$C = (5.74-2)^2 = 13.9876$$

Substituting these values into the equation for I_D, we find $I_D = 1.927$ mA. Then, $V_{DS} = 18\ \text{V} - (1.927\ \text{mA})(2.2\ \text{k}\Omega + 500\ \Omega) = 12.8$ V and $V_{GS} = 5.74\ \text{V} - (1.927\ \text{mA})(500\ \Omega) = 4.78$ V. These results agree well with those obtained graphically in part 1.

NMOSFET in OFF State

- We had previously assumed that there is no channel current when $V_{GS} < V_{TH}$. This is incorrect!
- As V_{GS} is reduced below V_{TH} (towards 0 V), the potential barrier to carrier diffusion from the source into the channel is increased. **I_D becomes limited by carrier diffusion** into the channel, rather than by carrier drift through the channel.

  (This is similar to the case of a PN junction diode!)

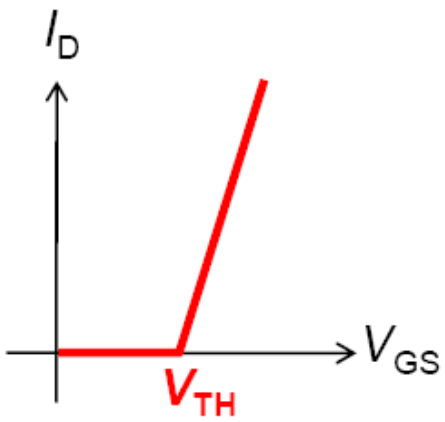
  → I_D varies exponentially with the potential barrier height at the source, which varies directly with the channel potential.

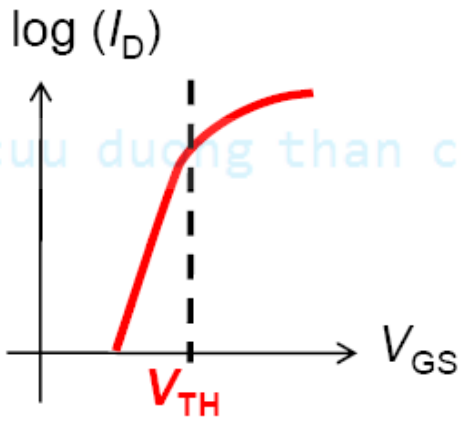
Sub-Threshold Leakage Current

- Recall that, in the depletion (sub-threshold) region of operation, the channel potential is capacitively coupled to the gate potential. A change in gate voltage (ΔV_{GS}) results in a change in channel voltage (ΔV_{CS}):

$$\Delta V_{CS} = \Delta V_{GS} \times \left(\frac{C_{ox}}{C_{ox} + C_{dep}} \right) \equiv \Delta V_{GS} / m \quad ; \quad m = 1 + \frac{C_{dep}}{C_{ox}} > 1$$

- Therefore, the sub-threshold current ($I_{D,subth}$) decreases exponentially with linearly decreasing V_{GS}/m



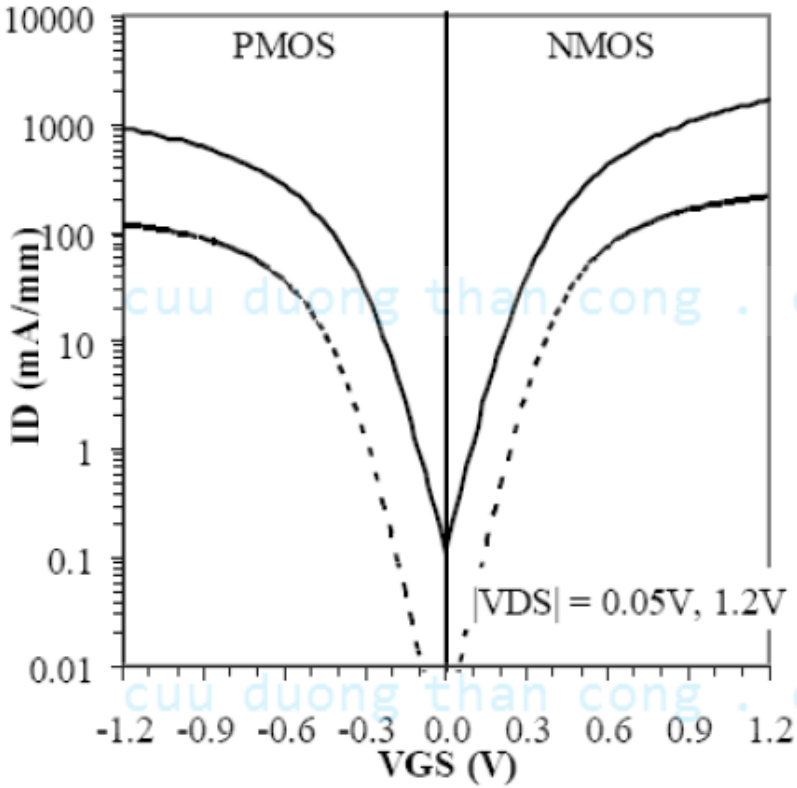


Sub-threshold swing:

$$S \equiv \left(\frac{d(\log_{10} I_{DS})}{dV_{GS}} \right)^{-1}$$

$$S = mV_T \ln(10) > 60\text{mV/dec}$$

Short-Channel MOSFET I_D-V_{GS}



Sub-threshold curves (I_{DS}-V_{GS}) for 35nm gate lengths

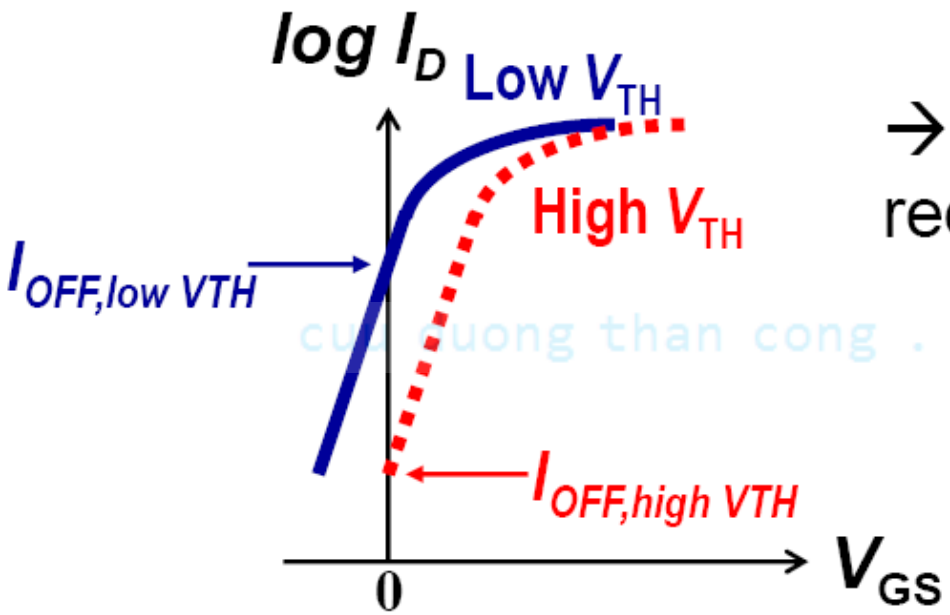
P. Bai et al. (Intel Corp.), *Int'l Electron Devices Meeting*, 2004.

V_{TH} Design Trade-Off

- Low V_{TH} is desirable for high ON-state current:

$$I_{D,sat} \propto (V_{DD} - V_{TH})^{\eta} \qquad 1 < \eta < 2$$

- But high V_{TH} is needed for low OFF-state current:



→ V_{TH} cannot be reduced aggressively.

MOSFET Transconductance, g_m

- Transconductance (g_m) is a measure of how much the drain current changes when the gate voltage changes.

$$g_m \equiv \frac{\partial I_D}{\partial V_{GS}}$$

- For amplifier applications, the MOSFET is usually operating in the saturation region.
  - **For a long-channel MOSFET:**

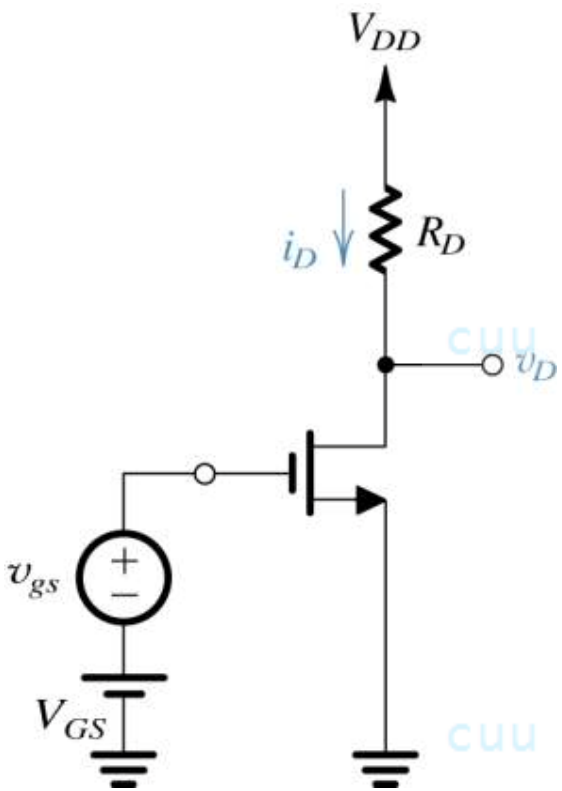
$$g_m = \mu_n C_{ox} \frac{W}{L}\left(V_{GS} - V_{TH}\right)\left\{1 + \lambda\left(V_{DS} - V_{D,sat}\right)\right\} = \frac{2I_D}{V_{GS} - V_{TH}}$$

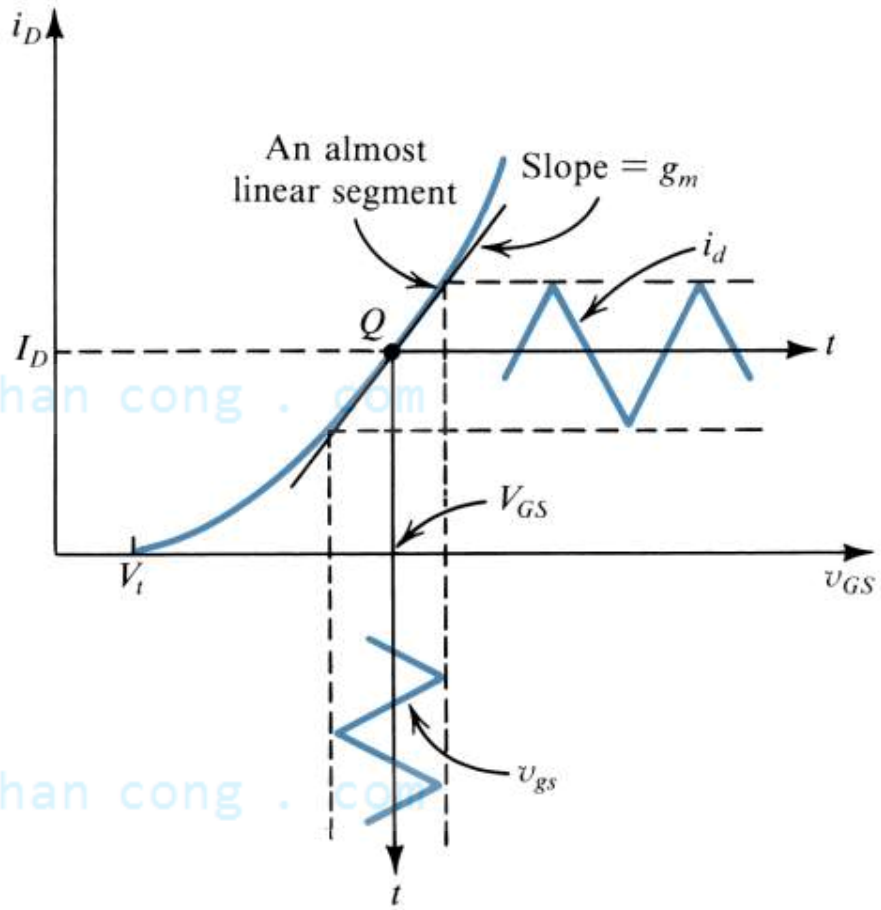
  - **For a short-channel MOSFET:**

$$g_m = v_{sat} W C_{ox}\left\{1 + \lambda\left(V_{DS} - V_{D,sat}\right)\right\} = \frac{I_D}{V_{GS} - V_{TH}}$$

MOSFET
Mạch tương đương tín hiệu nhỏ

MOSFET như mạch khuếch đại

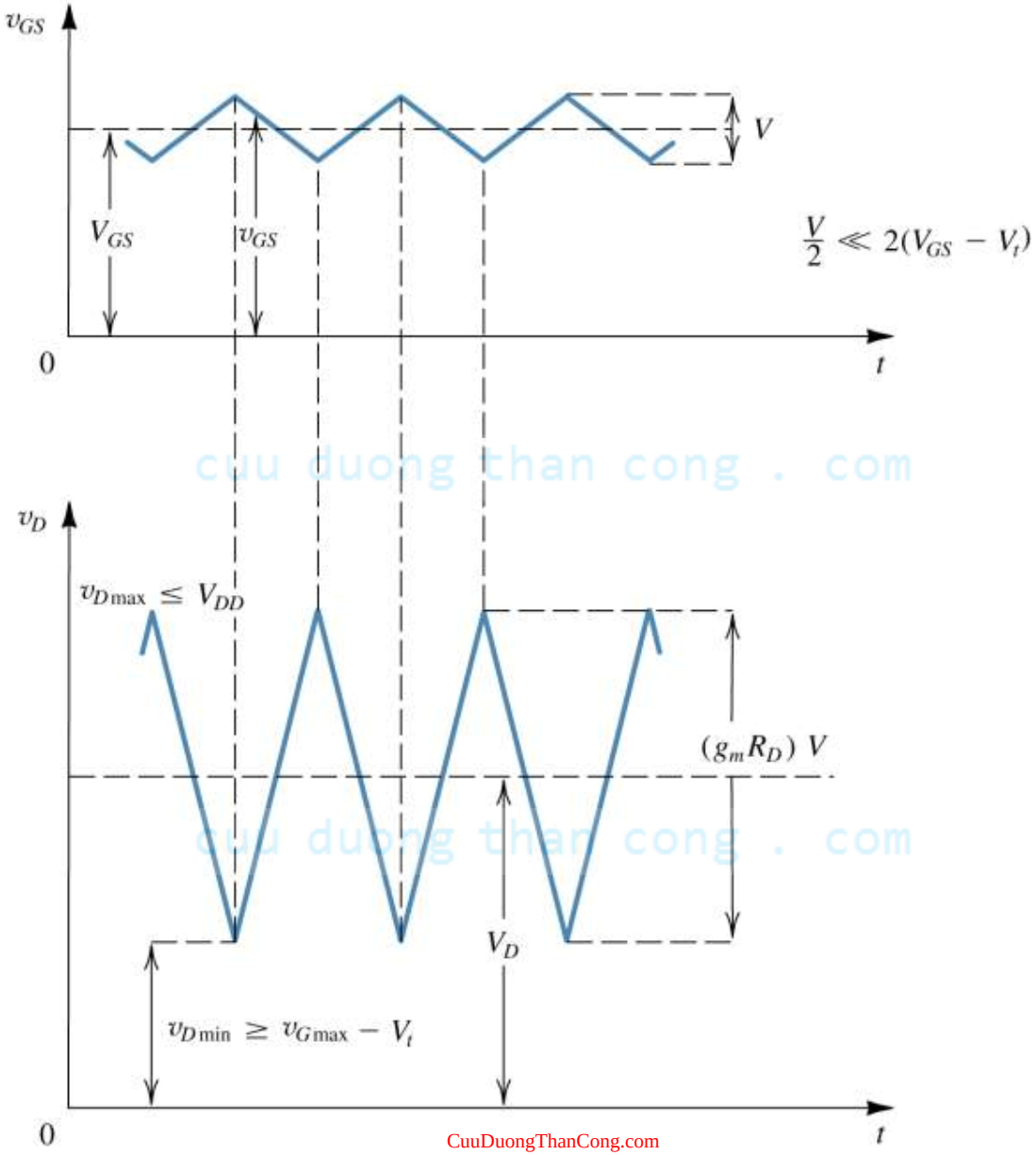




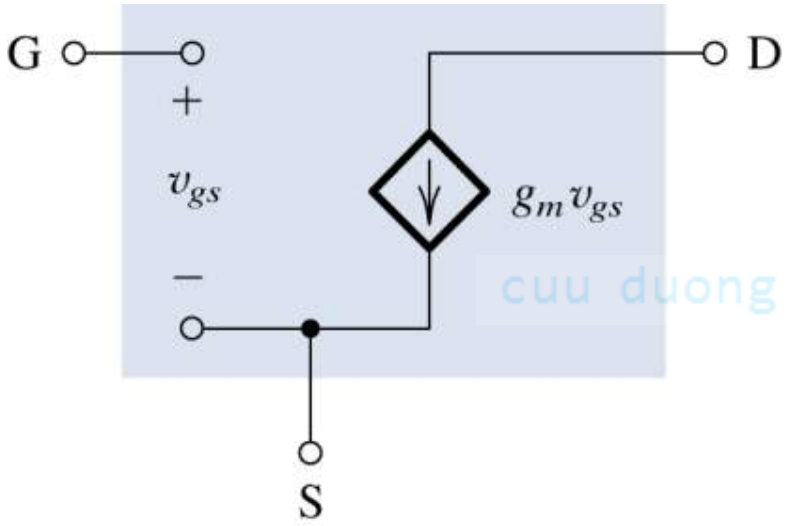
a) Mạch khảo sát tính chất KĐ

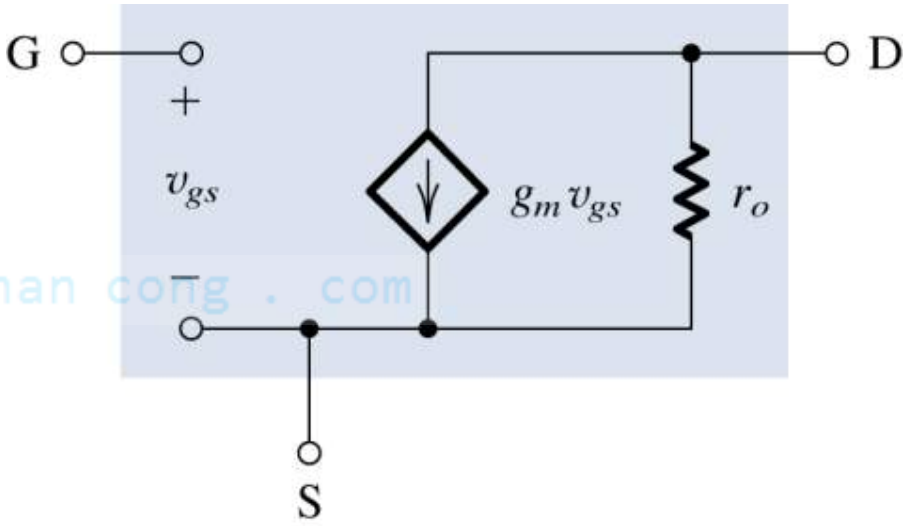
b) Giải tích tín hiệu nhỏ (AC)

Giải tích toàn phần (DC+AC)



Mô hình tín hiệu nhỏ – Mô hình pi

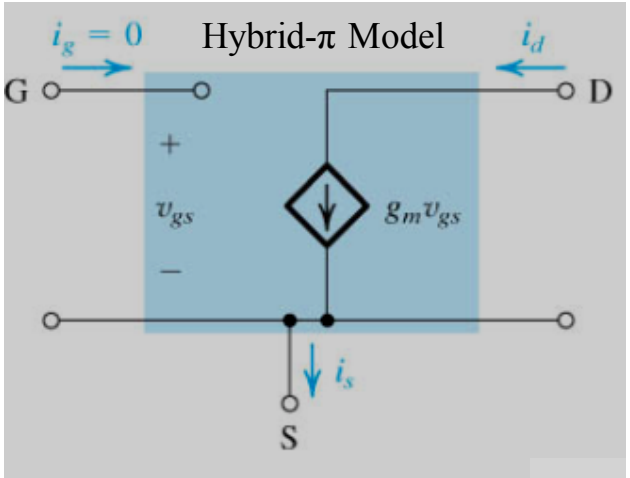


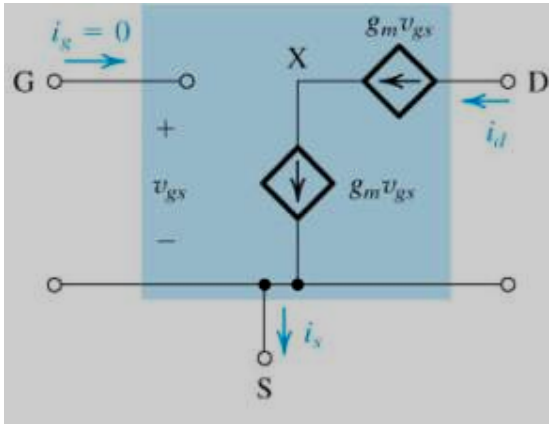


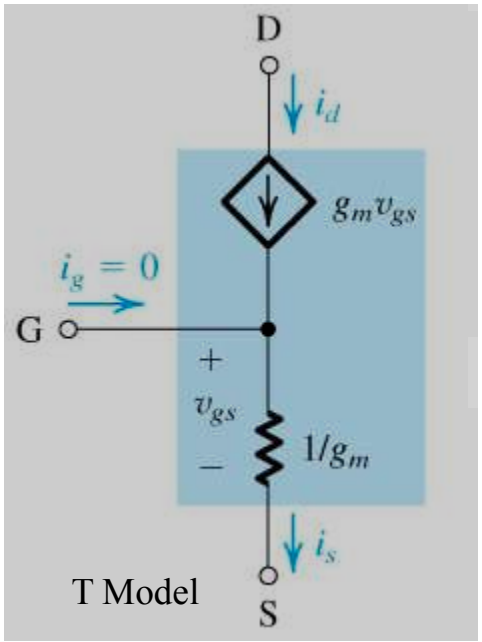
a) Bỏ qua sự phụ thuộc của I_D vào V_{DS} ở chế độ bão hòa

b) Kể đến hiệu ứng điều chế chiều dài kênh dẫn bởi điện trở ra $r_o = |V_A|/I_D$.

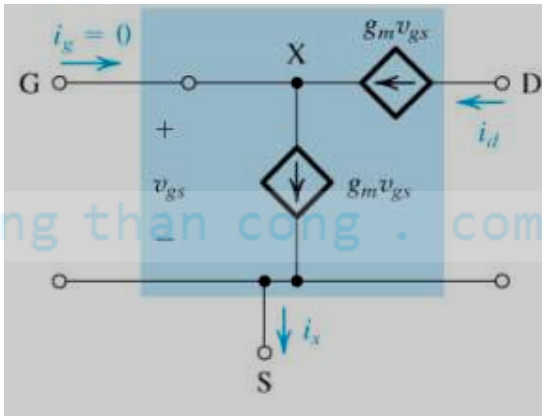
Mô hình tín hiệu nhỏ – Mô hình T

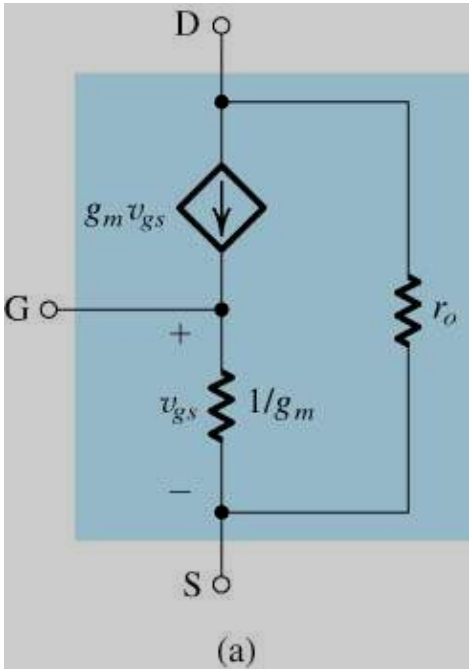






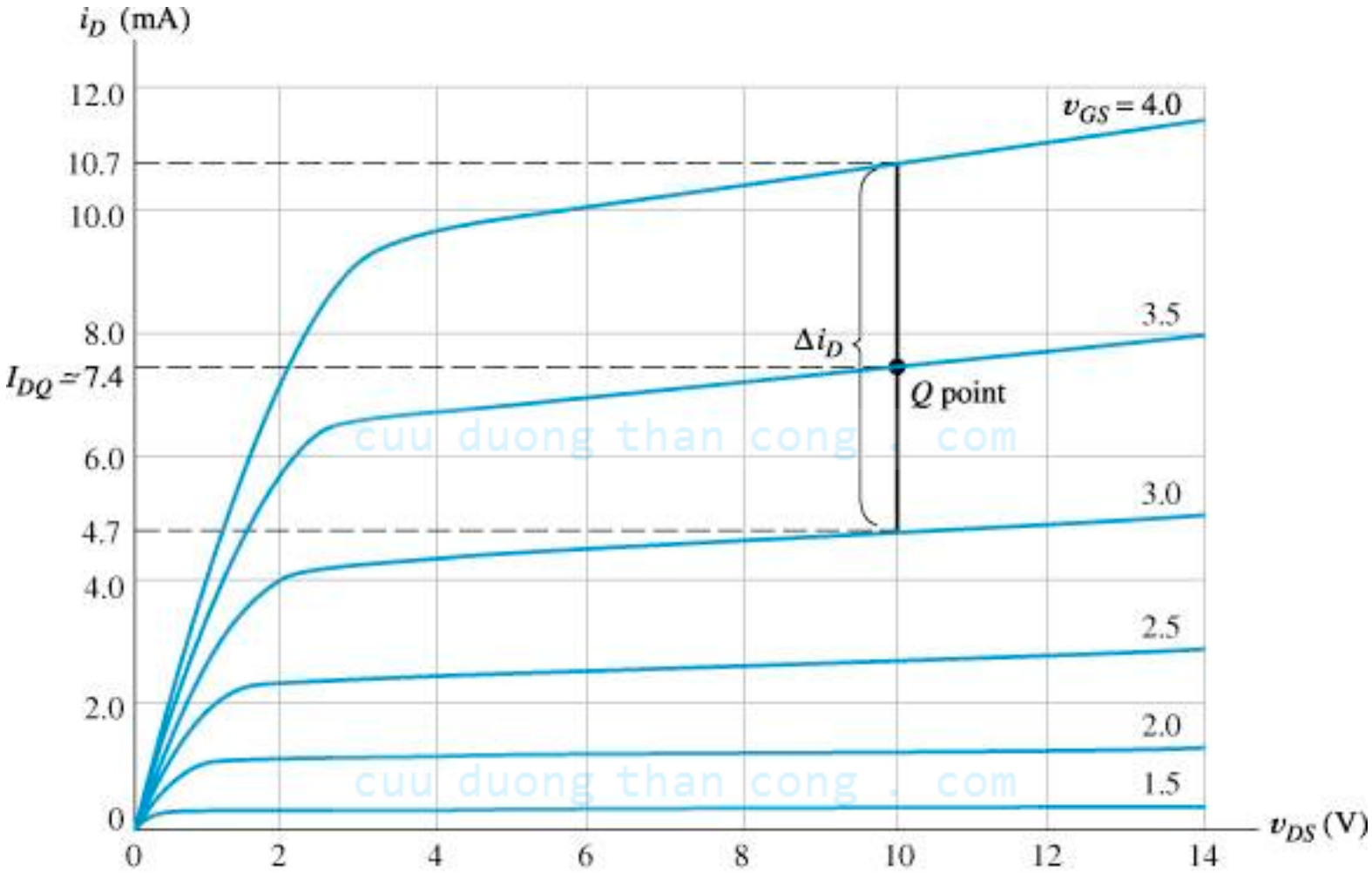
Mô hình T chưa kể r_O





Mô hình T với r_O

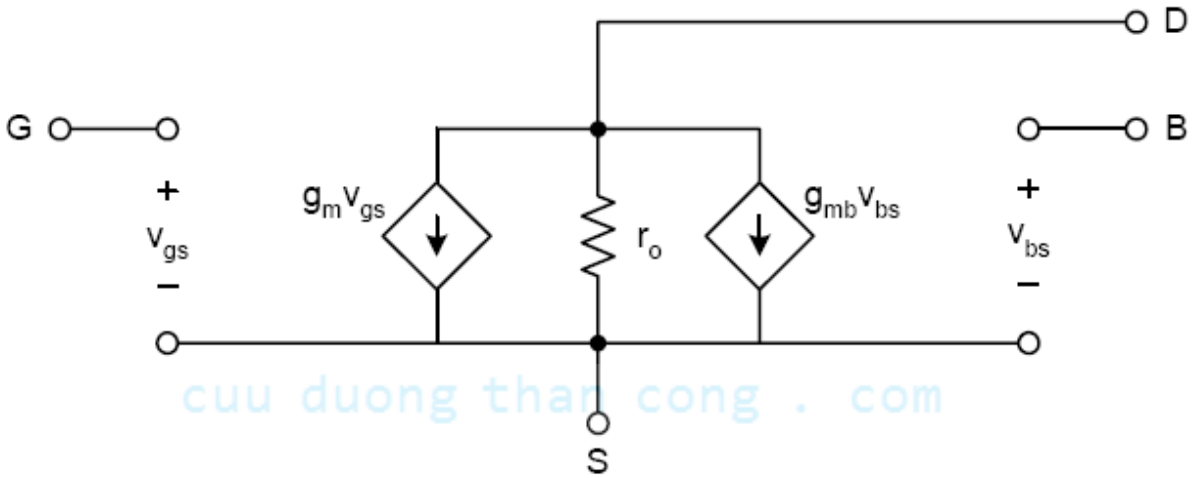
Cách tìm g_m và r_o bằng đặc tuyến ra



$$g_m = \Delta I_D / \Delta V_{GS}$$

$$r_O = (V_A + V_{DS})/I_D \approx V_A/I_D$$

Body Effect



$$g_{mb} \equiv \left.\frac{\partial i_d}{\partial v_{BS}}\right|_{v_{GS} \text{ and } v_{DS} \text{ constant}}$$

$$g_{mb} = \frac{\gamma}{2\sqrt{2\phi_f + V_{SB}}} g_m$$

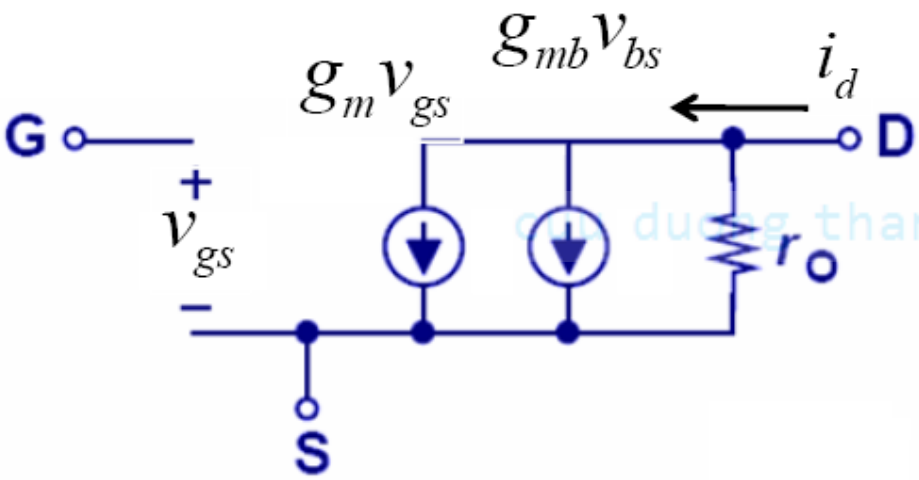
- Body Effect
  - We saw that the substrate bias V_{BS} affects V_t which has the effect of influencing current like another gate

Derivation of Small-Signal Model

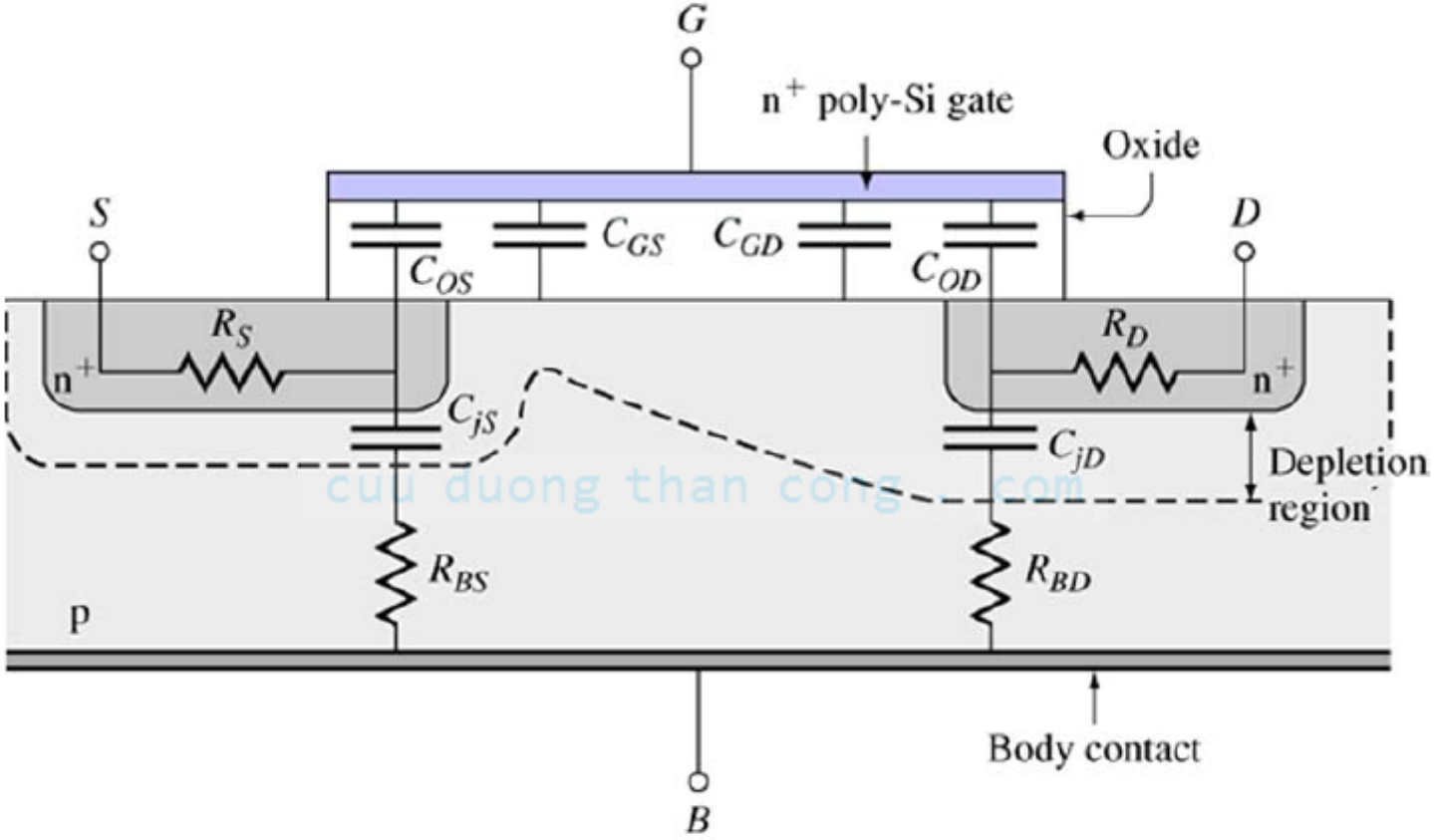
(Long-Channel MOSFET, Saturation Region)

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{GS} - V_{TH}\right)^2\left[1 + \lambda\left(V_{DS} - V_{D,sat}\right)\right]$$

$$i_d = \frac{\partial I_D}{\partial V_{GS}} v_{gs} + \frac{\partial I_D}{\partial V_{BS}} v_{bs} + \frac{\partial I_D}{\partial V_{DS}} v_{ds} \equiv g_m v_{gs} + g_{mb} v_{bs} + \frac{1}{r_o} v_{ds}$$

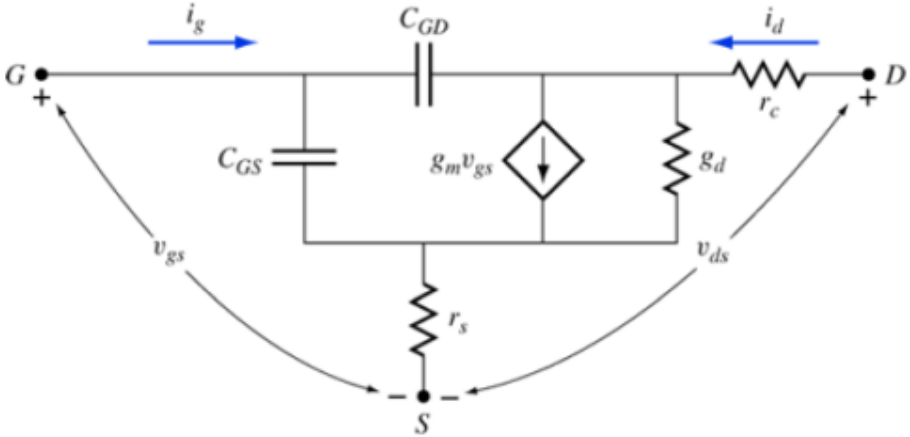


Mạch tương đương N-EMOS

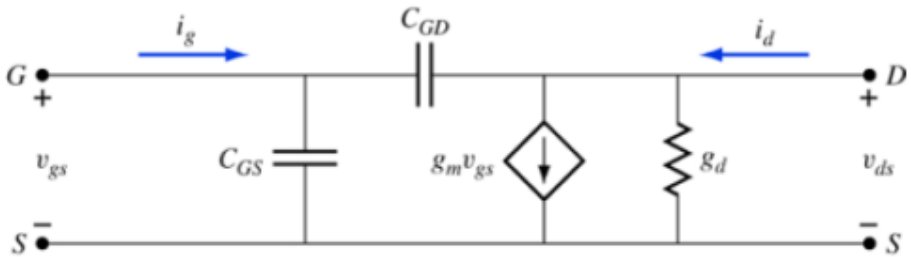


Mạch trên cho thấy N-EMOS có nhiều thành phần điện trở và tụ điện

Mạch tương đương tín hiệu nhỏ của MOSFET



(a) Ở tần số cao



(b) Bỏ qua các điện trở nguồn và máng

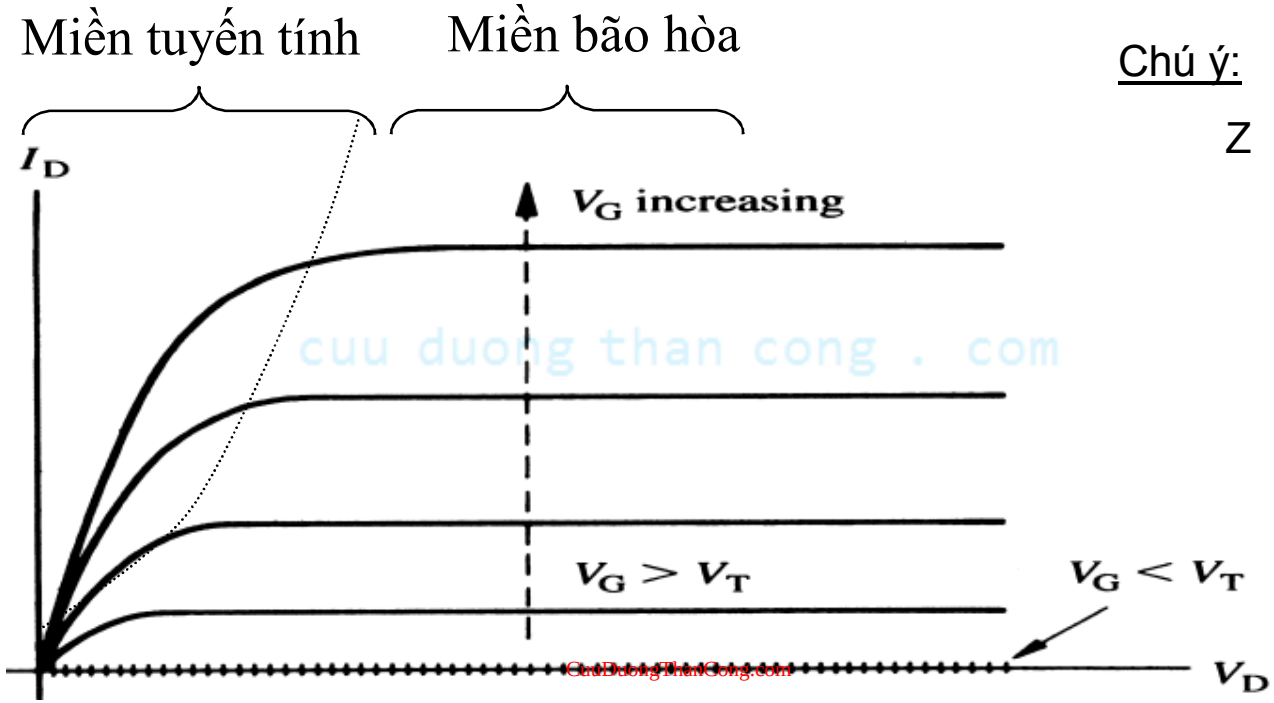
(c) Ở tần số thấp

MOSFET – Mạch tương đương tín hiệu nhỏ

Với N-EMOS ta có:

$$I_D = \frac{Z\mu_n}{L} C_{ox}\left[\left(V_G - V_{TN}\right)V_{DS} - \frac{V_{DS}^2}{2}\right] \qquad 0 < V_{DS} < V_{DS,sat} \quad ; \quad V_G > V_{TN}$$

$$I_{D,sat} = \frac{Z\mu C_{ox}}{2L}\left(V_G - V_{TN}\right)^2 \qquad V_{DS} > V_{DS,sat} \quad ; \quad V_G > V_{TN}$$

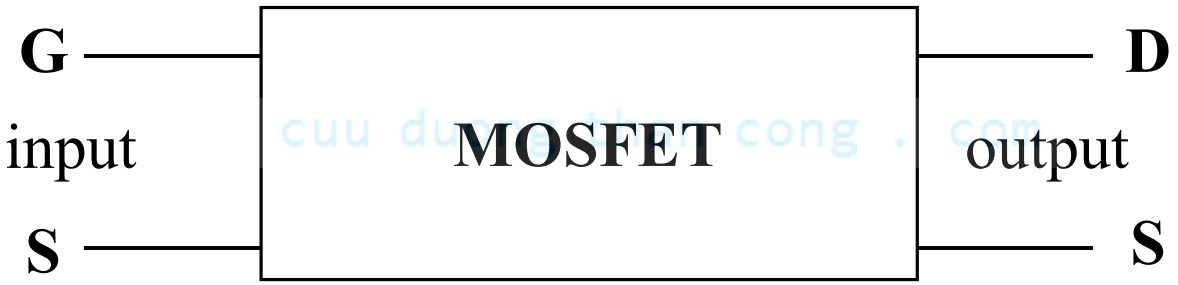


Chú ý:

Z = W

MOSFET – Đáp ứng AC

- Thường được biểu diễn qua mạch thụ động tín hiệu nhỏ
- Suy từ mạng 2 cổng sau:



Cổng vào coi như hở mạch, nogại trừ có tụ ở cực cổng

Đầu ra, dòng I_D được điều khiển bởi V_G và V_{DS}.

$$I_D = f(V_G, V_{DS})$$

MOSFET – Mạch tương đương tín hiệu nhỏ

Khi có bất kỳ tín hiệu AC ở V_G hay V_{DS} sẽ sinh ra sự thay đổi ở I_D

$$\Delta I_D = \left.\frac{\partial I_D}{\partial V_G}\right|_{V_{DS}} \Delta V_G + \left.\frac{\partial I_D}{\partial V_{DS}}\right|_{V_G} \Delta V_{DS}$$

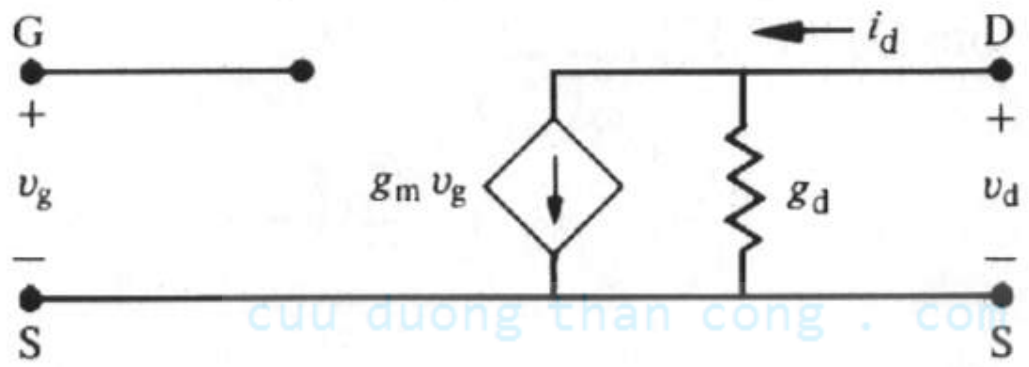
$$i_d = g_m v_g + g_d v_d$$ với $$g_m = \left.\frac{\partial I_D}{\partial V_G}\right|_{V_{DS}}$$ và $$g_d = \left.\frac{\partial I_D}{\partial V_{DS}}\right|_{V_G}$$

g_m = hỗ dẫn

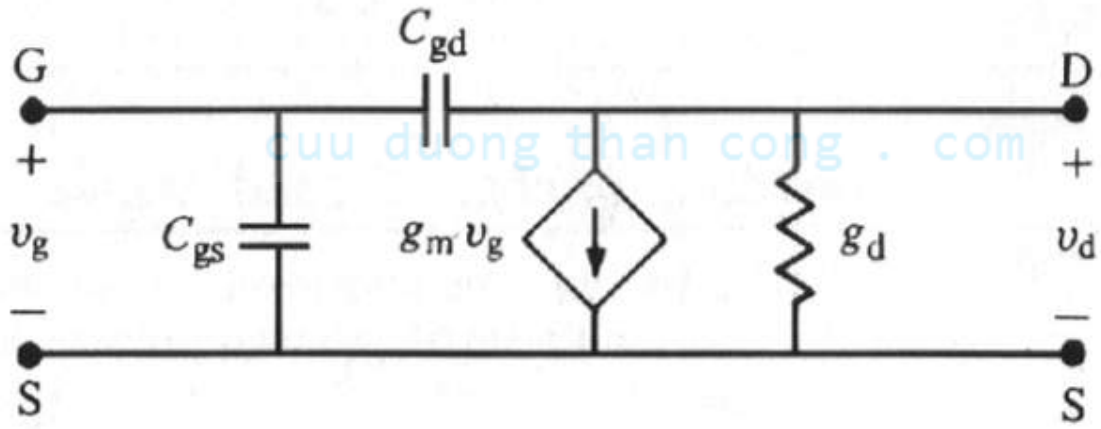
g_d = điện dẫn của máng hay kênh dẫn

Mạch tương đương tín hiệu nhỏ

Ở tần số thấp hoặc trung bình:



Ở tần số cao:



MOSFET – Các tham số tín hiệu nhỏ

Khi $V_{DS} < V_{DS,sat}$ (i.e., thấp hơn pinch-off hay miền tuyến tính)

$$g_d = \frac{Z\mu_n C_{ox}}{L}(V_G - V_{TN} - V_{DS})$$

$$g_m = \frac{Z\mu_n C_{ox}}{L} V_{DS}$$

Khi $V_{DS} > V_{DS,sat}$ (i.e., trên pinch-off hay miền bão hòa)

$$g_d = 0$$

$$g_m = \frac{Z\mu_n C_{ox}}{L}(V_G - V_{TN})$$

***Chú ý*: Các tham số phụ thuộc vào phân cực DC, V_G và V_{DS}**

MOSFET – Đáp ứng tần số

Tần số cắt f_T được định nghĩa là tần số làm cho độ lợi dòng là 1.

Dòng vào = $j\omega C_G v_G$

Dòng ra = $g_m v_G$

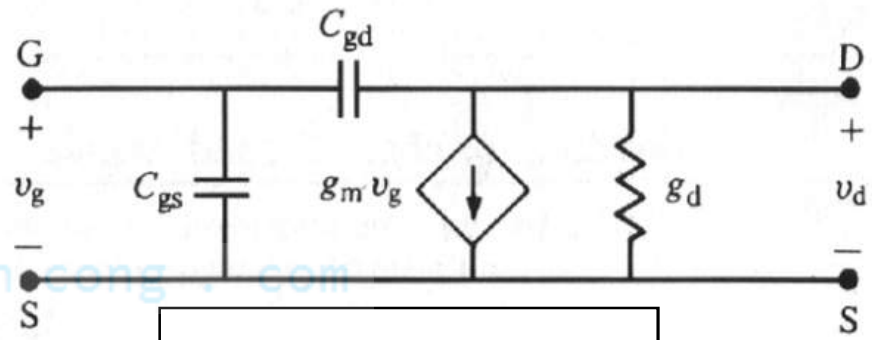
v_G ở đây là tín hiệu AC
C_{GS} xấp xỉ bằng điện dung cổng,
$C_{GS} \approx ZLC_{ox}$

Do đó ở f_T :

$$\frac{g_m v_G}{2\pi f_T \times C_{GS} v_G} = 1$$

Suy ra

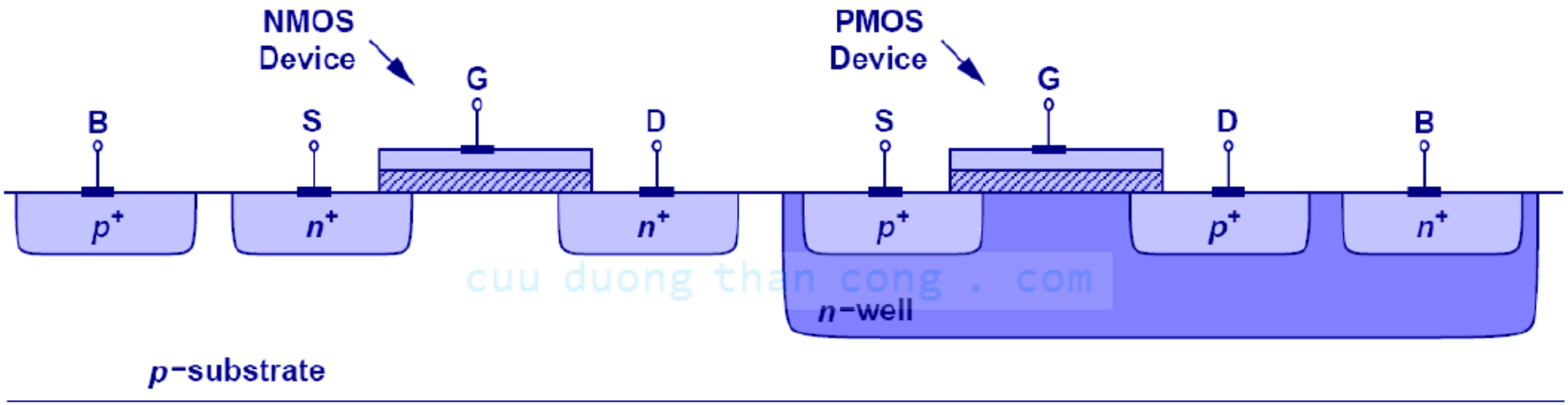
$$f_T = \frac{g_m}{2\pi C_{GS}}$$



Chính xác:

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}$$

Công nghệ CMOS



- It possible to grow an n-well inside a p-substrate to create a technology where both NMOS and PMOS can coexist.
- It is known as CMOS, or "Complementary MOS".

So sánh BJT và MOSFET

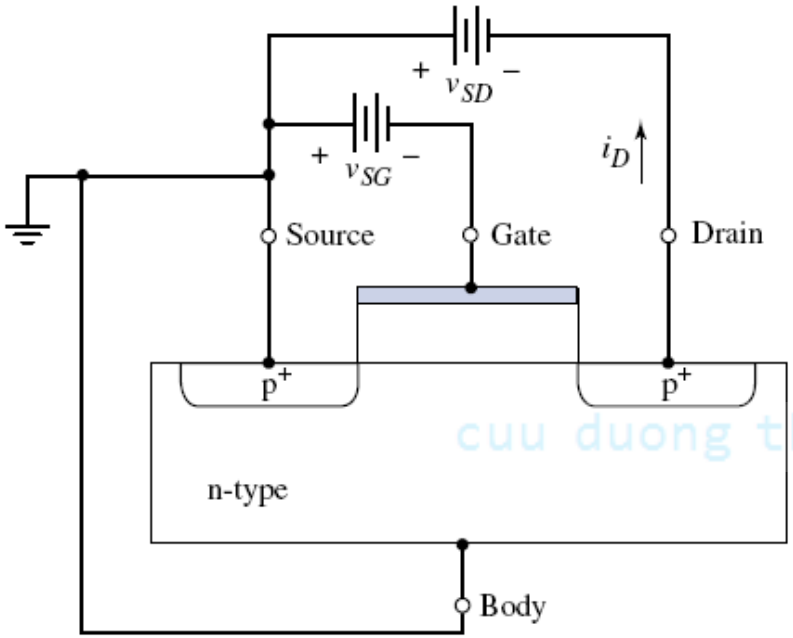
Bipolar Transistor	MOSFET
Exponential Characteristic	Quadratic Characteristic
Active: $V_{CB} > 0$	Saturation: $V_{DS} > V_{GS} - V_{TH}$
Saturation: $V_{CB} < 0$	Triode: $V_{DS} < V_{GS} - V_{TH}$
Finite Base Current	Zero Gate Current
Early Effect	Channel−Length Modulation
Diffusion Current	Drift Current
–	Voltage−Dependent Resistor

- Bipolar devices have a higher gm than MOSFETs for a given bias current due to its exponential IV characteristics.

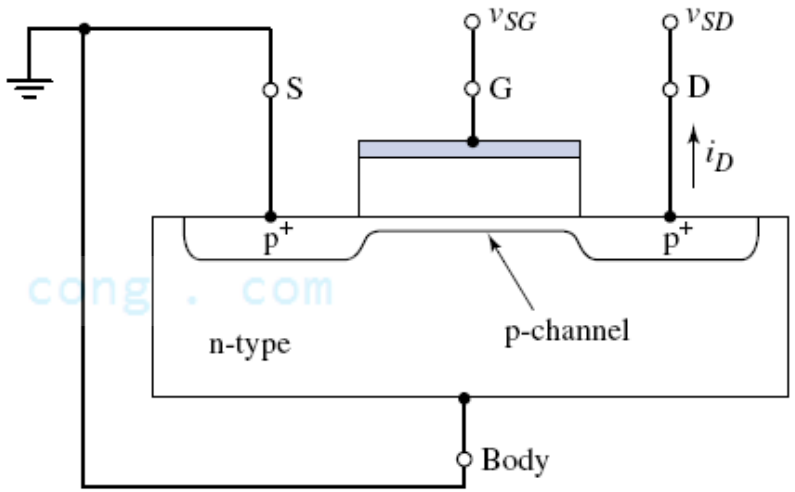
MOSFET loại nghèo (D-MOS)

- Cấu trúc
- Phương trình
- Đặc tuyến

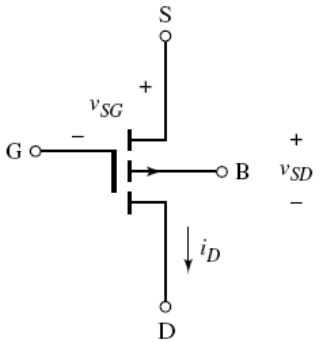
Cấu trúc của P-MOS

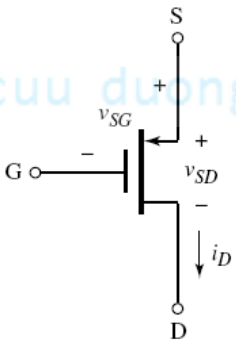


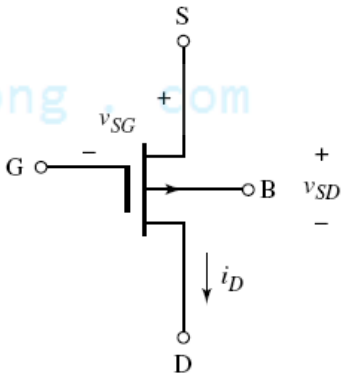
(a) P-EMOS

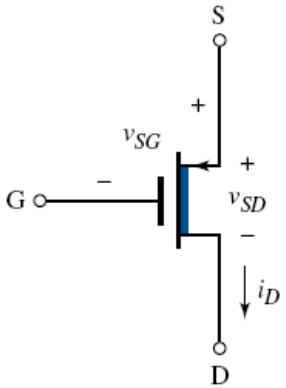


(b) P-DMOS

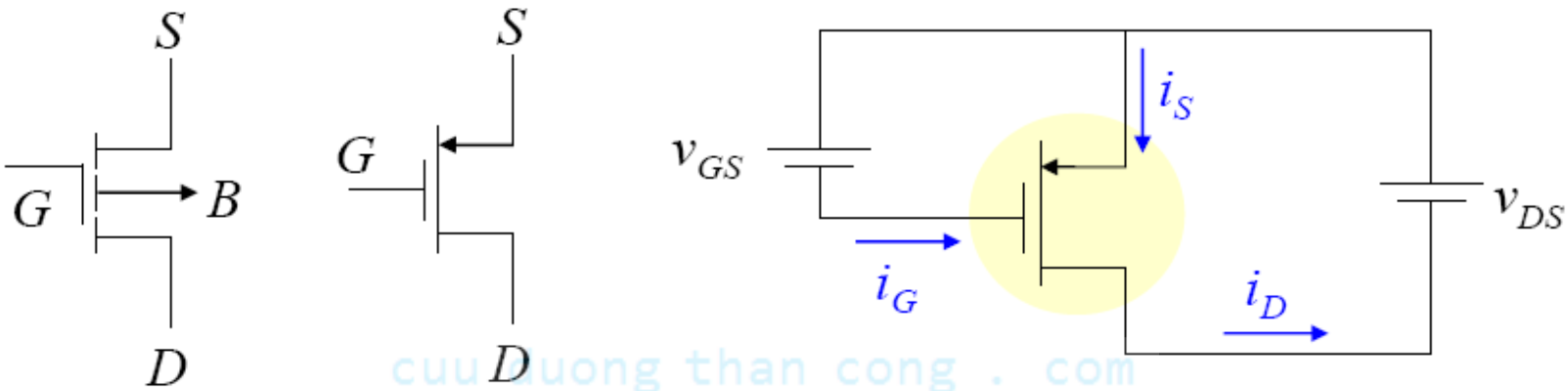








Các phương trình của P-EMOS



Induced Channel: $v_{GS} \le V_T$ V_T, v_{GS}, v_{DS}, *and* λ *are negative*

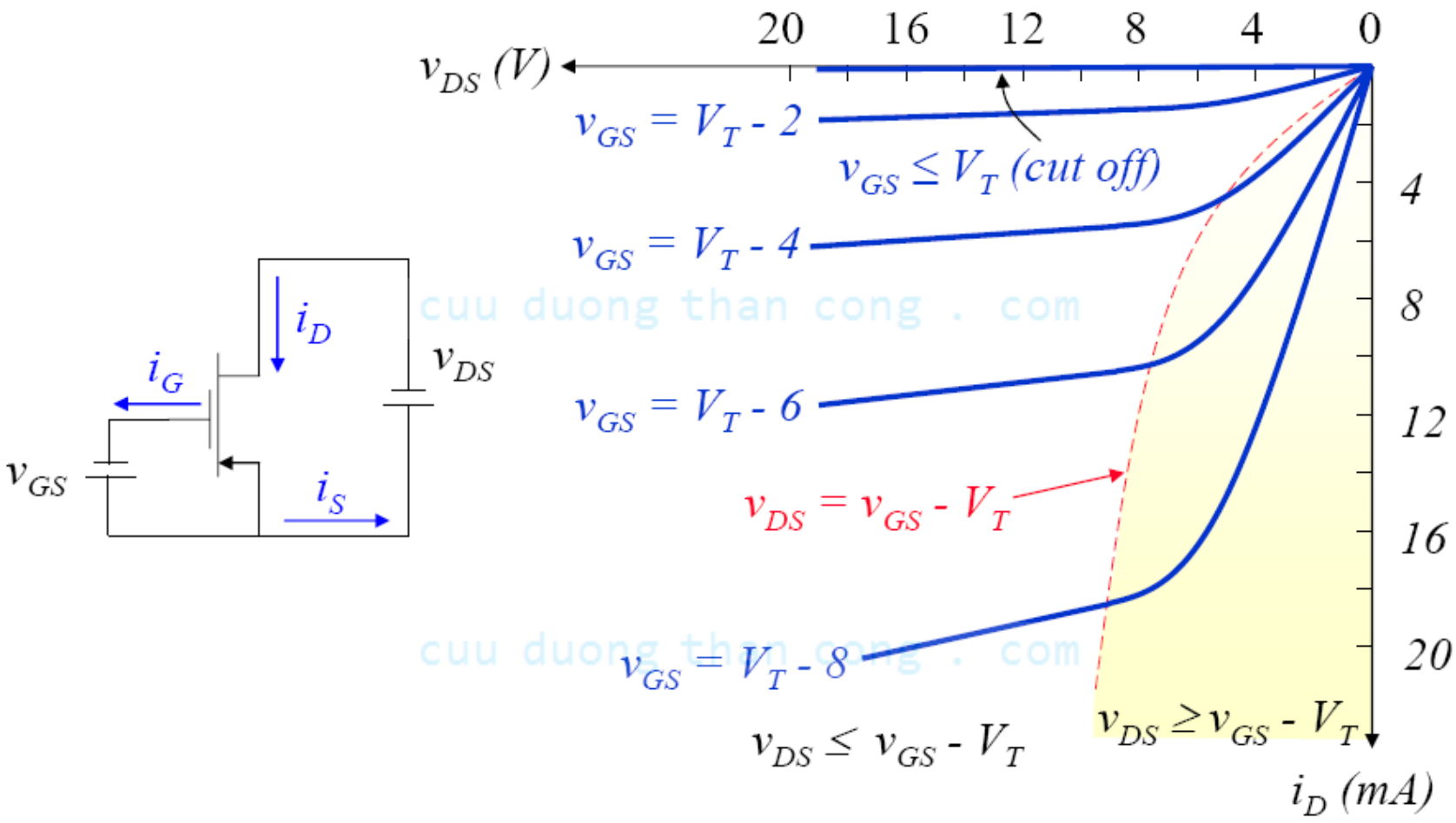
Triode Region:
$(v_{DS} \ge v_{GS} - V_T)$

$$i_D = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)\left[2(v_{GS} - V_T)v_{DS} - v_{DS}^2\right]$$

Saturation Region:
$(v_{DS} \le v_{GS} - V_T)$

$$i_D = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)(v_{GS} - V_T)^2(1 + \lambda v_{DS})$$

Đặc tuyến I-V của P-EMOS

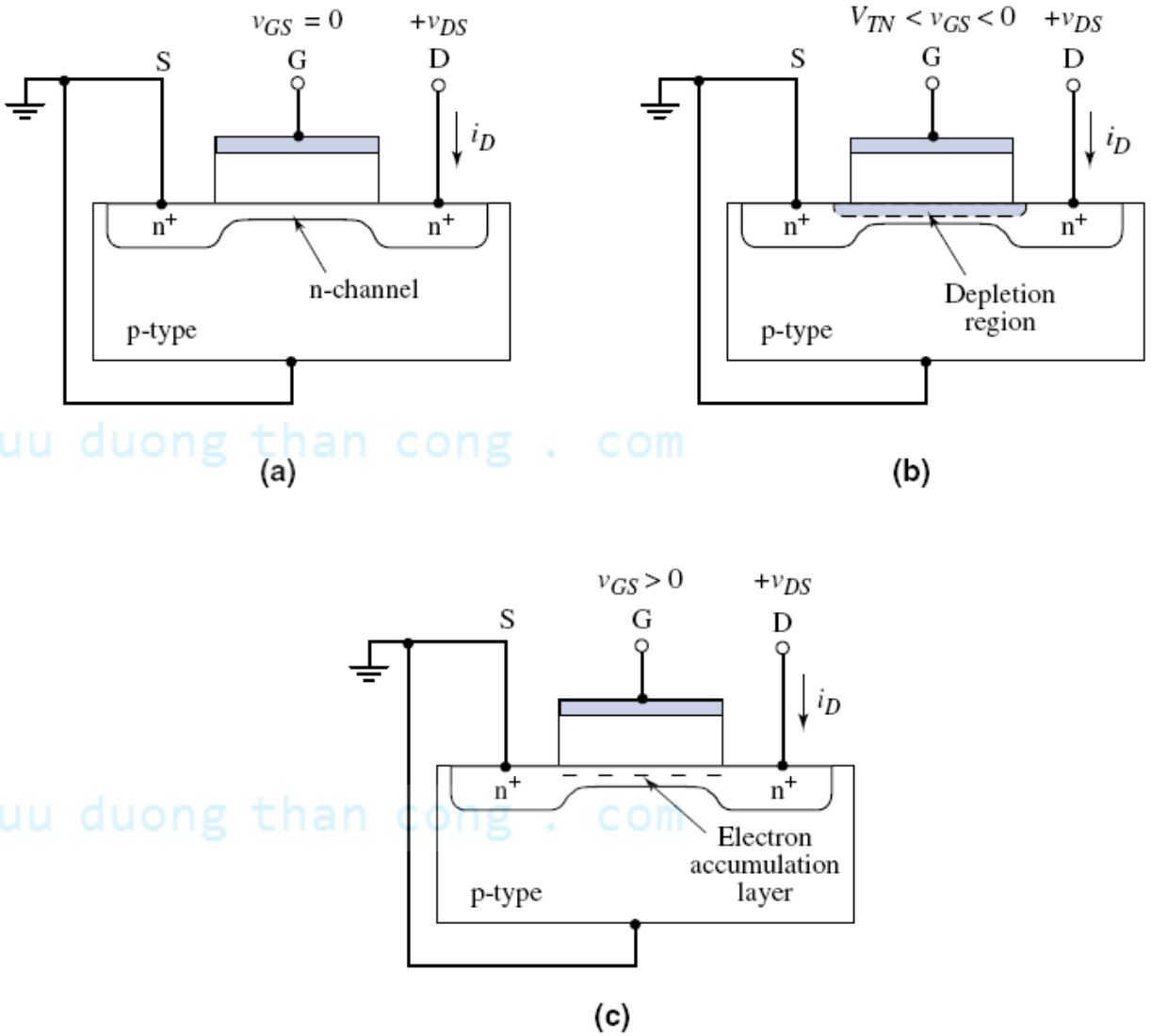


Cấu trúc của N-DMOS

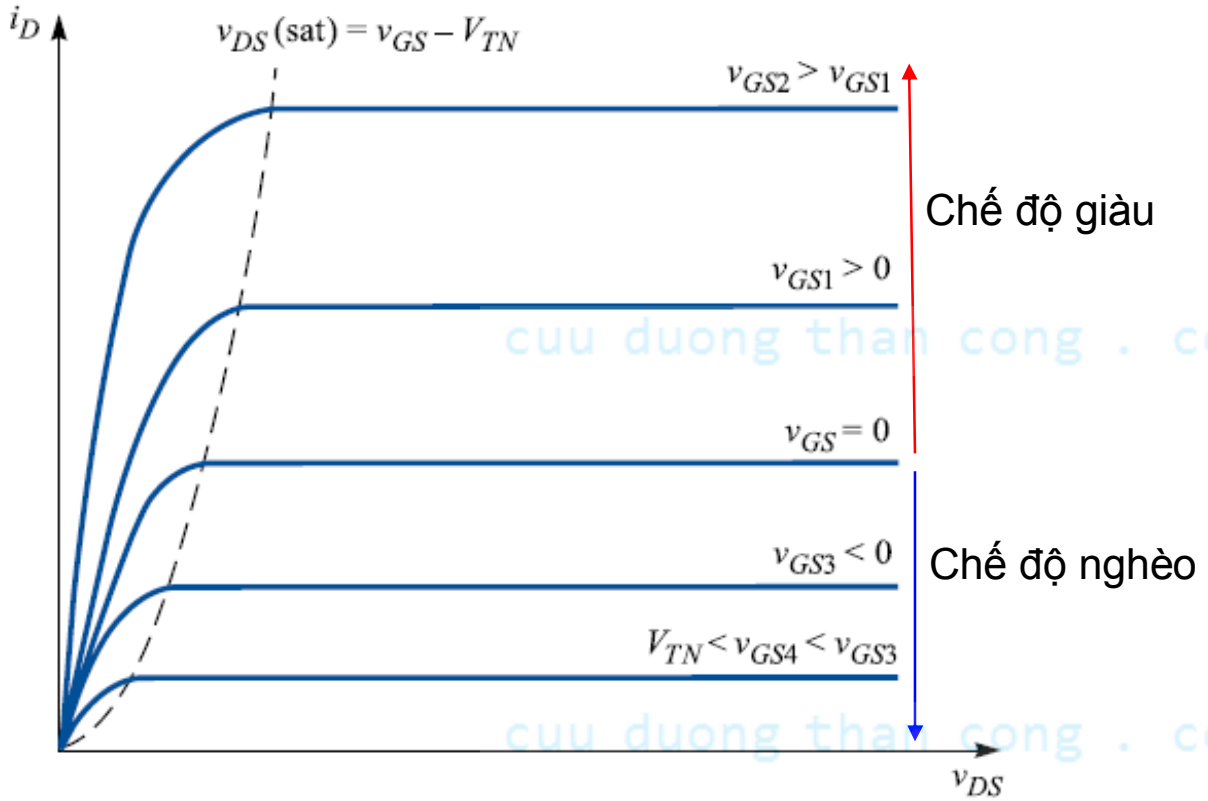
- The term depletion mode means that a channel exists even at zero gate voltage

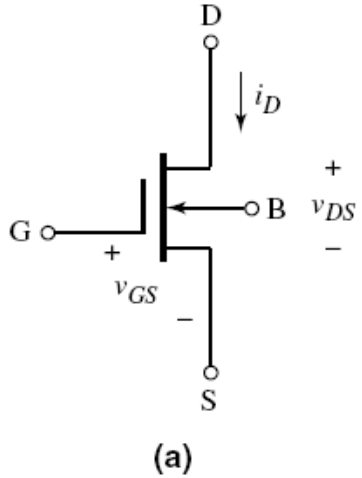
- A negative gate voltage must be applied to the n-channel depletion-mode MOSFET to turn the device off.

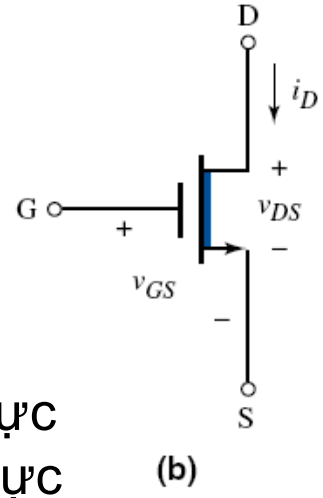
- The V_{TN} is positive for the enhancement-mode MOSFET and negative for the depletionmode



Đặc tuyến ra và ký hiệu của N-DMOS







Chú ý:

- Chế độ giàu: dòng tăng hơn so với khi chưa phân cực
- Chế độ nghèo: dòng giảm đi so với khi chưa phân cực

Tóm tắt các quan hệ dòng-áp của MOSFET

NMOS	PMOS
Miền tắt ($V_{GS} \le V_{TN}$): $I_D = 0$ Miền triode ($V_{GS} > V_{TN}$ và $0 \le V_{DS} < V_{DS,sat}$) $I_D = K_n\left[2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2\right]$ với $K_n = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}$ Miền bão hòa ($V_{GS} > V_{TN}$ và $V_{DS} \ge V_{DS,sat}$) $I_D = K_n(V_{GS} - V_{TN})^2$ $g_m = 2K_n(V_{GSQ} - V_{TN}) = 2\sqrt{K_n I_{DQ}}$ Điểm chuyển tiếp $V_{DS,sat} = V_{GS} - V_{TN}$ Loại giàu: $V_{TN} > 0$ Loại nghèo: $V_{TN} < 0$	Miền tắt ($V_{GS} \ge V_{TP}$): $I_D = 0$ Miền triode ($V_{GS} < V_{TP}$ và $0 \ge V_{DS} > V_{DS,sat}$) $I_D = K_p\left[2(V_{GS} - V_{TP})V_{DS} - V_{DS}^2\right]$ với $K_p = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}$ Miền bão hòa ($V_{GS} < V_{TP}$ và $V_{DS} \le V_{DS,sat}$) $I_D = K_p(V_{GS} - V_{TP})^2$ $g_m = -2K_p(V_{GSQ} - V_{TP}) = 2\sqrt{K_p I_{DQ}}$ Điểm chuyển tiếp $V_{DS,sat} = V_{GS} - V_{TP}$ Loại giàu: $V_{TP} < 0$ Loại nghèo: $V_{TP} > 0$

Example 5.2 **Objective:** Determine the source-to-drain voltage required to bias a p-channel depletion-mode MOSFET in the saturation region.

Consider a depletion-mode p-channel MOSFET for which $K_p = 0.2\,\text{mA/V}^2$, $V_{TP} = +0.50\,\text{V}$, and $i_D = 0.50\,\text{mA}$.

Solution: In the saturation region, the drain current is given by

$$i_D = K_p(v_{SG} + V_{TP})^2$$

or

$$0.50 = 0.2(v_{SG} + 0.50)^2$$

which yields

$$v_{SG} = 1.08\,\text{V}$$

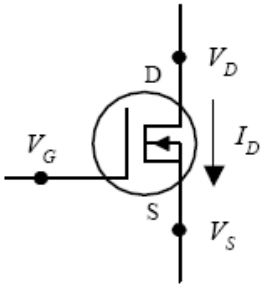
To bias this p-channel MOSFET in the saturation region, the following must apply:

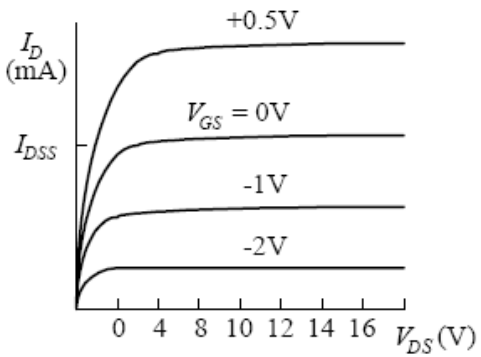
$$v_{SD} > v_{SD}(\text{sat}) = v_{SG} + V_{TP} = 1.08 + 0.5 = 1.58\,\text{V}$$

Comment: Biasing a transistor in either the saturation or the nonsaturation region depends on both the gate-to-source voltage and the drain-to-source voltage.

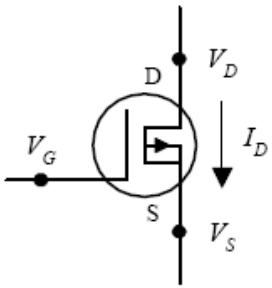
Tóm tắt các loại MOSFET (1/4)

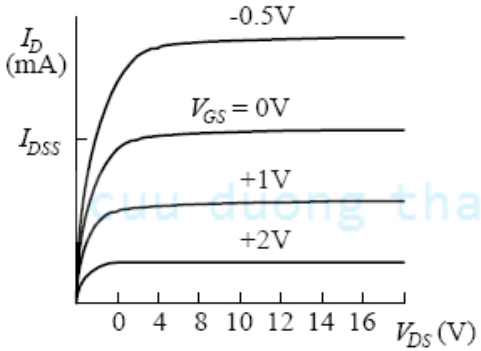
N-CHANNEL DEPLETION-TYPE MOSFET





P-CHANNEL DEPLETION-TYPE MOSFET





OHMIC REGION MOSFET is just beginning to resist. In this region, the MOSFET behaves like a resistor.

ACTIVE REGION MOSFET is most strongly influenced by gate-source voltage (V_{GS}) but hardly at all influenced by drain-source voltage (V_{DS}).

CUTOFF VOLTAGE ($V_{GS,off}$) Often referred to as the *pinch-off voltage* (V_p). Represents the particular gate-source voltage that causes the MOSFET to block most all drain-source current flow.

BREAKDOWN VOLTAGE (BV_{DS}) The drain-source voltage (V_{DS}) that causes current to "break through" MOSFET's resistive channel.

DRAIN CURRENT FOR ZERO BIAS (I_{DSS}) Represents the drain current when gate-source voltage is zero volts (or when gate is shorted to source).

TRANSCONDUCTANCE (g_m) Represents the rate of change in the drain current with change in gate-source voltage when drain-

Tóm tắt các loại MOSFET (2/4)

Useful Formulas for Depletion-Type MOSFETs

DRAIN CURRENT (OHMIC REGION)

$$I_D = I_{DSS}\left[2\left(1 - \frac{V_{GS}}{V_{GS,\text{off}}}\right)\frac{V_{DS}}{-V_{GS,\text{off}}} - \left(\frac{V_{DS}}{V_{GS,\text{off}}}\right)^2\right]$$

DRAIN CURRENT (ACTIVE REGION)

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS,\text{off}}}\right)^2$$

DRAIN-SOURCE RESISTANCE

$$R_{DS} = \frac{V_{DS}}{I_D} \approx \frac{V_{GS,\text{off}}}{2I_{DSS}(V_{GS} - V_{GS,\text{off}})} = \frac{1}{g_m}$$

ON RESISTANCE

$$R_{DS,\text{on}} = \text{constant}$$

DRAIN-SOURCE VOLTAGE

$$V_{DS} = V_D - V_S$$

TRANSCONDUCTANCE

$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS}} = \frac{1}{R_{DS}}$$

$$= g_{m_0}\left(1 - \frac{V_{GS}}{V_{GS,\text{off}}}\right) = g_{m_0}\sqrt{\frac{I_D}{I_{DSS}}}$$

TRANSCONDUCTANCE FOR SHORTED GATE

$$g_{m_0} = \frac{2I_{DSS}}{V_{GS,\text{off}}}$$

An n-channel JFET's $V_{GS,\text{off}}$ is negative. A p-channel JFET's $V_{GS,\text{off}}$ is positive.

$V_{GS,\text{off}}$, I_{DSS} are typically the knowns (you get their values by looking them up in a data table or on the package).

Typical JFET values:

I_{DSS}: 1 mA to 1 A

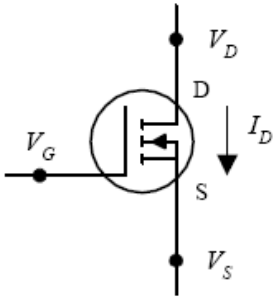
$V_{GS,\text{off}}$:
–0.5 to –10 V (n-channel)
0.5 to 10 V (p-channel)

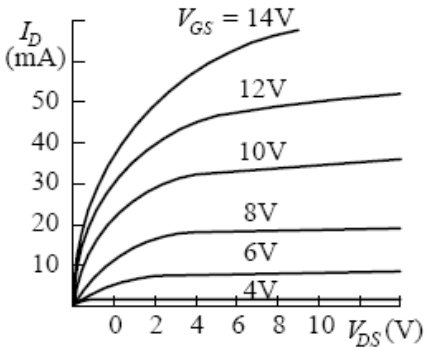
$R_{DS,\text{on}}$: 10 to 1000 Ω

BV_{DS}: 6 to 50 V

g_m at 1 mA:
500 to 3000 μmho

Tóm tắt các loại MOSFET (3/4)



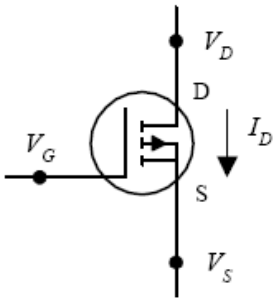


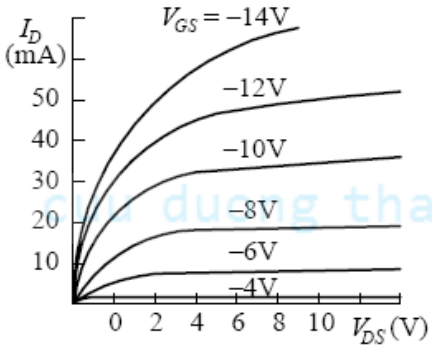
OHMIC REGION MOSFET is just beginning to conduct. Acts like a variable resistor.

ACTIVE REGION MOSFET is most strongly influenced by gate-source voltage V_{GS} but hardly at all influenced by drain-source voltage V_{DS}.

THRESHOLD VOLTAGE ($V_{GS,th}$) Particular gate-source voltage where MOSFET is just beginning to conduct.

BREAKDOWN VOLTAGE (BV_{DS}) The voltage across drain source (V_{DS}) that causes current to "break through" MOSFET's resistance channel.





DRAIN-CURRENT FOR GIVEN BIAS ($I_{D,on}$) Represents the amount of current I_D at a particular V_{GS}, which is given on data sheets, etc.

TRANSCONDUCTANCE (g_m) Represents the rate of change in the drain current with the change is gate-source voltage when drain-source voltage is fixed. It is analogous to the transconductance (I/R_{tr}) for bipolar transistors.

Tóm tắt các loại MOSFET (4/4)

DRAIN CURRENT (OHMIC REGION)

$$I_D = k[2(V_{GS} - V_{GS,th})V_{DS} - \tfrac{1}{2}V_{DS}^2]$$

DRAIN CURRENT (ACTIVE REGION)

$$I_D = k(V_{GS} - V_{GS,th})^2$$

The value of the construction parameter k is proportional to the width/length ratio of the transistor's channel and is dependent on temperature. It can be determined by using the construction parameter equations to the left.

CONSTRUCTION PARAMETER

$$k = \frac{I_D}{(V_{GS} - V_{GS,th})^2}$$

$$= \frac{I_{D,on}}{(V_{GS,on} - V_{GS,th})^2}$$

$V_{GS,th}$ is positive for n-channel enhancement MOSFETs.
$V_{GS,th}$ is negative for p-channel enhancement MOSFETs.

Typical values

$I_{D,on}$: 1 mA to 1 A

$R_{DS(on)}$: 1 Ω to 10 kΩ

$V_{GS,off}$: 0.5 to 10 V

$BV_{DS(off)}$: 6 to 50 V

$BV_{GS(off)}$: 6 to 50 V

TRANSCONDUCTANCE

$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS}} = \frac{1}{R_{DS}}$$

$$= 2k(V_{GS} - V_{GS,th}) = 2\sqrt{kI_D}$$

$$= g_{m_0}\sqrt{\frac{I_D}{I_{D_o}}}$$

$V_{GS,th}$, $I_{D,on}$, g_m at a particular I_D are typically "knowns" you can find in the data tables or on package labels.

RESISTANCE OF DRAIN-SOURCE CHANNEL

$$R_{DS} = 1/g_m$$

$$R_{DS_2} = \frac{V_{G_1} - V_{GS,th}}{V_{G_2} - V_{GS,th}} R_{DS_1}$$

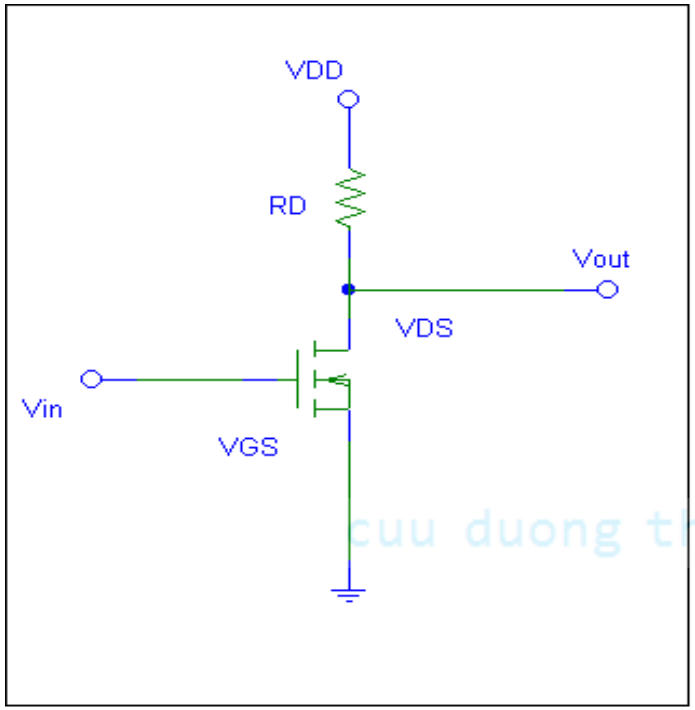
R_{DS_1} is the known resistance at a given voltage V_{G_1}. R_{DS_2} is the resistance you calculate at another gate voltage V_{G_2}.

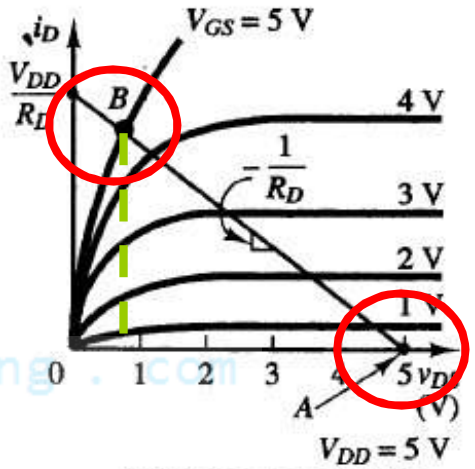
Transistors as Switches- MOSFET

- <u>Advantages over BJT logic gates</u>
  - Normally Off. Does not require much current from input signal
  - Easy Fabrication – Economical for large scale production
  - CMOS – consumes very little power. Used in pocket calculators and wrist watches

- <u>Disadvantages over BJT logic gates</u>
  - Cannot provide as much current as BJT
  - Switching speed is not as fast

Transistors as Switches- MOSFET Inverter



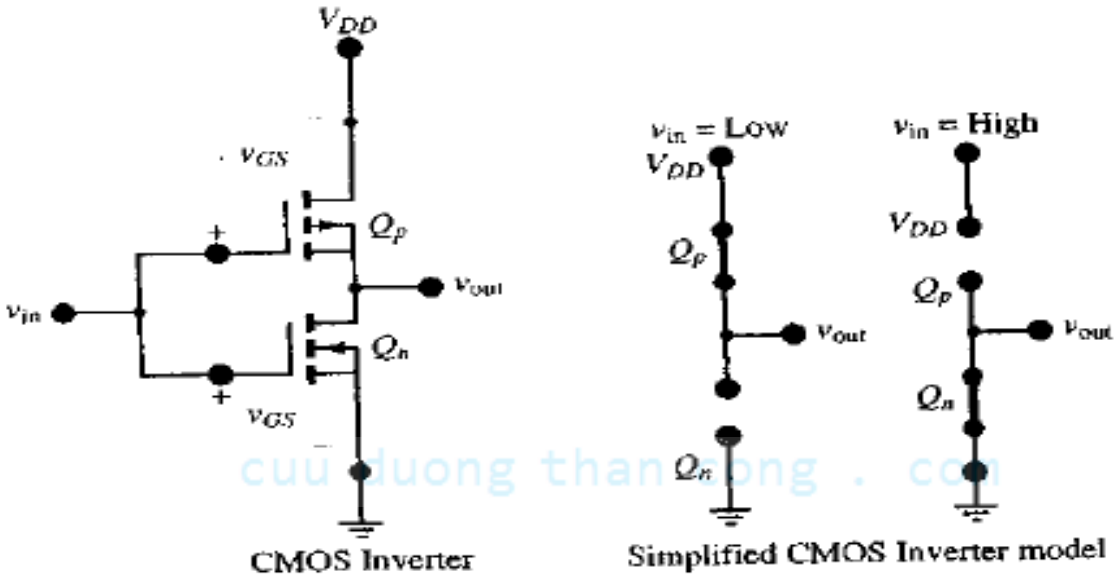


Switching characteristic

- <u>Vin Low</u>
  - Cutoff region
  - No Voltage drop across RD
  - Vout = VDD
- <u>Vout = High</u>

- <u>Vin High</u>
  - Ohmic region
  - VDS small
  - Vout = small
- <u>Vout = Low</u>

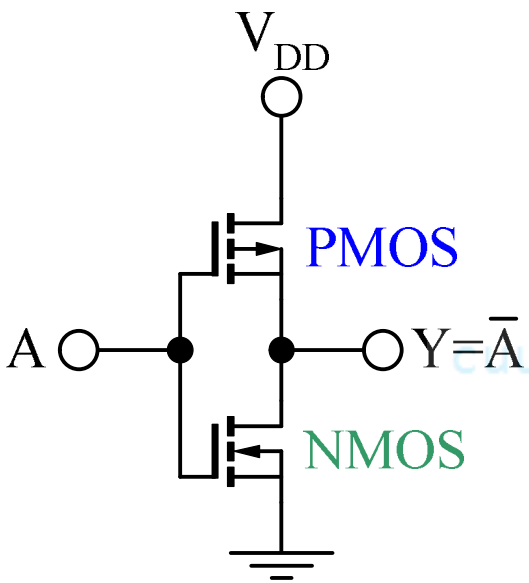
Transistors as Switches- CMOS Inverter



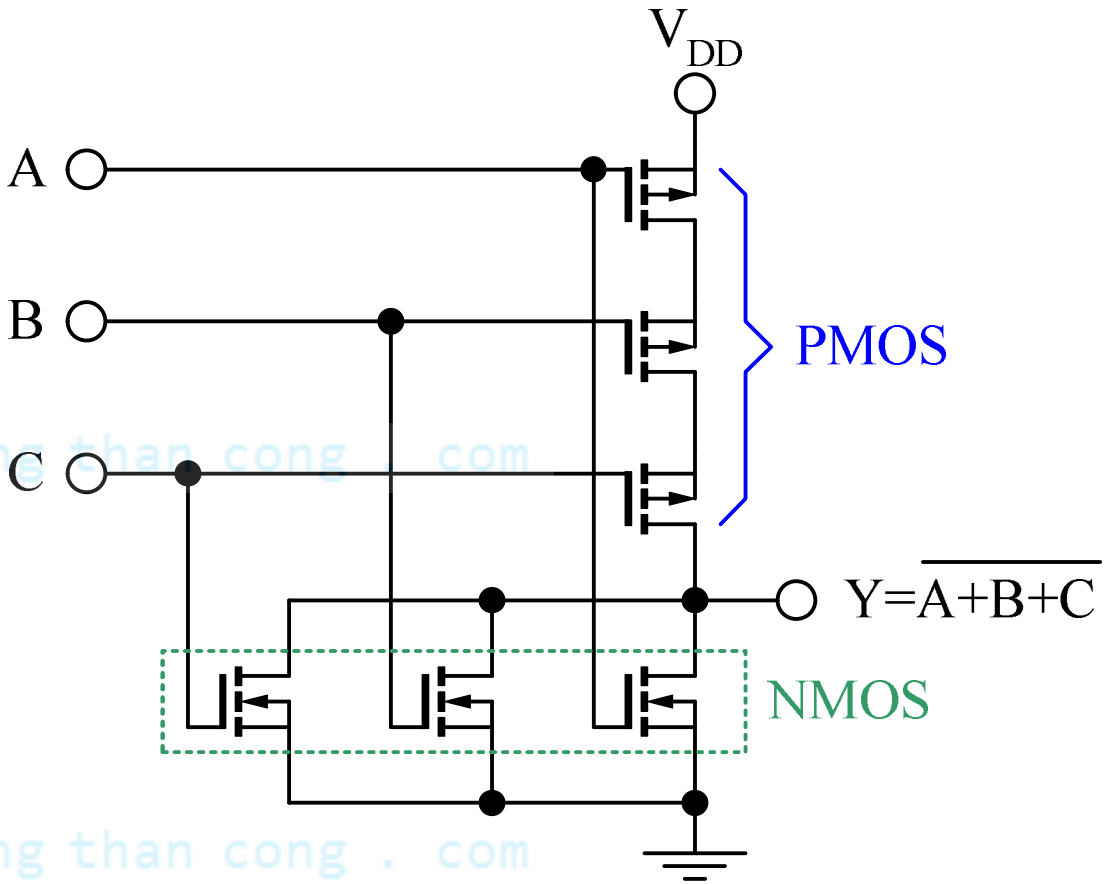
CMOS Inverter and circuit model

- Employs a p-channel, Qp, and an n-channel, Qn MOSFET
  - <u>Vin = Low</u>
    - Qn = off
    - Qp = on
  - <u>Vout = High</u>
  - <u>Vin = High</u>
    - Qn = on
    - Qp = off
  - <u>Vout = Low</u>

CMOS



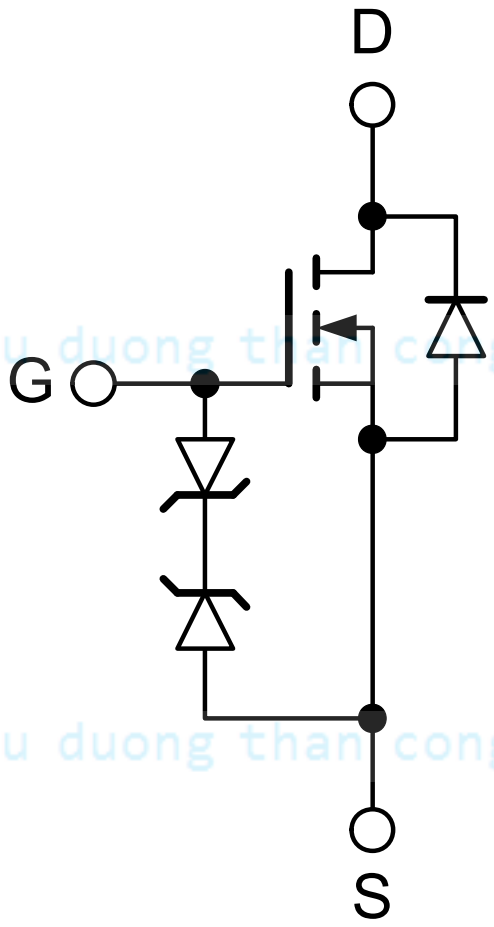
Inverter gate



NOR gate

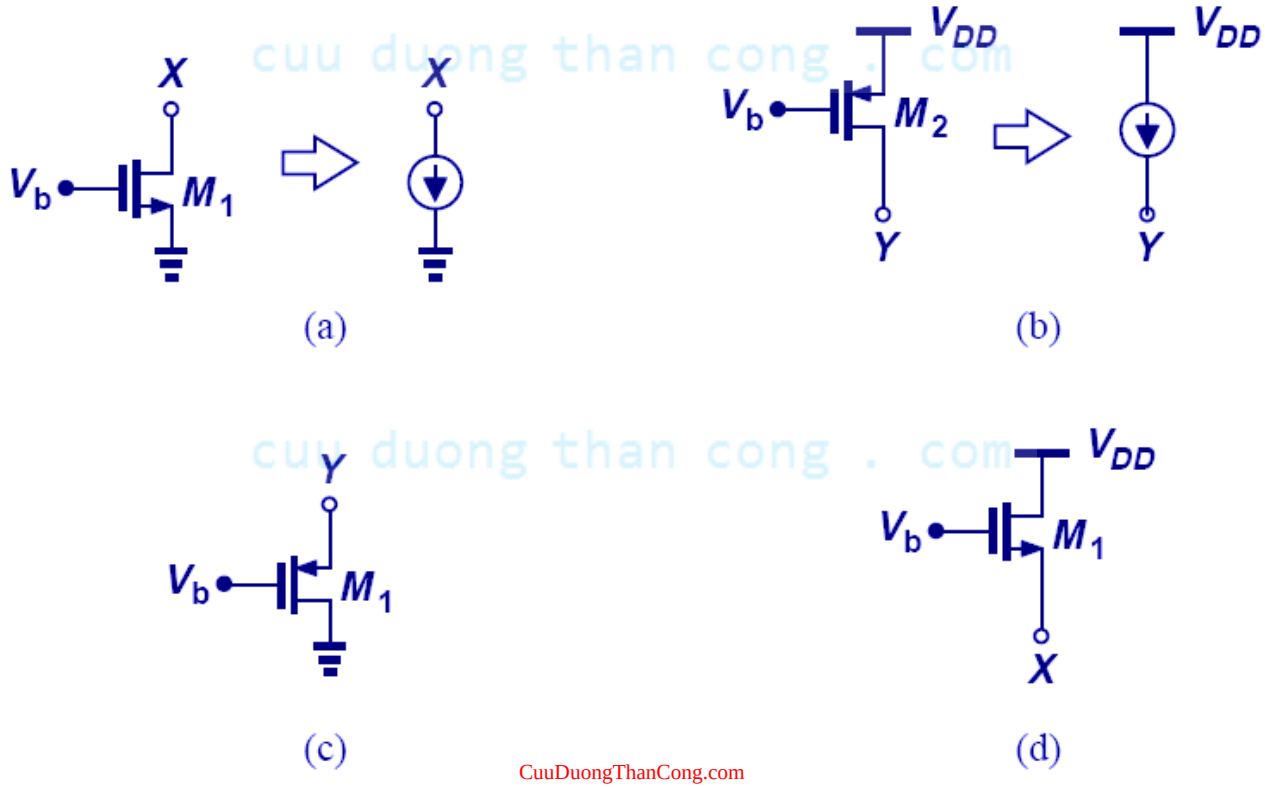
When input voltage is near mid-point ($V_{DD}/2$), the circuit consumes high current.

MOSFET static protection.



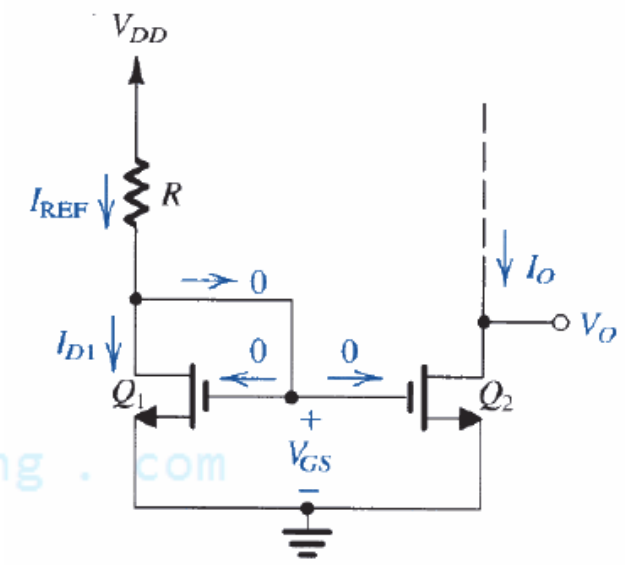
MOSFETs as Current Sources

- A MOSFET behaves as a current source when it is operating in the saturation region.
- An NMOSFET draws current from a point to ground ("sinks current"), whereas a PMOSFET draws current from V_{DD} to a point ("sources current").



Gương dòng điện dùng N-EMOS

Current Mirror is an important building block in IC amplifiers.



As Q_1 must be in saturation mode,

$$I_{D1} = \frac{1}{2}k_n'\left(\frac{W}{L}\right)_1 (V_{GS} - V_t)^2$$

$$I_{D1} = I_{REF} = \frac{V_{DD} - V_{GS}}{R}$$

If Q_2 operates in saturation,

$$I_O = I_{D2} = \frac{1}{2}k_n'\left(\frac{W}{L}\right)_2 (V_{GS} - V_t)^2$$

$$\frac{I_O}{I_{REF}} = \frac{(W/L)_2}{(W/L)_1}$$

If $(W/L)_2=(W/L)_1$, $I_O=I_{REF}$, output mirrors the input.

Note that channel modulation effect is neglected.

Current Mirrors - dc Analysis

- matched devices assumed !
- Gate currents of MOS-Transistors are zero
- =>I_{REF} flows into drain of M1 ($I_{D1} = I_{REF}$)
- M1 operates in saturation ($V_{DS1} = V_{GS1} = V_{GS}$) : $V_{GS} - V_T < V_{DS}$
- Current I_O is qual to I_{D2}
- Circuit Connection forces $V_{GS2} = V_{GS1}$
- Substituting both equation yields:

M1 :

$$I_{REF} = \frac{K_n}{2}(V_{GS1} - V_{TN})^2(1 + \lambda V_{DS1})$$

$$V_{GS1} = V_{TN} + \sqrt{\frac{2I_{REF}}{K_{n1}(1 + \lambda V_{DS1})}}$$

M2 :

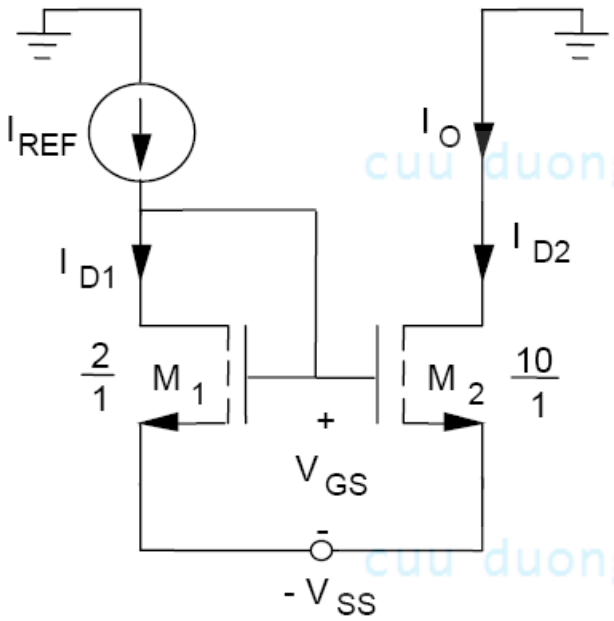
$$I_O = I_{D2} = \frac{K_n}{2}(V_{GS2} - V_{TN})^2(1 + \lambda V_{DS2})$$

$$I_O = I_{REF}\frac{(1 + \lambda V_{DS2})}{(1 + \lambda V_{DS1})} \approx I_{REF}$$

Current Mirrors - Changing the Mirror ratio

Example: MOS current mirror

- New mirror ratio achieved by changing W/L ratios of both transistors



MOS current mirror with unequal (W/L) ratios

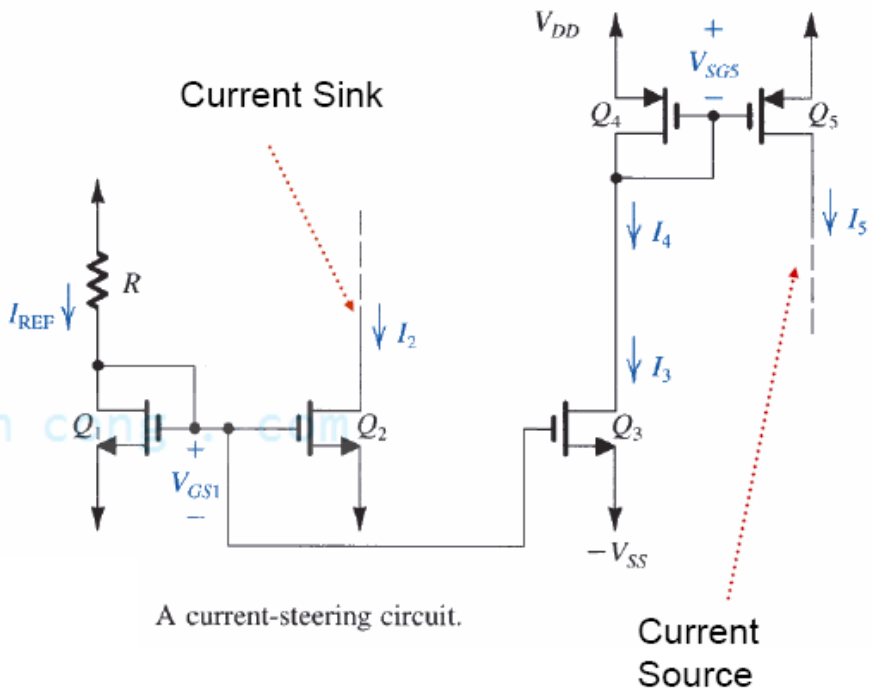
$$K_{n1} = K_n'\left(\frac{W}{L}\right)_1 \; and \; K_{n2} = K_n'\left(\frac{W}{L}\right)_2$$

$$I_O = I_{REF}\frac{K_{n2}(1+\lambda V_{DS2})}{K_{n1}(1+\lambda V_{DS1})} = I_{REF}\frac{\left(\frac{W}{L}\right)_2(1+\lambda V_{DS2})}{\left(\frac{W}{L}\right)_1(1+\lambda V_{DS1})}$$

$$Here: \; I_O = 5I_{REF}$$

Current Steering Circuit

Once a constant current is generated, it can be replicated to provide dc bias currents for the various amplifier stages in an IC.



A current-steering circuit.

Assume Q_2, Q_3 and Q_5 are in active mode.

$$I_2 = I_{REF}\frac{(W/L)_2}{(W/L)_1}$$

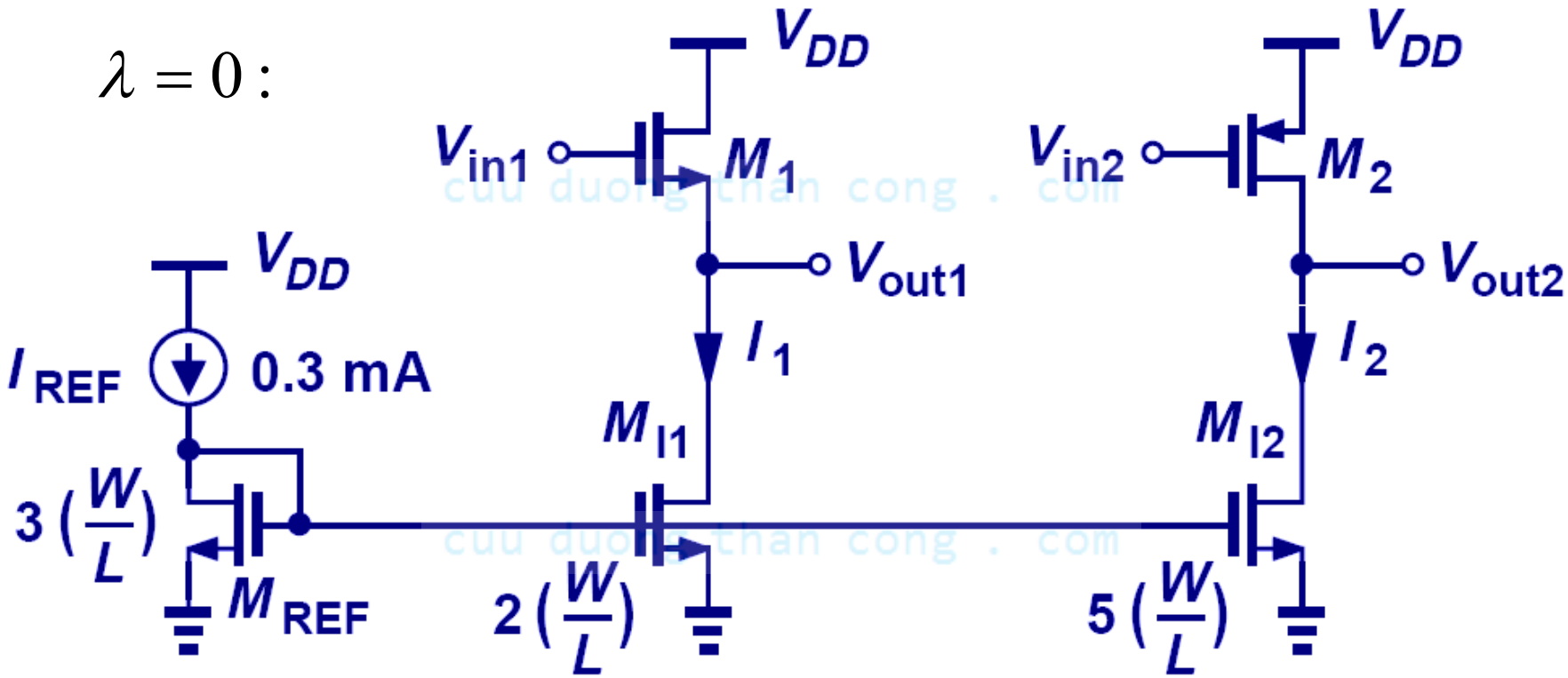
$$I_3 = I_{REF}\frac{(W/L)_3}{(W/L)_1}$$

$$I_5 = I_4\frac{(W/L)_5}{(W/L)_4} \quad \text{where} \quad I_4 = I_3$$

Example: Current Scaling

- MOS current mirrors can be used to scale I_{REF} up or down
  - I_1 = 0.2mA; I_2 = 0.5mA

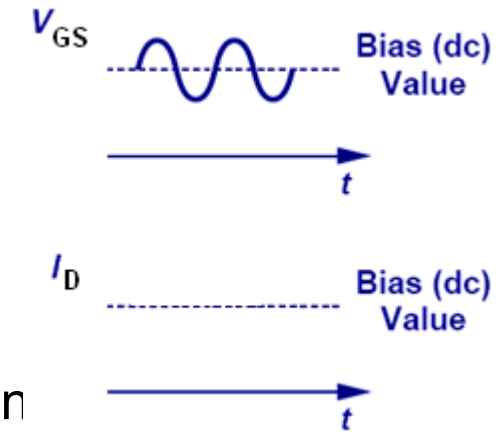
$\lambda = 0:$



Review: MOSFET Amplifier Design

- A MOSFET amplifier circuit should be designed to
  1. ensure that the MOSFET operates in the saturation region,
  2. allow the desired level of DC current to flow, and
  3. couple to a small-signal input source and to an output "load".

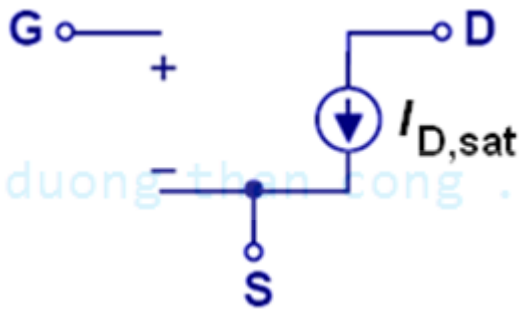
→ Proper "DC biasing" is required!
(DC analysis using large-signal MOSFET model)



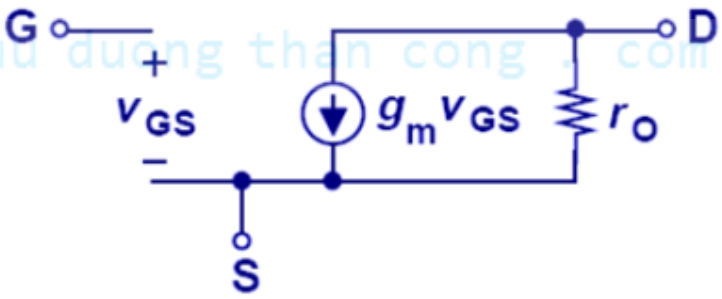
- Key amplifier parameters:
  (AC analysis using small-signal MOSFET model)
  - **Voltage gain** $\boldsymbol{A_v} \equiv v_{out}/v_{in}$
  - **Input resistance** $\boldsymbol{R_{in}} \equiv$ resistance seen between ground (with output terminal floating)
  - **Output resistance** $\boldsymbol{R_{out}} \equiv$ resistance seen between the output node and ground (with input terminal grounded)

MOSFET Models

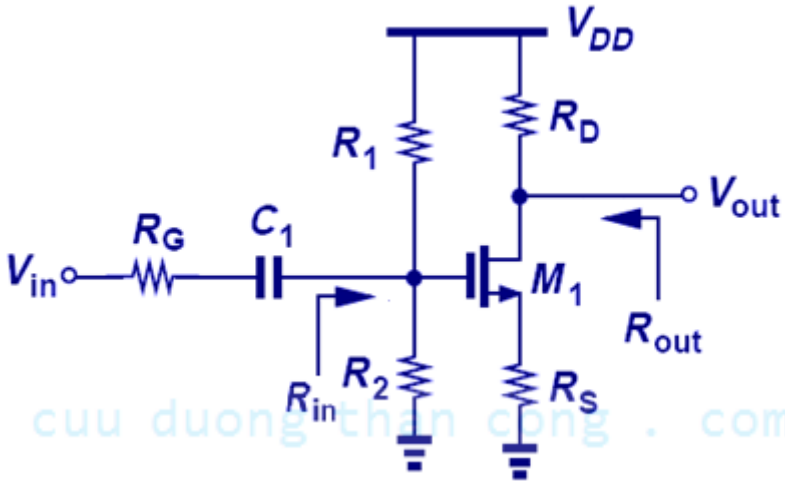
- The large-signal model is used to determine the DC operating point (V_{GS}, V_{DS}, I_D) of the MOSFET.



- The small-signal model is used to determine how the output responds to an input signal.



Common Source Stage



$\lambda = 0$

$$A_v = \frac{R_1 \parallel R_2}{R_G + R_1 \parallel R_2} \cdot \frac{-R_D}{\frac{1}{g_m} + R_S}$$

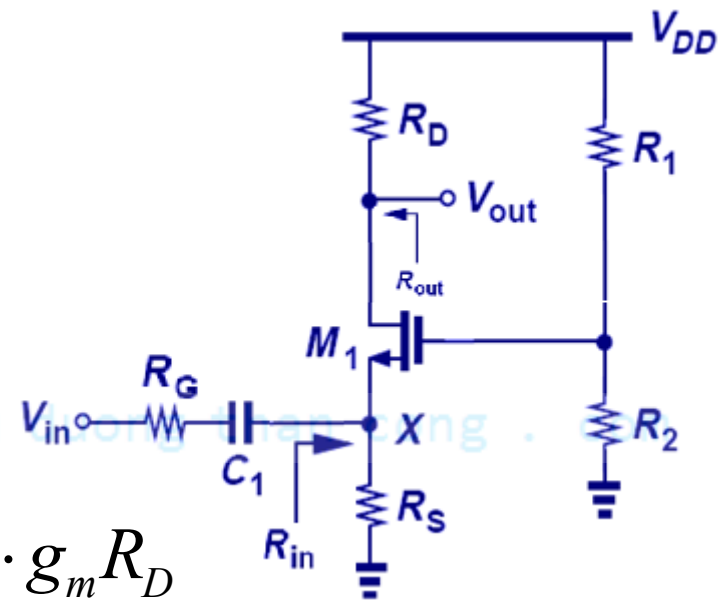
$$R_{in} = R_1 \parallel R_2$$

$$R_{out} = R_D$$

$\lambda \neq 0$

$$R_{out} \cong R_D \left\| \left(r_O + g_m r_O R_S \right) \right.$$

Common Gate Stage



$\lambda = 0$

$$A_v = \frac{R_S \| (1/g_m)}{R_S \| (1/g_m) + R_G} \cdot g_m R_D$$

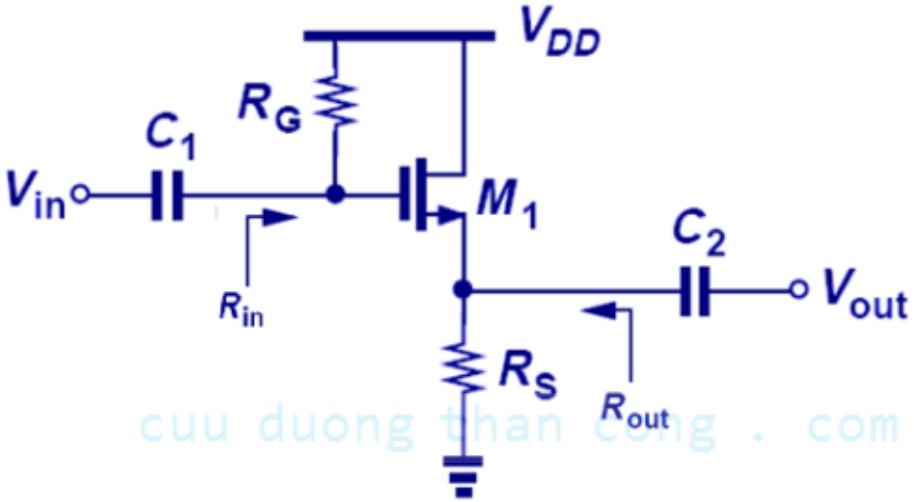
$$R_{in} \approx \frac{1}{g_m} \| R_S$$

$$R_{out} = R_D$$

$\lambda \neq 0$

$$R_{out} \cong R_D \| (r_O + g_m r_O R_S)$$

Source Follower



$\lambda = 0$

$$A_v = \frac{R_S}{\frac{1}{g_m} + R_S}$$

$$R_{in} = R_G$$

$$R_{out} = \frac{1}{g_m} \| R_S$$

$\lambda \neq 0$

$$A_v = \frac{r_O \| R_S}{\frac{1}{g_m} + r_O \| R_S}$$

$$R_{in} = R_G$$

$$R_{out} = \frac{1}{g_m} \| r_o \| R_S$$

Comparison of Amplifier Topologies

Common Source

- **Large $A_v < 0$**
  - degraded by R_S
- **Large R_{in}**
  - determined by biasing circuitry
- **$R_{out} \cong R_D$**
- **r_o decreases A_v & R_{out}**
  but impedance seen looking into the drain can be "boosted" by source degeneration

Common Gate

- **Large $A_v > 0$**
  -degraded by R_S
- **Small R_{in}**
  - decreased by R_S
- **$R_{out} \cong R_D$**
- **r_o decreases A_v & R_{out}**
  but impedance seen looking into the drain can be "boosted" by source degeneration

Source Follower

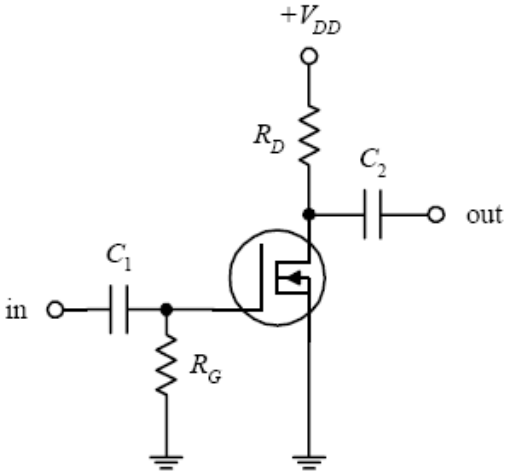
- **$0 < A_v \leq 1$**
- **Large R_{in}**
  - determined by biasing circuitry
- **Small R_{out}**
  - decreased by R_S
- **r_o decreases A_v & R_{out}**

Giới thiệu các ứng dụng của MOSFET

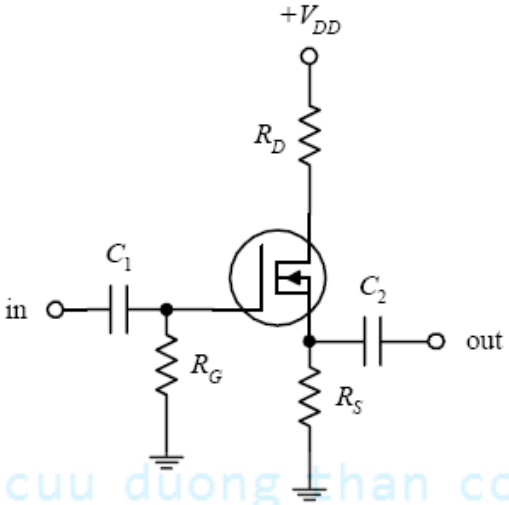
- Mạch KĐ
- Khóa điện tử (analog switch)
- IC: NMOS, PMOS, CMOS, BiCMOS
- . . .

AMPLIFIERS

common-source amplifier
(depletion MOSFET)

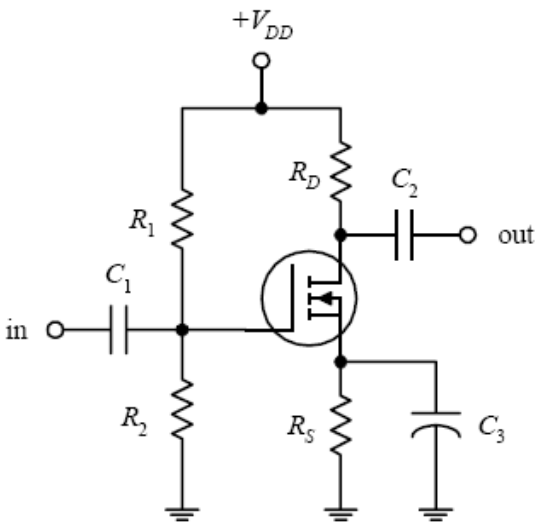


source-follower amplifier
(depletion MOSFET)

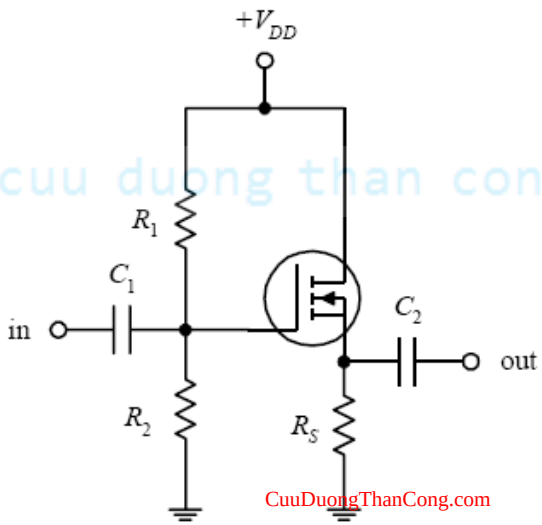


Common-source and source-follower amplifiers can be constructed using both depletion- and enhancement-type MOSFETs. The depletion-type amplifiers are similar to the JFET amplifiers discussed earlier, except that they have higher input impedances. The enhancement-type MOSFET amplifiers essentially perform the same operations as the depletion-type MOSFET amplifiers, but they require a voltage divider (as compared with a single resistor) to set the quiescent gate voltage. Also, the output for the enhancement-type common-source MOSFET amplifier is inverted. The role of the resistors and capacitors within these circuits can be better understood by referring to the amplifier circuits discussed earlier.

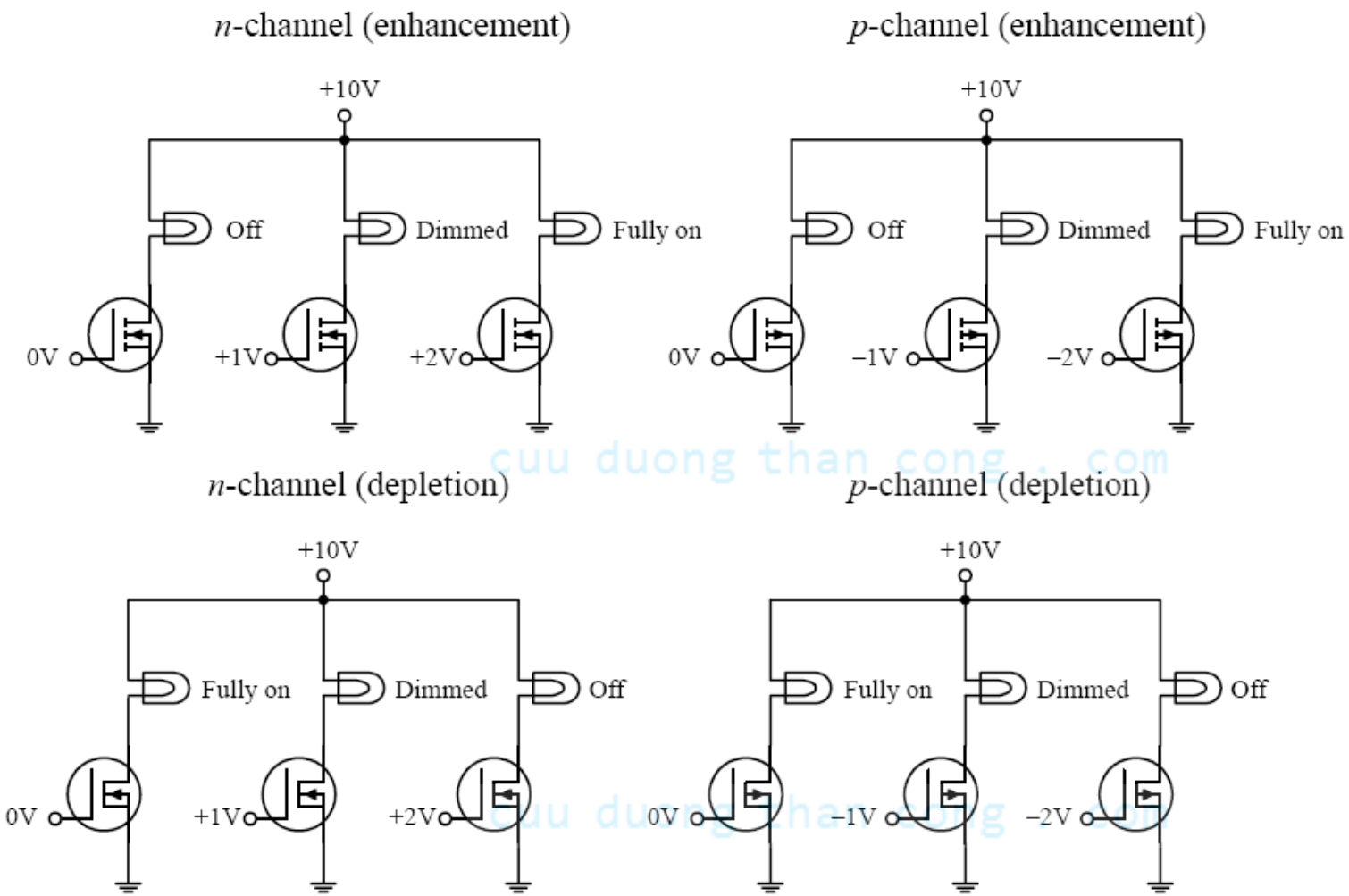
common-source amplifier
(enhancement MOSFET)



source-follower amplifier
(enhancement MOSFET)

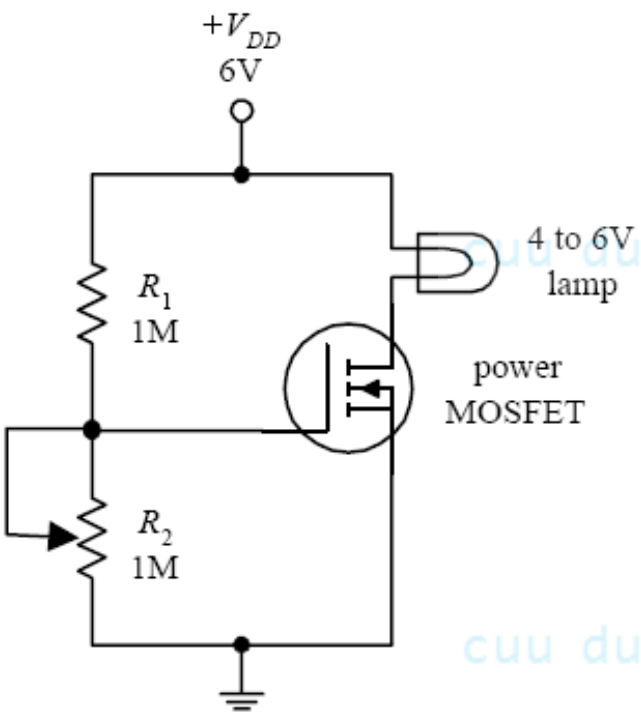


Basic Operation



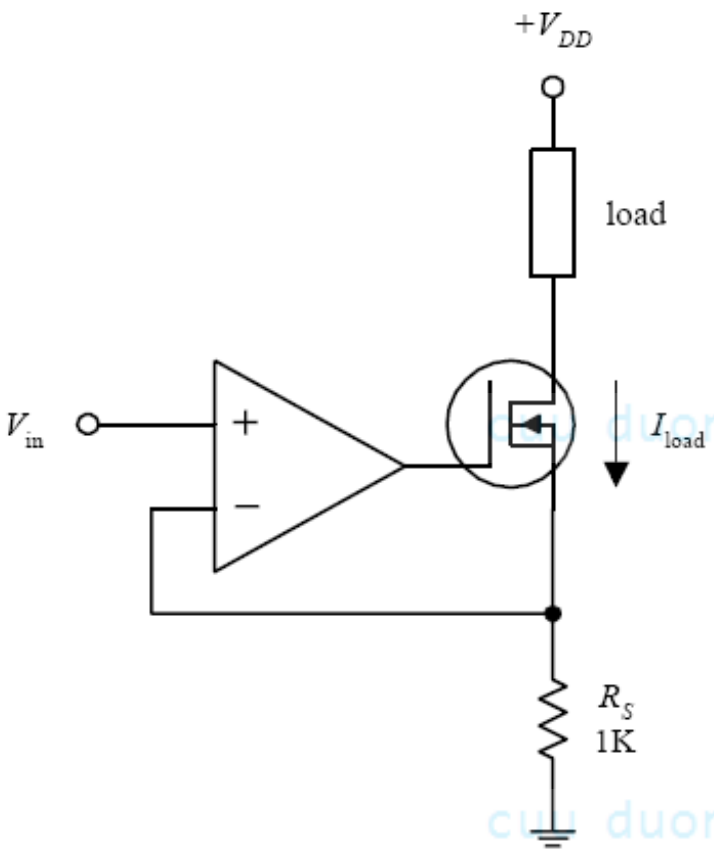
The circuits shown here demonstrate how MOSFETs can be used to control current flow through a light bulb. The desired dimming effects produced by the gate voltages may vary depending on the specific MOSFET you are working with.

LIGHT DIMMER



Here, an *n*-channel enhancement-type power MOSFET is used to control the current flow through a lamp. The voltage-divider resistor R_2 sets the gate voltage, which in turn sets the drain current through the lamp.

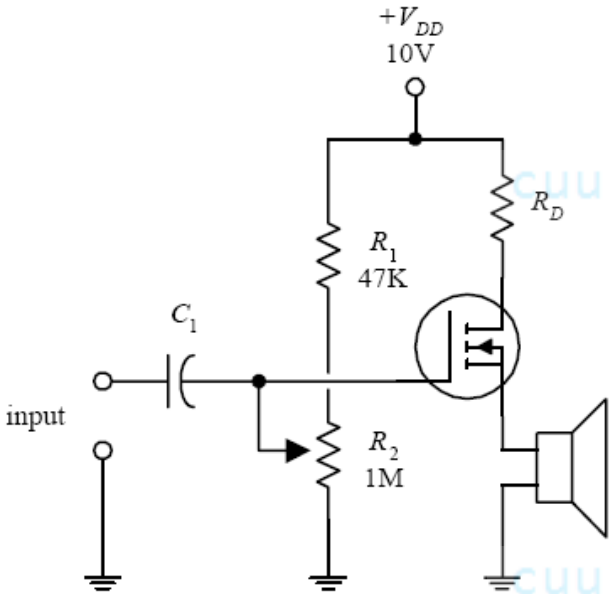
CURRENT SOURCE



In the circuit shown here, an op amp is combined with an *n*-channel depletion-type MOSFET to make a highly reliable current source (less than 1 percent error). The MOSFET passes the load current, while the inverting input of the op amp samples the voltage across R_S and then compares it with the voltage applied to the noninverting input. If the drain current attempts to increase or decrease, the op amp will respond by decreasing or increasing its output, hence altering the MOSFETs gate voltage in the process. This in turn controls the load current. This op amp/MOSFET current source is more reliable than a simple bipolar transistor-driven source. The amount of leakage current is extremely small. The load current for this circuit is determined by applying Ohm's law (and applying the rules for op amps discussed in Chap. 7):

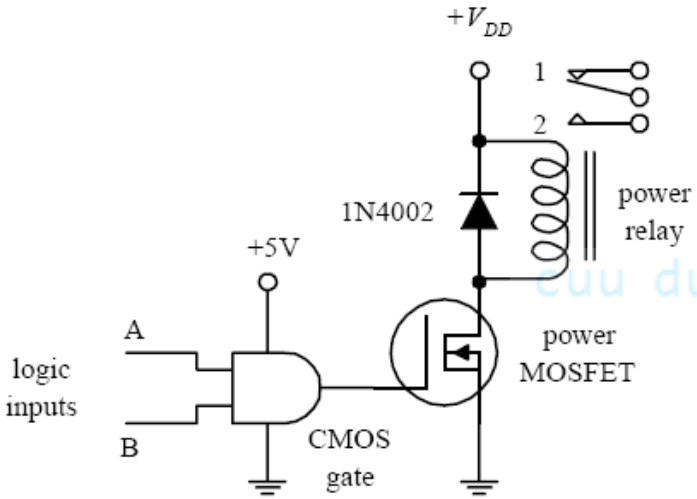
$$I_{load} = V_{in}/R_S$$

AUDIO AMPLIFIER



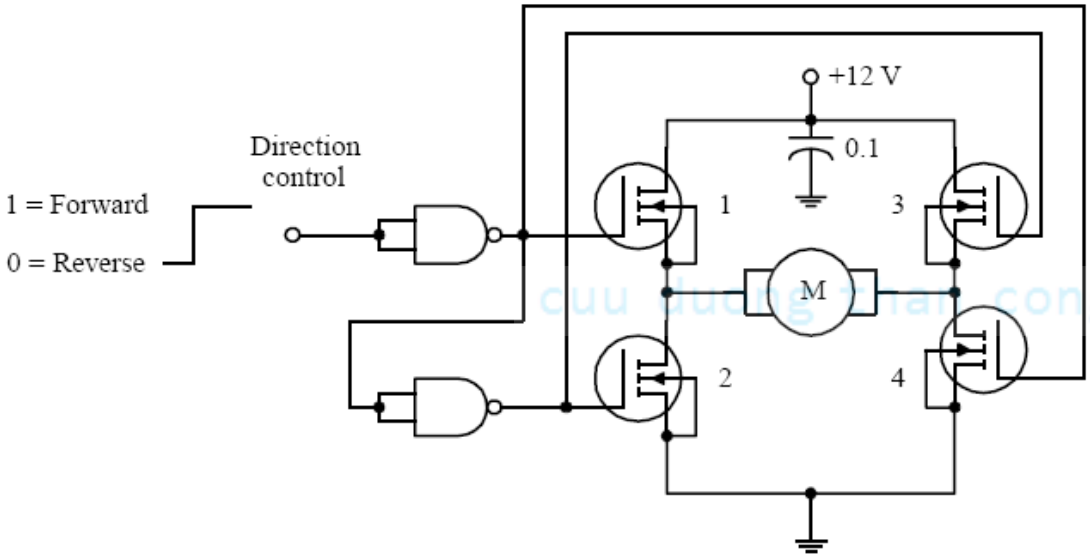
In this circuit, an *n*-channel enhancement-type MOSFET is used to amply an audio signal generated by a high-impedance microphone and then uses the amplified signal to drive a speaker. C_1 acts as an ac coupling capacitor, and the R_2 voltage divider resistor acts to control the gain (the volume).

RELAY DRIVER (DIGITAL-TO-ANALOG CONVERSION)



The circuit shown here uses an *n*-channel depletion-type MOSFET as an interface between a logic circuit and an analog circuit. In this example, an AND gate is used to drive a MOSFET into conduction, which in turn activates the relay. If inputs *A* and *B* are both high, the relay is switched to position 2. Any other combination (high/low, low/high, low/low) will put the relay into position 1. The MOSFET is a good choice to use as a digital-to-analog interface; its extremely high input resistance and low input current make it a good choice for powering high-voltage or high-current analog circuits without worrying about drawing current from the driving logic.

DIRECTION CONTROL OF A DC MOTOR



Logic input signals applied to this circuit act to control the direction of rotation of a dc motor. When the input is set high, the upper NAND gate outputs a low in response, turning transistors 1 and 4 on. At the same time, the high output from this gate is sent to the input of the lower NAND gate. The lower gate responses by outputting a low, thereby turning off transistors 2 and 3. Now, the only direction in which current can flow through the circuit is from the power supply through transistor 1, through the motor, and through transistor 4 to ground. This in turn causes the motor to turn in one direction. However, if you now apply a low to the input, transistors 2 and 3 turn on, while transistors 4 and 1 remain off. This causes current to flow through the motor in the opposite direction, thereby reversing the motor's direction of rotation.

CMOS inverter for linear operation

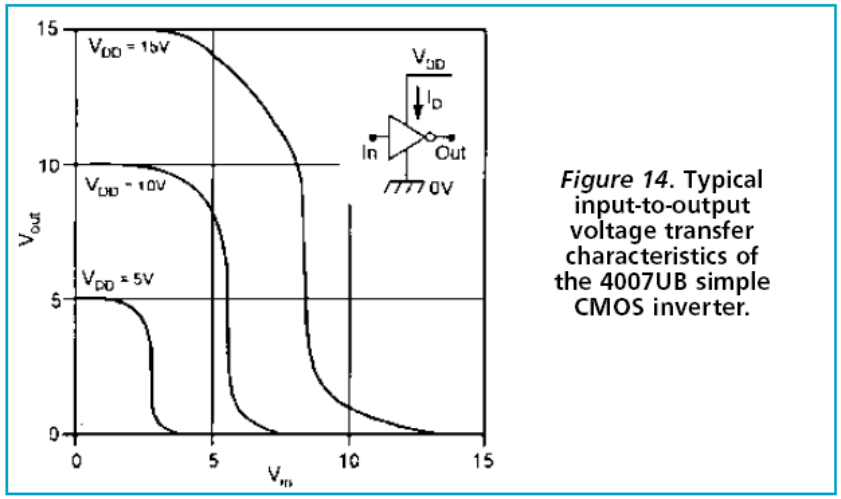


Figure 14. Typical input-to-output voltage transfer characteristics of the 4007UB simple CMOS inverter.

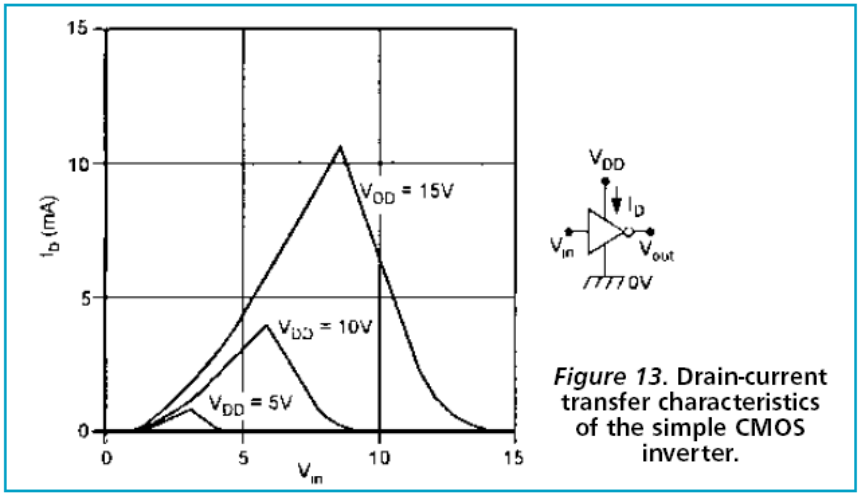


Figure 13. Drain-current transfer characteristics of the simple CMOS inverter.

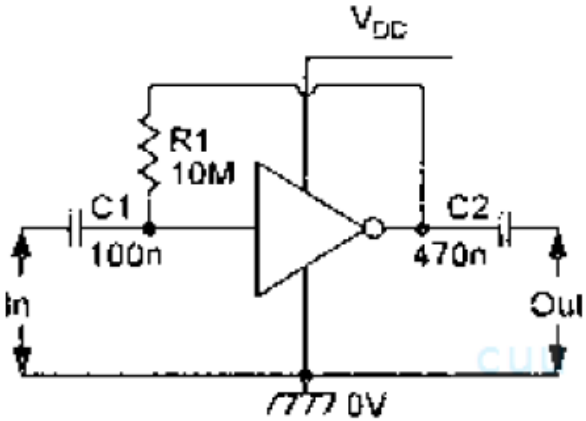


Figure 15. Method of biasing the simple CMOS inverter for linear operation.

Figure 16. Typical A_V and frequency characteristics of the linear-mode basic CMOS amplifier.

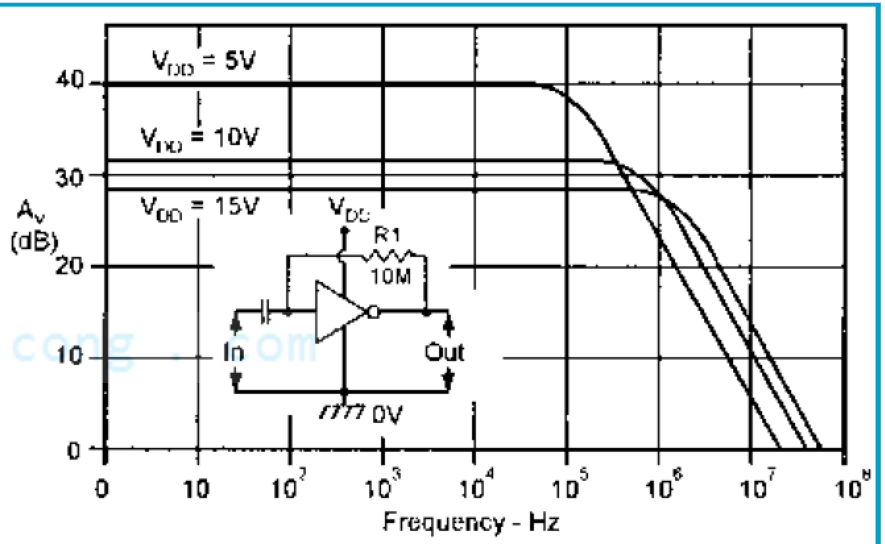
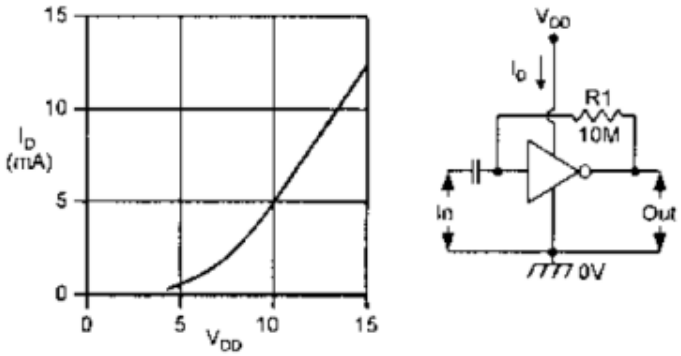
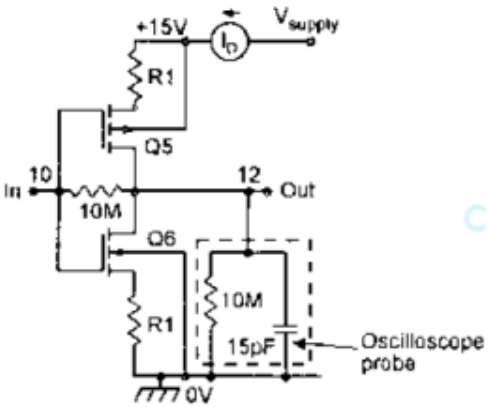


Figure 17. Typical I_D/V_{DD} characteristics of the linear-mode CMOS amplifier.





R1	I_D	A_V (V_{out}/V_{in})	Upper 3dB Bandwidth
0	12.5mA	20	2.7MHz
100R	8.2mA	20	1.5MHz
560R	3.9mA	25	300kHz
1k0	2.5mA	30	150kHz
5k6	600µA	40	25kHz
10k	370µA	40	15kHz
100k	40µA	30	2kHz
1M0	4µA	10	1kHz

Figure 18. Micropower 4007UB CMOS linear amplifier, showing method of reducing I_D, with performance details.

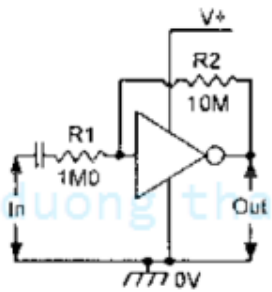


Figure 19. Linear CMOS amplifier wired as x10 inverting amplifier.

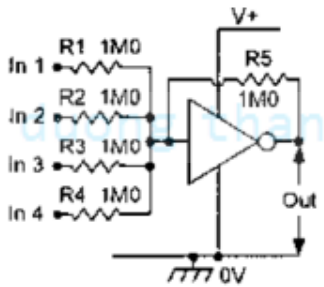
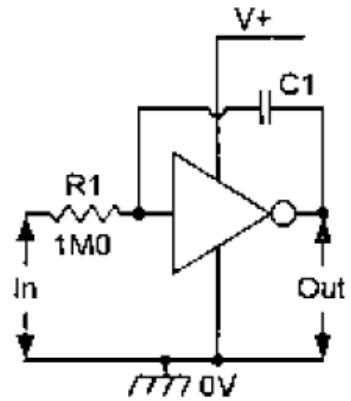


Figure 20. Linear CMOS amplifier wired as unity-gain four-input audio mixer.

Figure 21. Linear CMOS amplifier wired as an integrator.



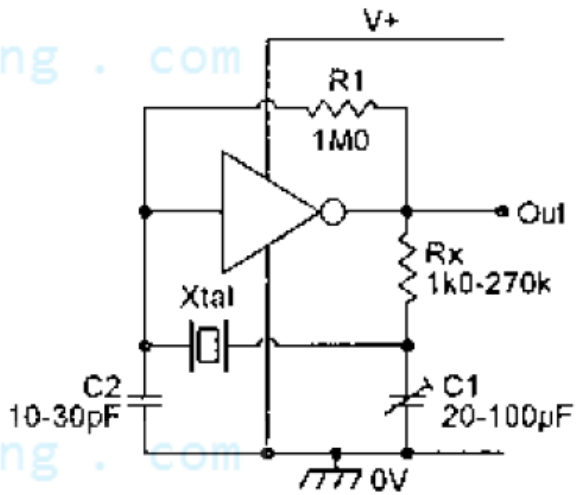


Figure 22. Linear CMOS amplifier wired as a crystal oscillator.

The circuit has four input terminals, and the voltage gain between each input and the output is fixed at

enabling the circuit to oscillate. If