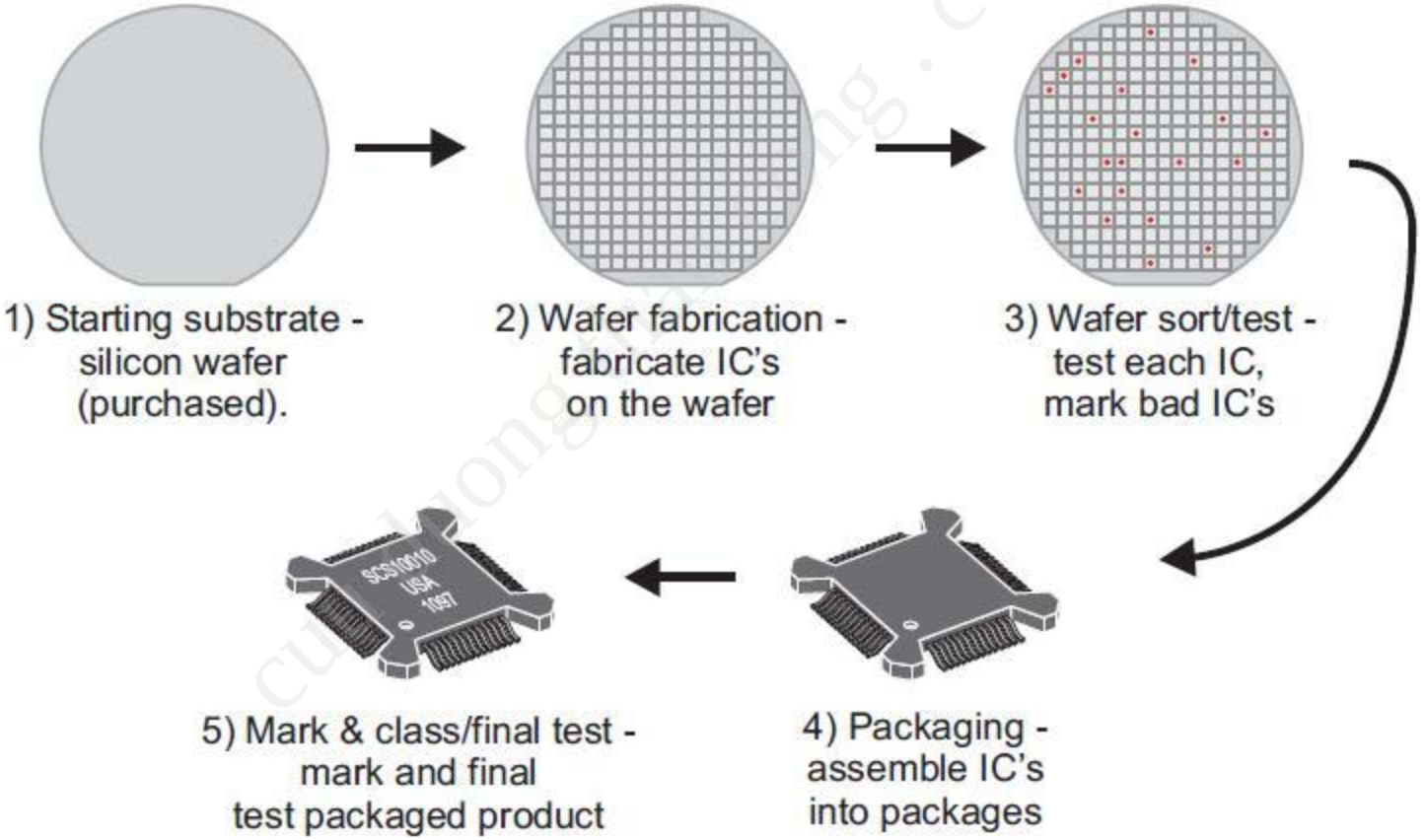
ĐẠI HỌC QUỐC GIA TP.HỒ CHÍ MINH
TRƯỜNG ĐẠI HỌC BÁCH KHOA
KHOA ĐIỆN-ĐIỆN TỬ
BỘ MÔN KỸ THUẬT ĐIỆN TỬ

ASIC CHIP AND IP CORE DESIGN

Chapter 2: IC Fabrication

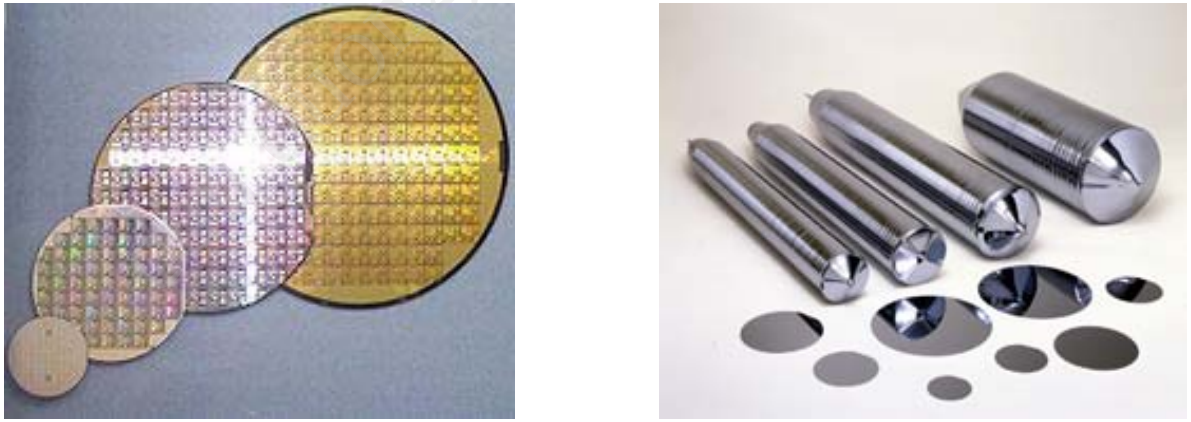
2.1 IC Fabrication Process
2.2 Transistors & Logic Gates
2.3 Layout and Design Tools

2.1 IC Fabrication Process



Wafer

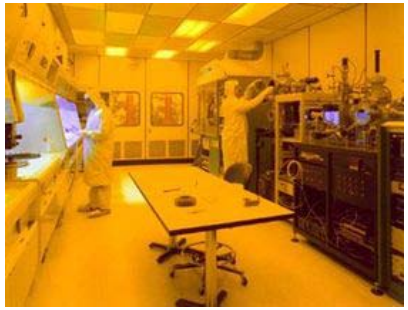
- Wafer
  - is a thin slice of highly pure semiconductor material, such as a silicon crystal
  - serves as the substrate for microelectronic devices
- Standard wafer sizes
  - 1-inch, 2-inch thickness 275 µm, 3-inch thickness 375 µm, 4-inch thickness 525 µm, 5 inch thickness 625 µm, 6 inch thickness 675 µm, 8 inch



Different wafer sizes

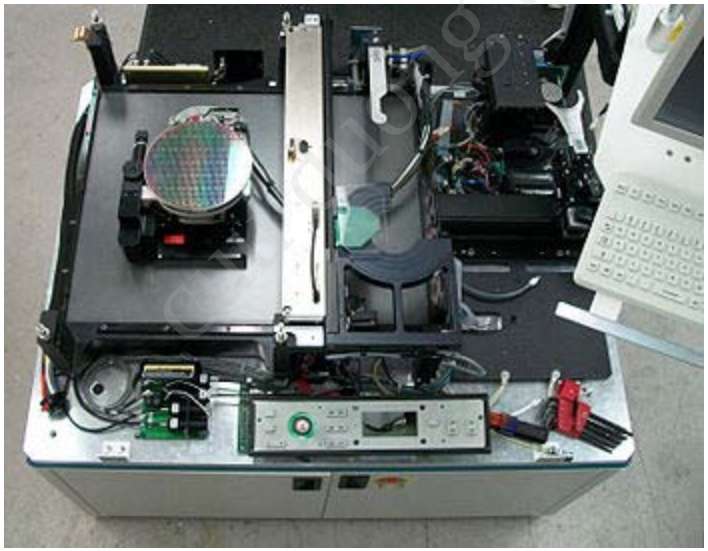
IC Fabrication

- **Deposition:** grows, coats a material onto the wafer.
  - Available technologies: physical vapor deposition (PVD), chemical vapor deposition (CVD), electrochemical deposition (ECD), …
- **Removal processes** (etching processes): remove material from the wafer
  - Technology: Chemical-mechanical planarization (CMP)
- **Patterning** (lithography): shape or alter the existing shape of the deposited materials
  - Technology: the wafer is coated with a chemical called a photoresist. The exposed regions are washed away by a developer solution. After etching, the remaining photoresist is removed by plasma ashing.
- **Doping processes:** doping transistor sources and drains originally by diffusion furnaces and later by ion implantation.
  - Technology: rapid thermal anneal (RTA), UV processing (UVP).



Wafer Test

- All individual ICs are tested for functional defects by applying special test patterns to them.
- The wafer testing is performed by a piece of test equipment called a **wafer prober.**

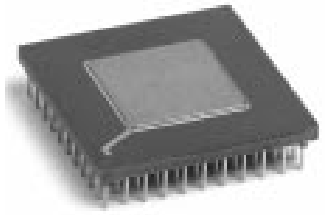


8-inch semiconductor wafer prober

Packaging

- The die, integrated circuit, is encased.
  - prevents physical damage and corrosion
  - supports the electrical contacts
- Package standard:
  - DIP: dual in-line package
  - PGA: pin grid array
  - LCC: leadless chip carrier

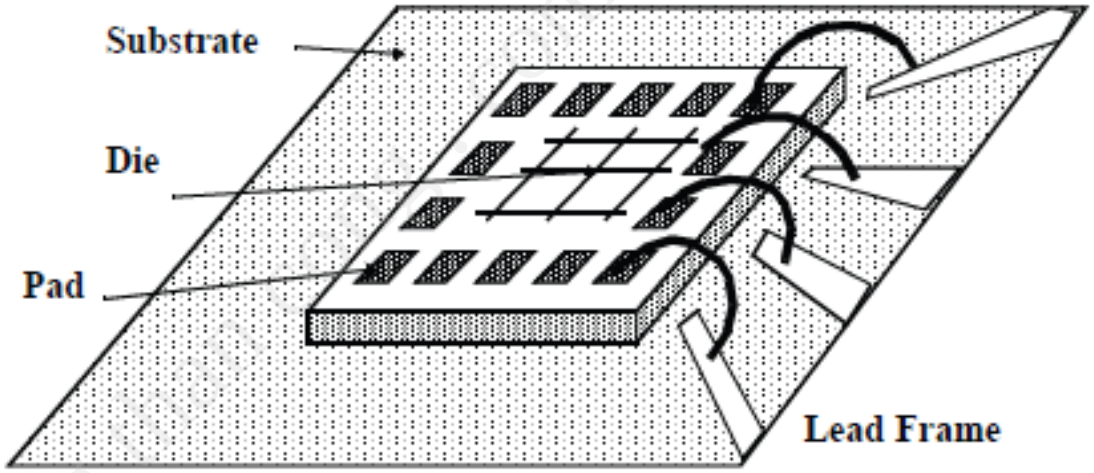
DIP

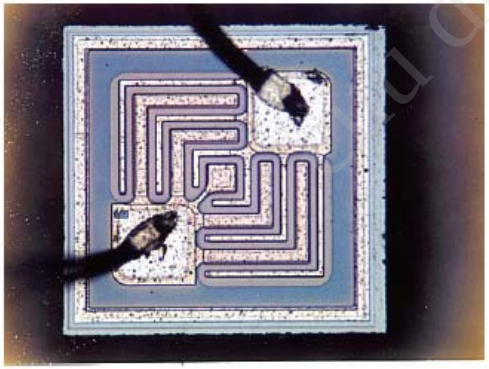


PGA

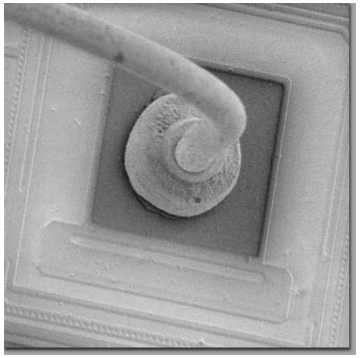
Package Connections

- Wire bonding
  - die attached
  - gold or aluminum wires
  - one at a time





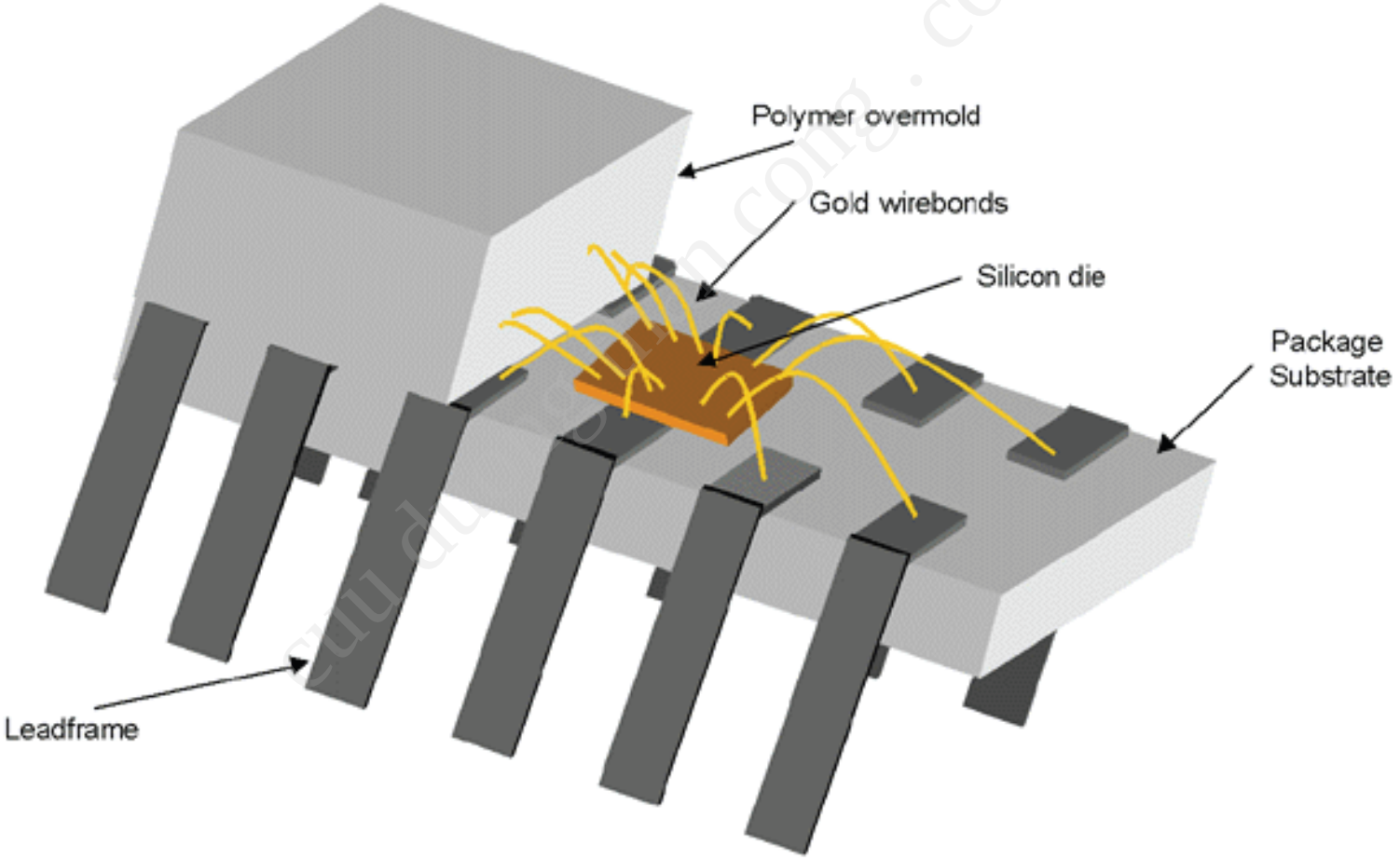
Optical microscope view of bond wires for a two pad package



Gold wire bond on aluminum die pad

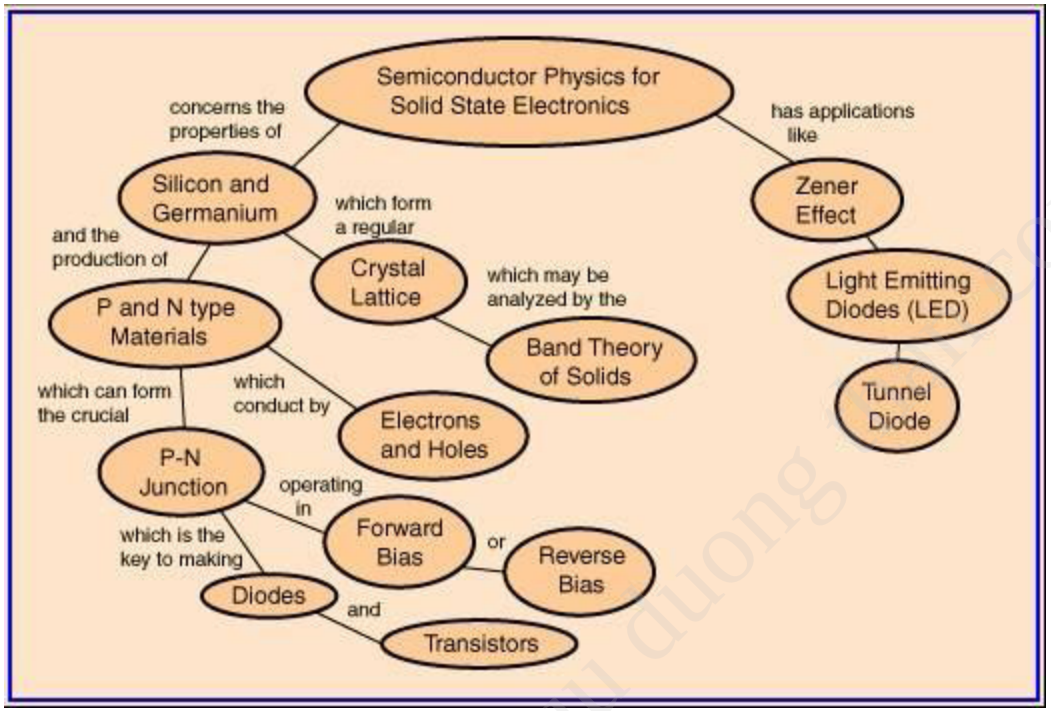
Package Types

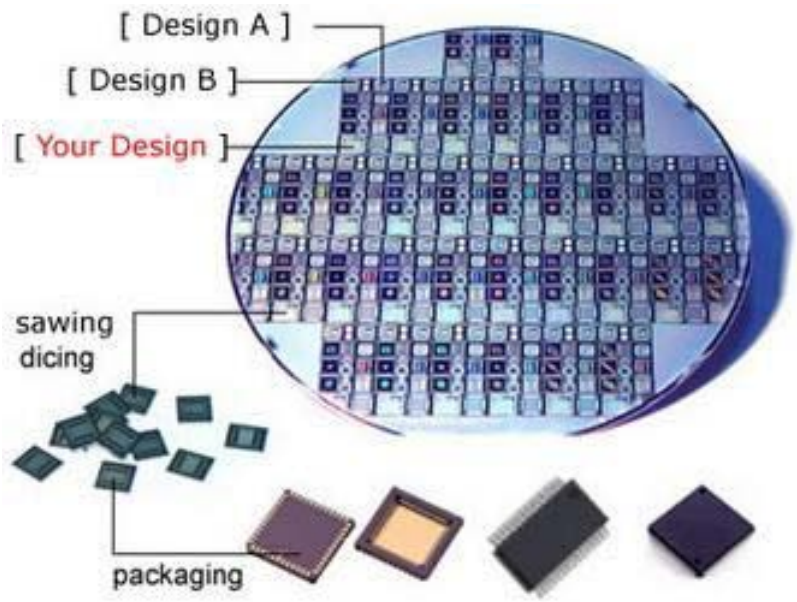
- DIP – Dual In-Line Package



Semiconductor Industry

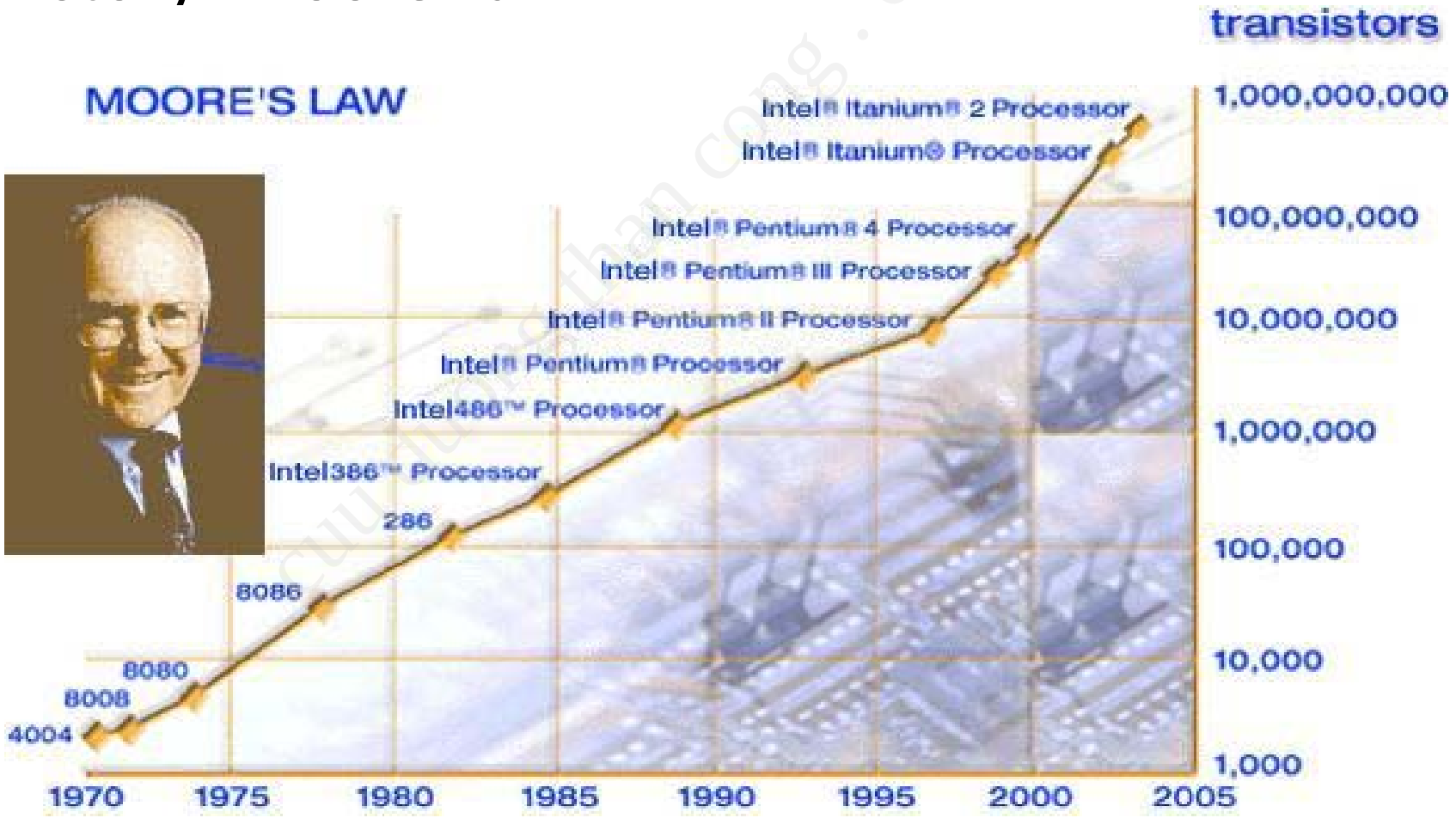
- Hardware design flow





Semiconductor Industry

- History: Moore Law



Semiconductor Industry

Companies designing and/or manufacturing “semiconductor products”

1. Silicon wafer producers
2. Foundry semiconductor companies (fab)
3. Assembly and Test semiconductor companies
4. Fabless semiconductor companies (fabless)
5. Equipment semiconductor companies

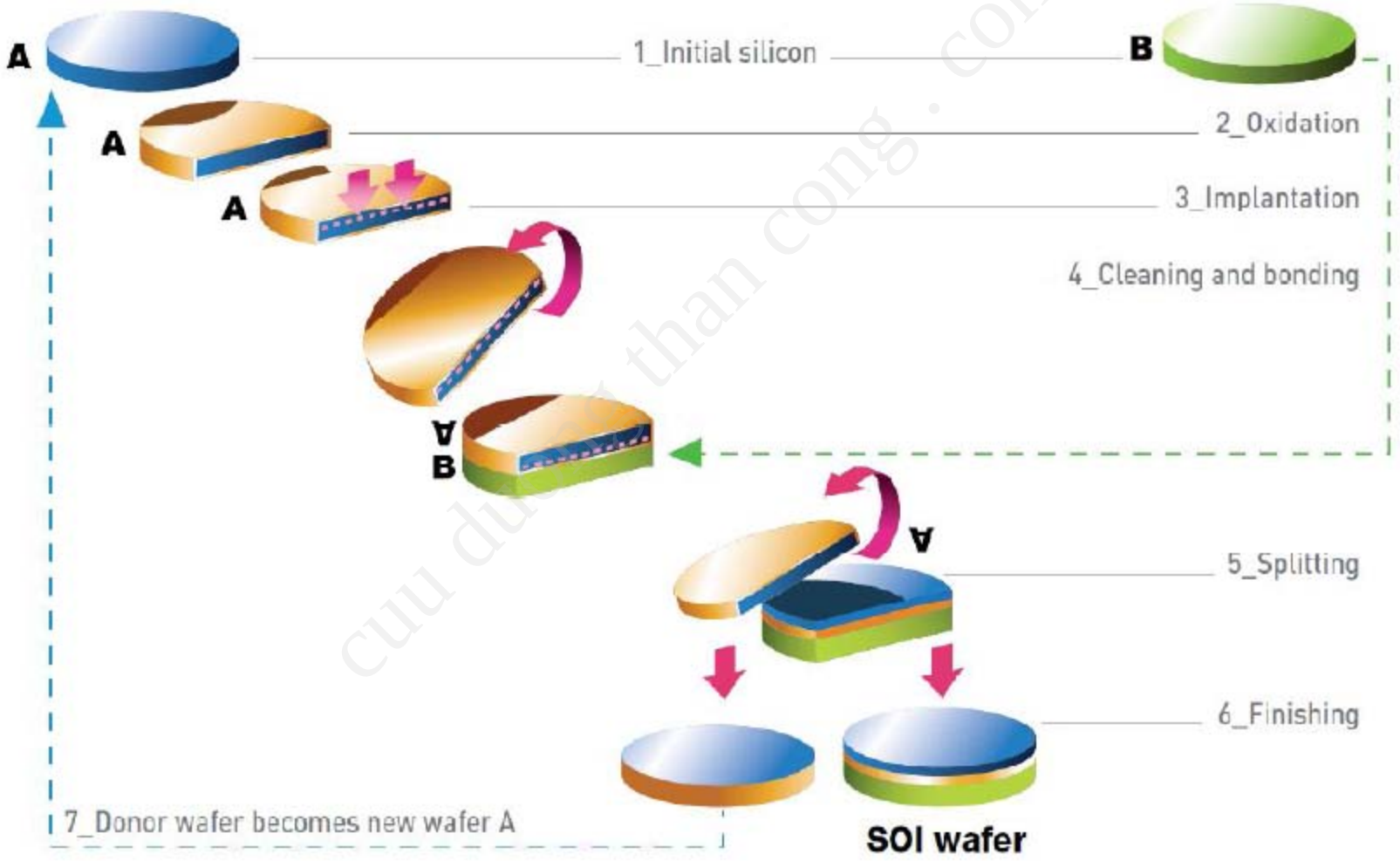
Semiconductor Industry

A list of major producers of wafers (made of high purity Silicon, mono- or polycrystalline):

- 1. Shin-Etsu Handotai Chemical Company (Shin-Etsu Chemical)
- 2. Sumco (Mitsubishi/Sumitomo Sumco Silicon) (Sumitomo Metal Industries)
- 3. SiltronicAG
- 4. MEMC Electronic Materials
- 5. Zhejiang DC Chemical
- 6. LDK Solar
- 7. Renewable Energy Corporation
- 8. Renesola
- 9. M. Setek
- 10. Covalent
- 11. Tokuyama
- 12. Topsil
- 13. SOItech

Semiconductor Industry

- Semiconductor Industry: Silicon wafer producers



Semiconductor Industry

- Semiconductor Industry: Semiconductor sales

Rank 2009	Rank 2008	Company	Country of origin	Revenue (million $ USD)	2009/2008 changes	Market share
11	10	Infineon Technologies	Germany	4 456	-25.2%	1.9%
12	11	NEC Semiconductors	Japan	4 384	-24.8%	1.9%
13	16	Micron Technology	USA	4 293	-3.2%	1.9%
14	14	Broadcom	USA	4 278	-7.9%	1.9%
15	19	Elpida Memory	Japan	3 948	+9.7%	1.7%
16	24	MediaTek	Taiwan	3 551	+22.6%	1.5%
17	13	Freescale Semiconductor	USA	3 402	-31.5%	1.5%
18	15	Panasonic Corporation	Japan	3 243	-27.5%	1.4%
19	17	NXP	Netherlands	3 240	-20.1%	1.4%
20	18	Sharp Electronics	Japan	2 977	-17.5%	1.3%
21	20	NVIDIA	USA	2 826	-12.8%	1.2%
22	25	Rohm	Japan	2 586	-22.8%	1.1%
23	23	Fujitsu Microelectronics	Japan	2 574	-13.6%	1.1%
24	22	Marvell Technology Group	USA	2 572	-15.9%	1.1%
25	26	IBM Microelectronics	USA	2 253	-8.9%	1.0%
Top 25				**156 472**	**-10.39%**	**68.1%**
All Other companies				**73 445**	**-14.2%**	**31.9%**
TOTAL				**229 917**	**-11.7%**	**100.0%**

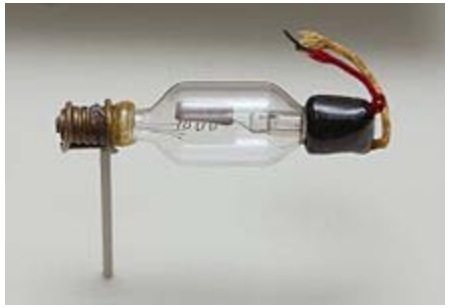
Semiconductor Industry

- Semiconductor Industry: Semiconductor Sales

Rank 2009	Rank 2008	Company	Country of origin	Revenue (million $ USD)	2009/2008 changes	Market share
1	1	Intel Corporation	USA	32 410	-4.0%	14.1%
2	2	Samsung Electronics	South Korea	17 496	+3.5%	7.6%
3	3	Toshiba Semiconductors	Japan	10 319	-6.9%	4.5%
4	4	Texas Instruments	USA	9 617	-12.6%	4.2%
5	5	STMicroelectronics	France Italy	8 510	-17.6%	3.7%
6	8	Qualcomm	USA	6 409	-1.1%	2.8%
7	9	Hynix	South Korea	6 246	+3.7%	2.7%
8	12	AMD	USA	5 207	-4.6%	2.3%
9	6	Renesas Technology	Japan	5 153	-26.6%	2.2%
10	7	Sony	Japan	4 468	-35.7%	1.9%

2.2 Transistors & Logic Gates

- The **thermionic triode**, a vacuum tube invented in 1907, propelled the electronics age forward, enabling amplified radio technology and long-distance telephony.
- The **transistor**, "transfer resistor", was first invented by Bardeen, Brattain, and Shockley at at AT&T's Bell Labs in the United States



Tridiode

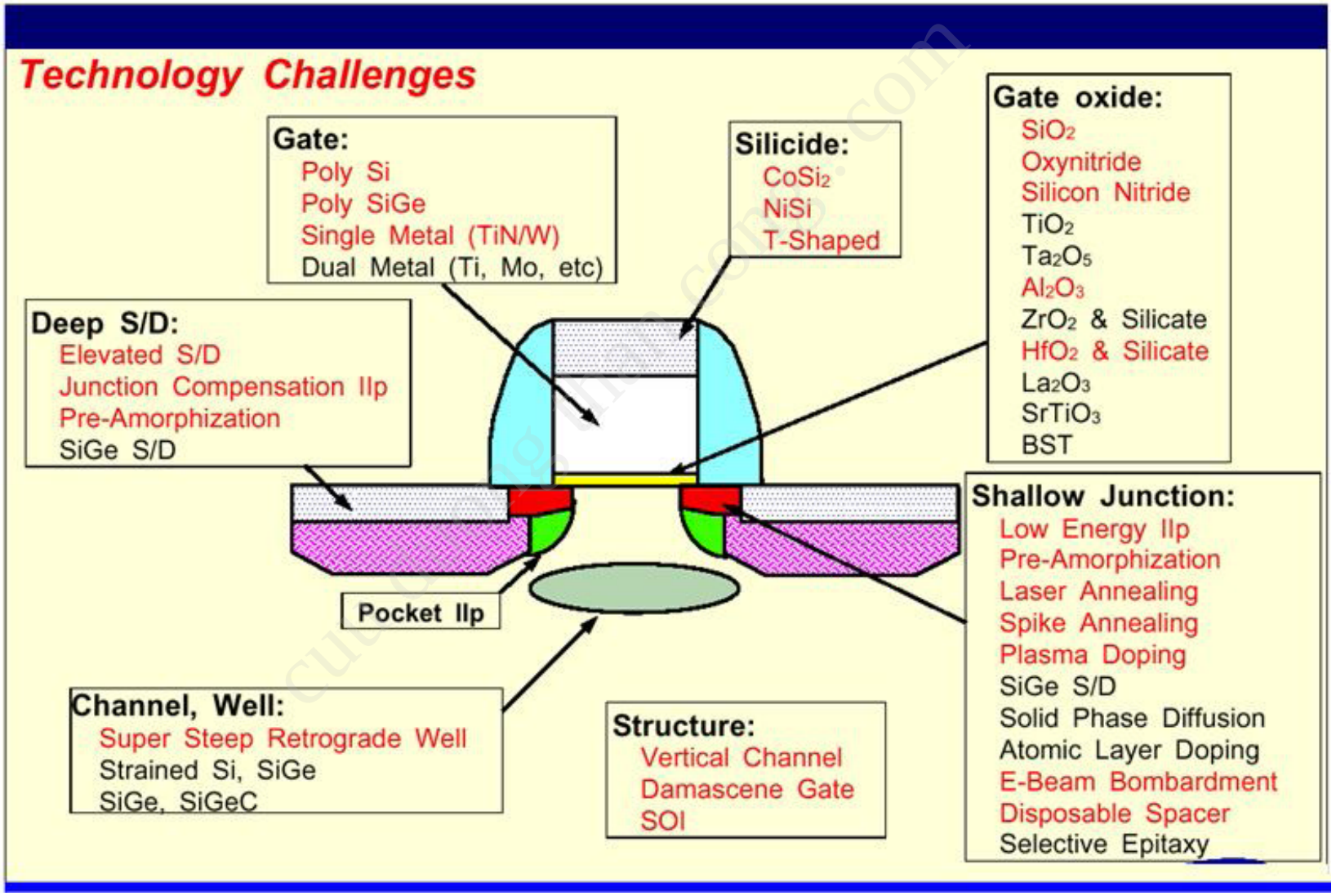
John Bardeen, William Shockley and Walter Brattain at Bell Labs, 1948

The first transistor, 1947

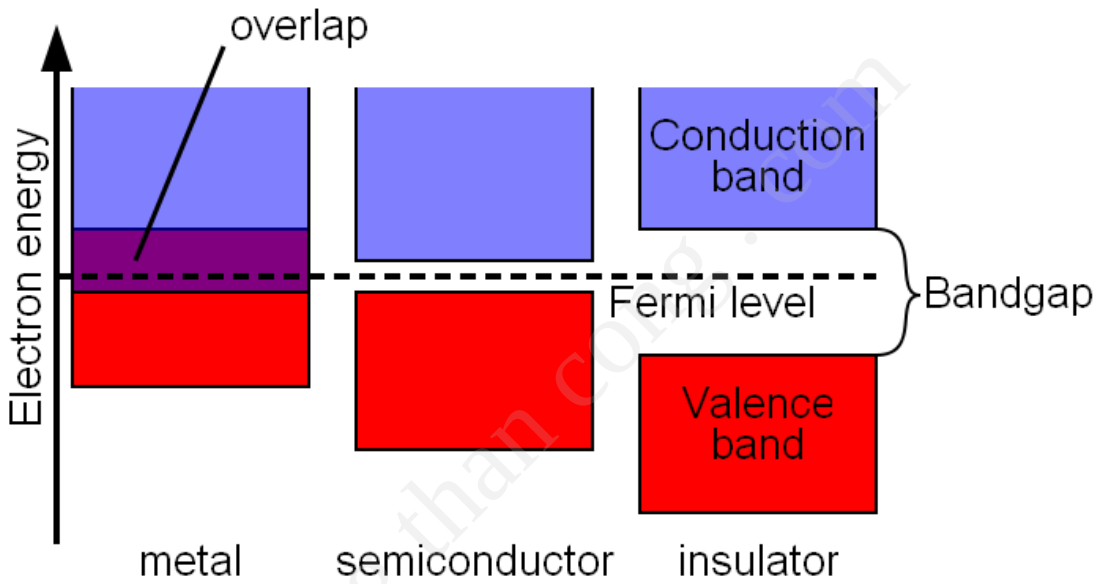
Now

Source: http://en.wikipedia.org/wiki/Transistor

Transistors



Semiconductor material



- Energy band diagram

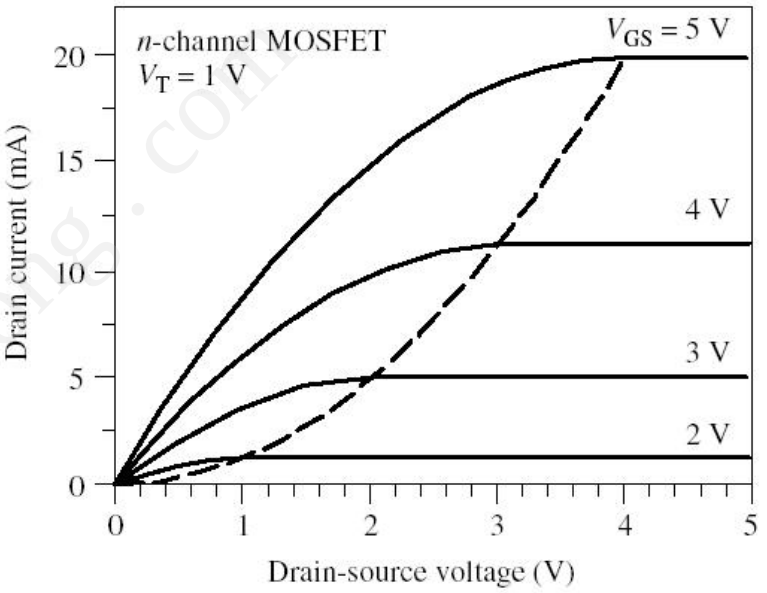
Group IV materials
-Diamond (C)
-Silicon (Si)
-Germanium (Ge)
Group IV compounds
-Silicon carbide (SiC)
-Silicon germanide (SiGe)

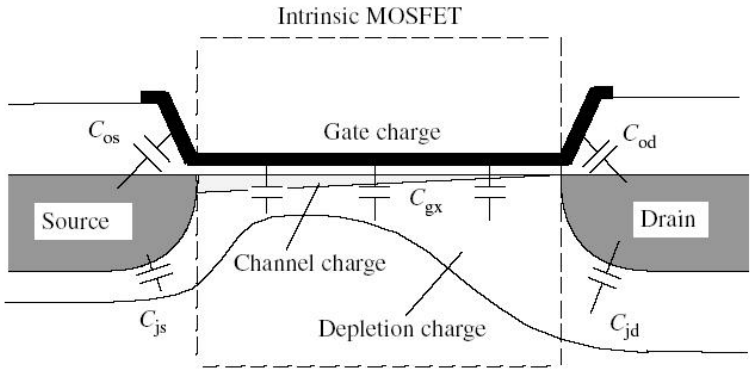
Organic semiconductors
-Carbon nanotube

III-V compounds
-Gallium arsenide (GaAs)
-Gallium nitride (GaN)
-Gallium phosphide (GaP)

Transistors

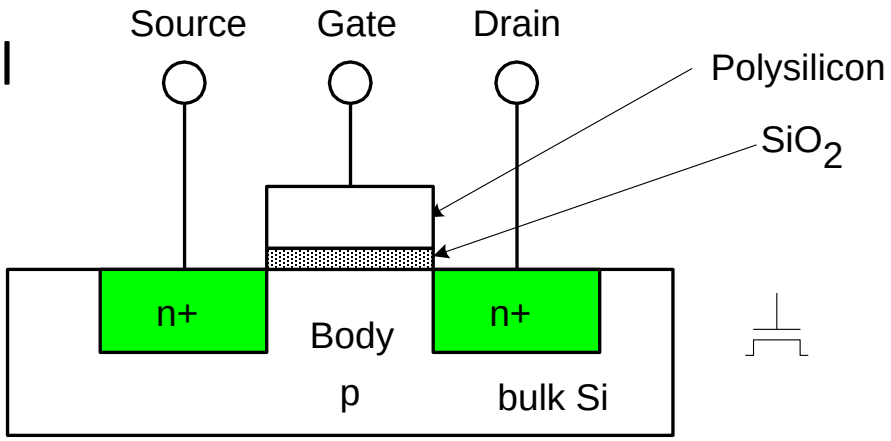
- The MOSFET can be categorized into three separate modes when in operation.
  - Sub-threshold or cut-off mode: VGS < Vt, where Vt is the threshold voltage
  - Linear mode: when VGS > Vt and VDS < VGS − Vt. Essentially, the MOSFET operates similar to a resistor in this mode with a linear relation between voltage and current.
  - Saturation mode: occurs when VGS > Vt and VDS > VGS − Vt. In this mode the switch is on and conducting, however since drain voltage is higher than the gate voltage
- Pinch-off occurs when the MOSFET stops operating in the linear region and saturation occurs.
- In digital circuits, MOSFETS are only operated in the linear mode, while the saturation region is reserved for analogue circuits.





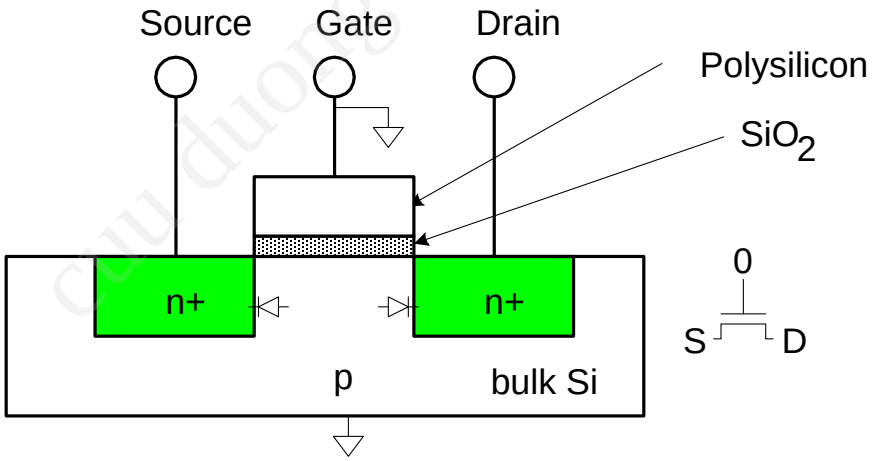
nMOS Transistor

- Four terminals: gate, source, drain, body
- Gate – oxide – body stack looks like a capacitor
  - Gate and body are conductors
  - SiO_2 (oxide) is a very good insulator
  - Called metal – oxide – semiconductor (MOS) capacitor
  - Even though gate is no longer made of metal



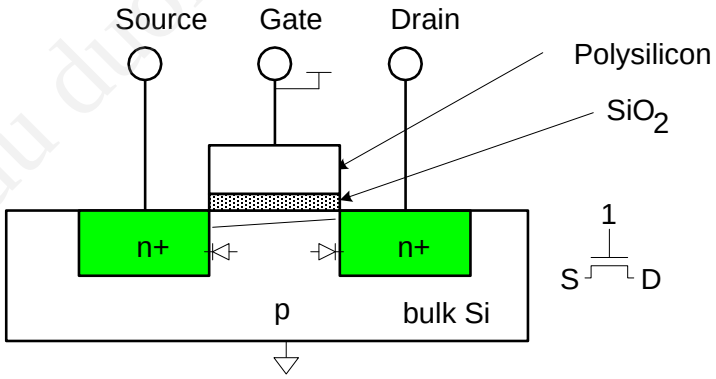
nMOS Operation

- Body is usually tied to ground (0 V)
- When the gate is at a low voltage:
  - P-type body is at low voltage
  - Source-body and drain-body diodes are OFF
  - No current flows, transistor is OFF



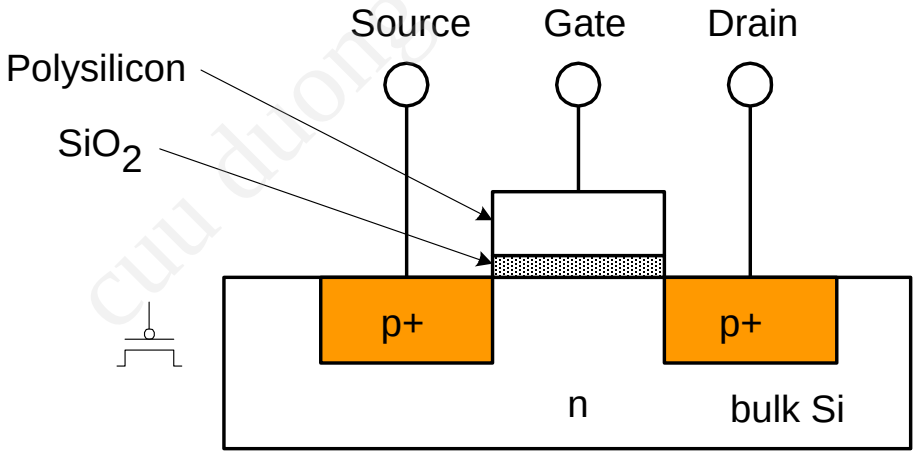
nMOS Operation Cont.

- When the gate is at a high voltage:
  - Positive charge on gate of MOS capacitor
  - Negative charge attracted to body
  - Inverts a channel under gate to n-type
  - Now current can flow through n-type silicon from source through channel to drain, transistor is ON



pMOS Transistor

- Similar, but doping and voltages reversed
  - Body tied to high voltage (V_{DD})
  - Gate low: transistor ON
  - Gate high: transistor OFF
  - Bubble indicates inverted behavior



Transistors

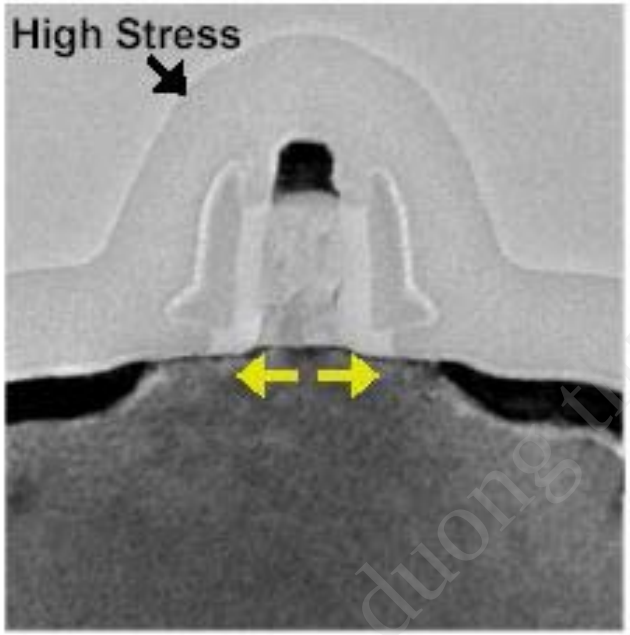


Fig. 3 TEM of NMOS transistor showing high tensile stress nitride overlayer.

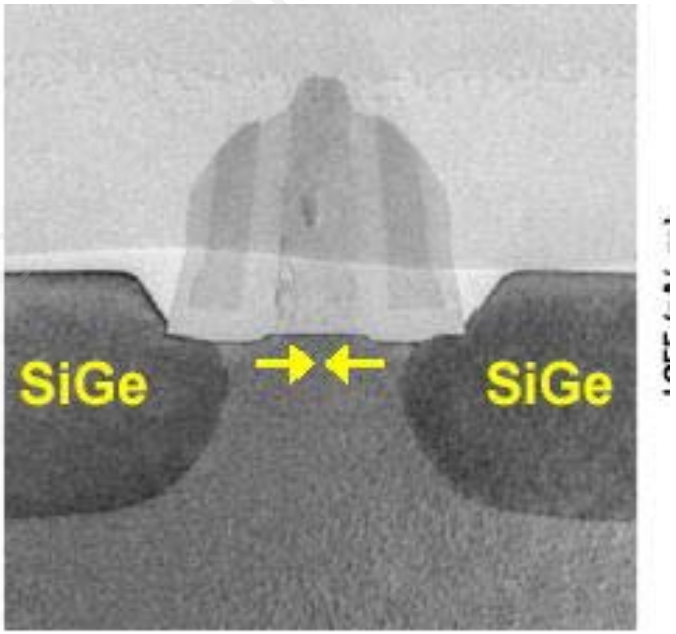
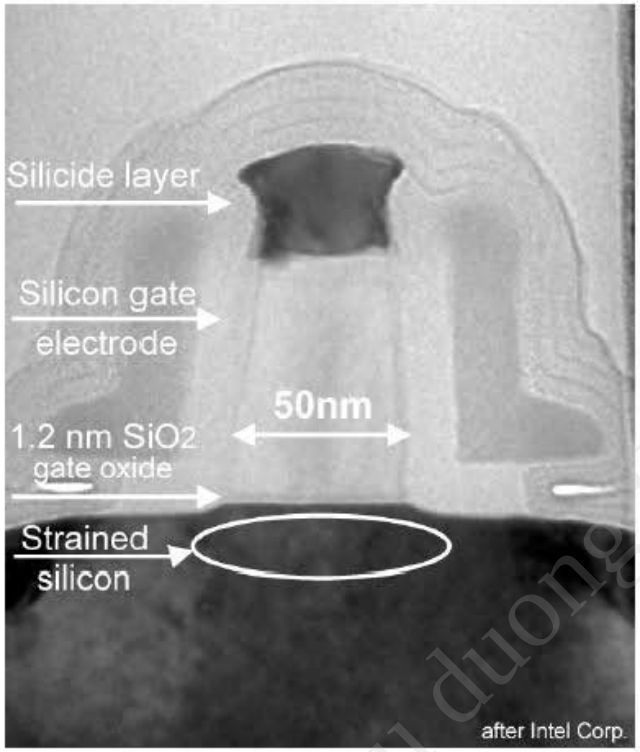
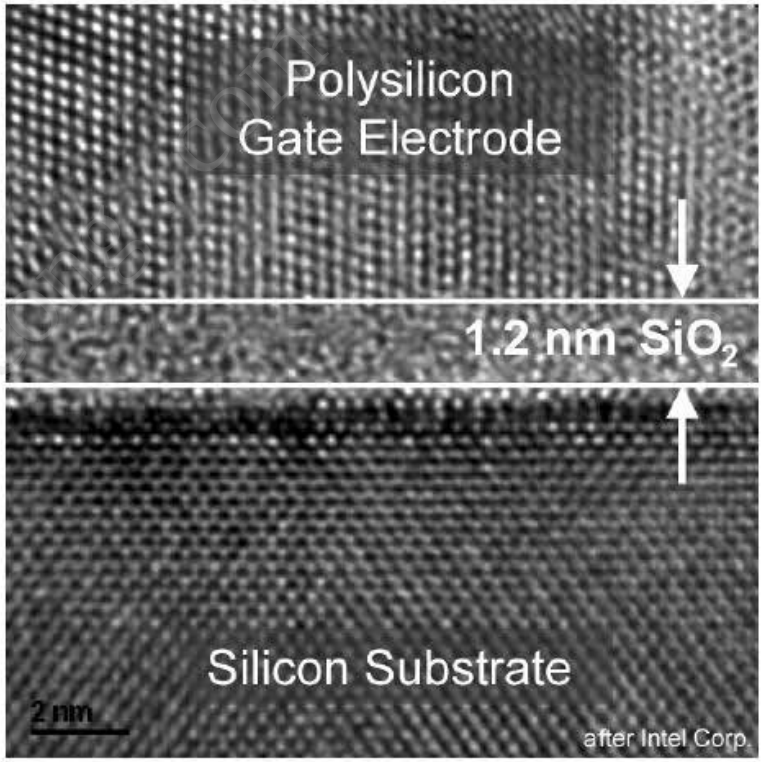


Fig. 4 TEM of PMOS showing SiGe heteroepitaxial S/D inducing uniaxial strain.

Transistors





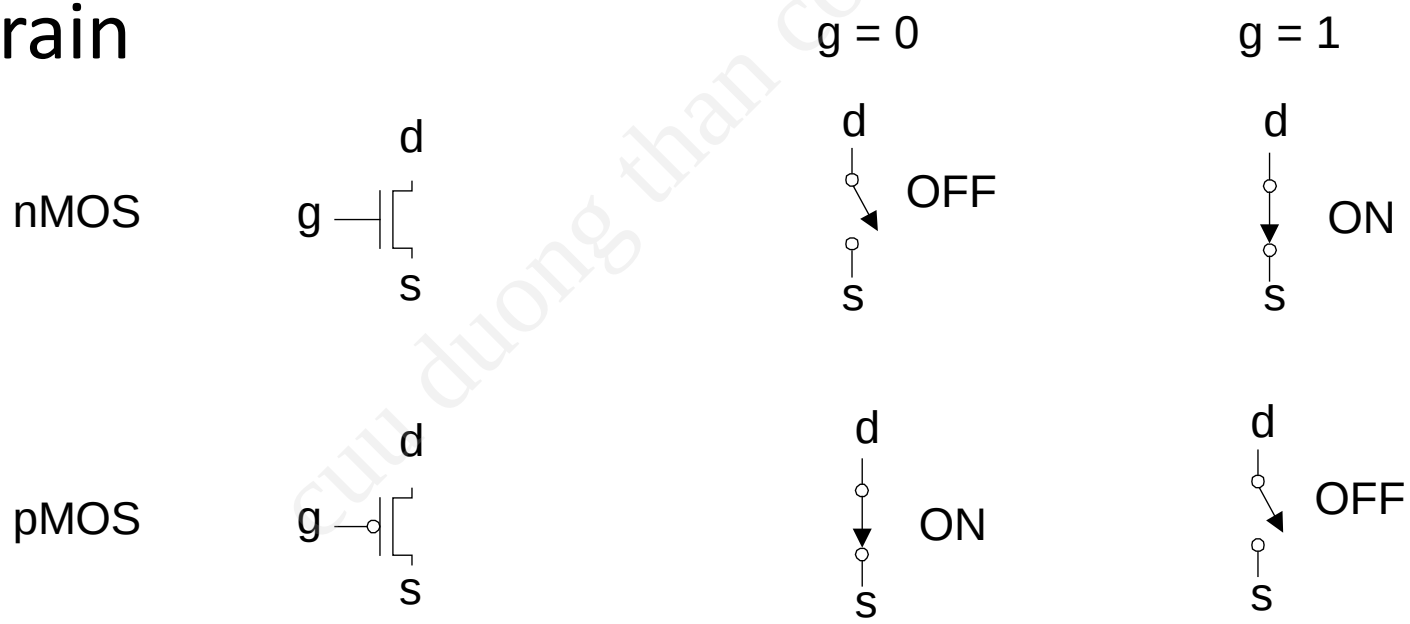
- Micrograph reveals a gate length of 0.05 μm
- Silicide layer has purpose of contacting the poly-Si gate

Power Supply Voltage

- GND = 0 V
- In 1980's, V_{DD} = 5V
- V_{DD} has decreased in modern processes
  - High V_{DD} would damage modern tiny transistors
  - Lower V_{DD} saves power
  - Lower V -> increase f
- V_{DD} = 3.3, 2.5, 1.8, 1.5, 1.2, 1.0, …

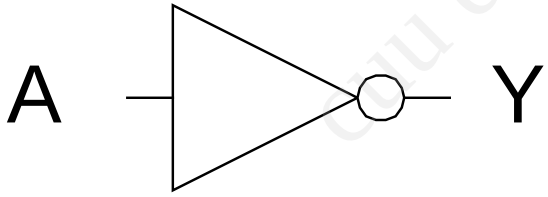
Transistors as Switches

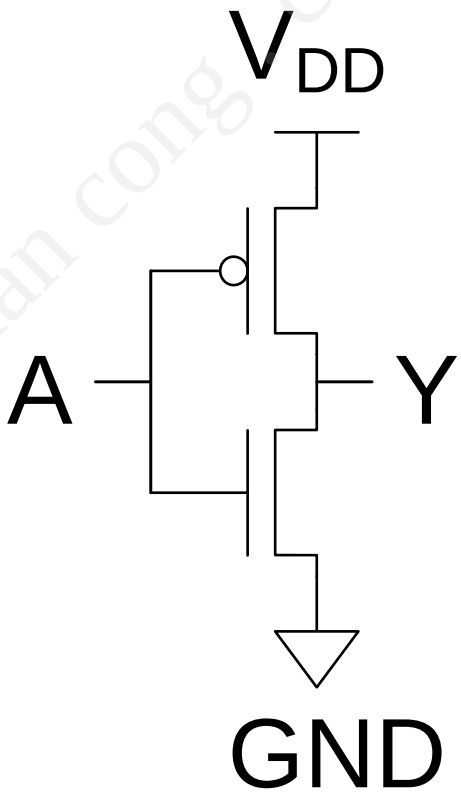
- We can view MOS transistors as electrically controlled switches
- Voltage at gate controls path from source to drain



CMOS Inverter

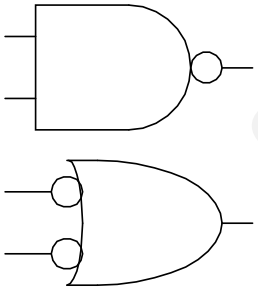
A	Y

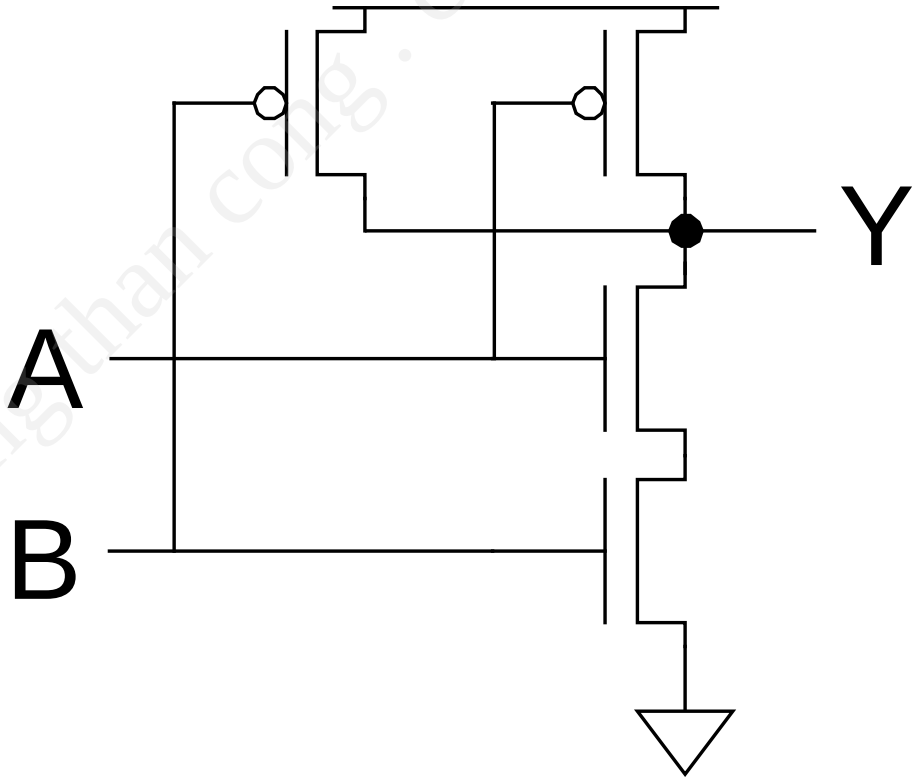




CMOS NAND Gate

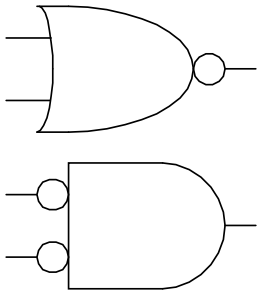
A	B	Y
0	0	
0	1	
1	0	
1	1	

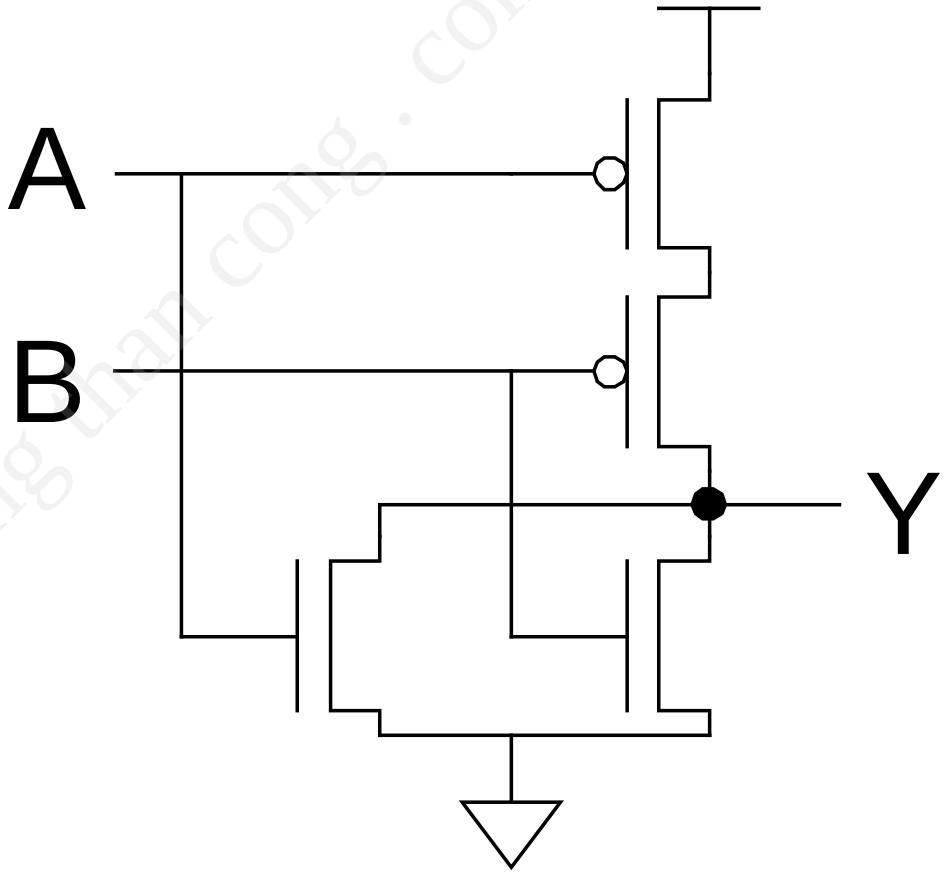




CMOS NOR Gate

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0





3-input NAND Gate

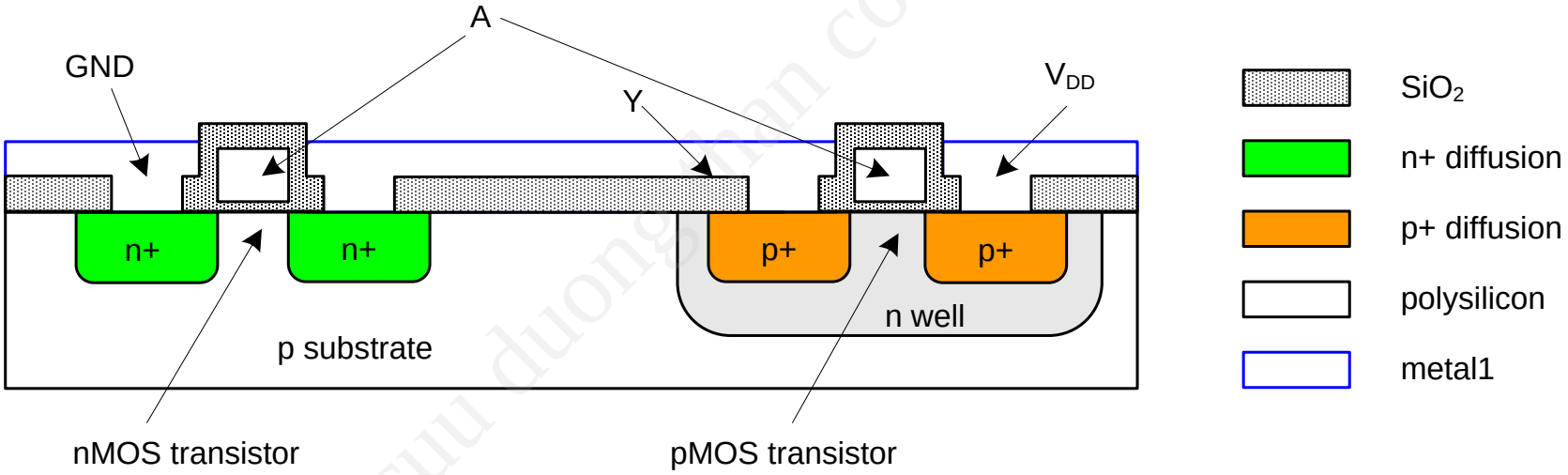
- Y pulls low if ALL inputs are 1
- Y pulls high if ANY input is 0

CMOS Fabrication

- CMOS transistors are fabricated on silicon wafer
- Lithography process similar to printing press
- On each step, different materials are deposited or etched
- Easiest to understand by viewing both top and cross-section of wafer in a simplified manufacturing process

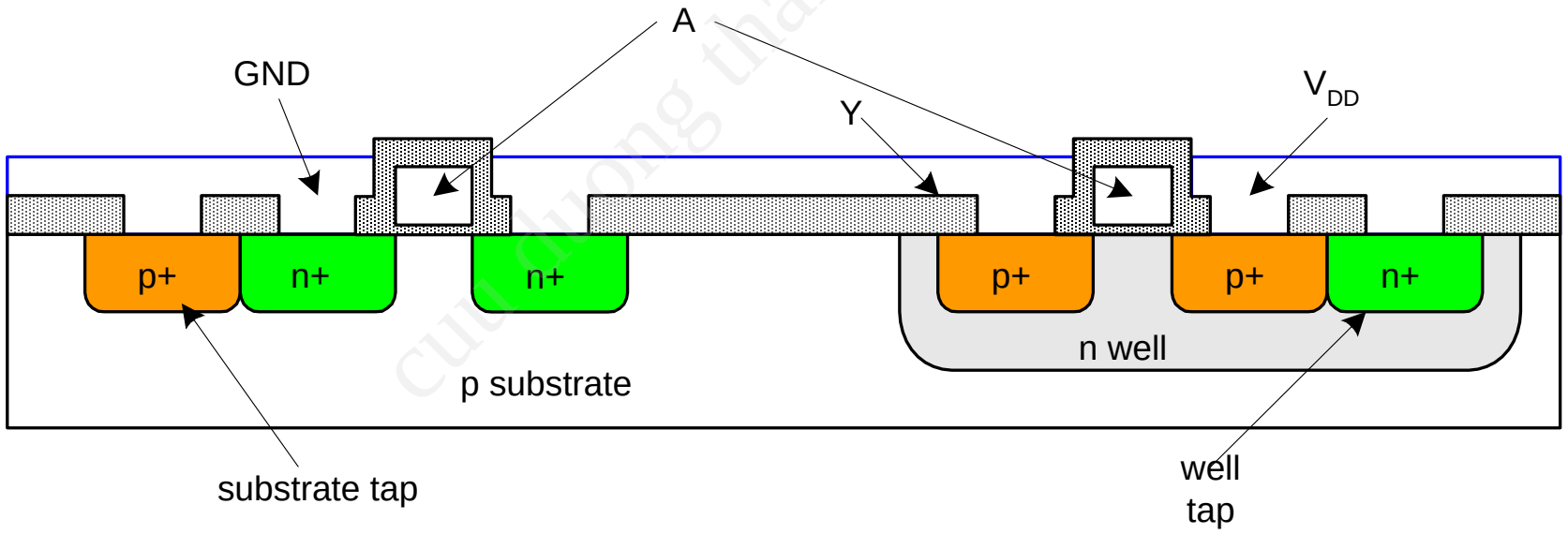
Inverter Cross-section

- Typically use p-type substrate for nMOS transistors
- Requires n-well for body of pMOS transistors



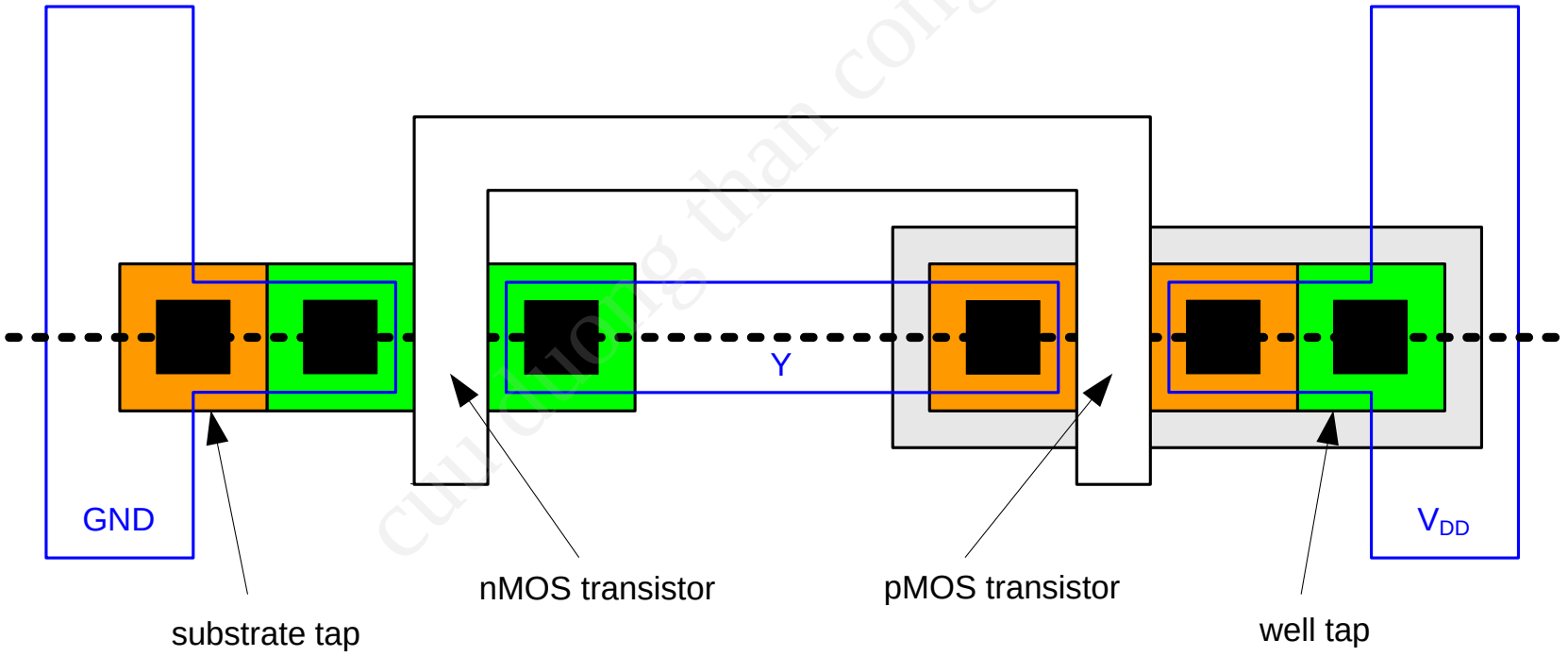
Well and Substrate Taps

- Substrate must be tied to GND and n-well to V_{DD}
- Metal to lightly-doped semiconductor forms poor connection called Shottky Diode
- Use heavily doped well and substrate contacts / taps



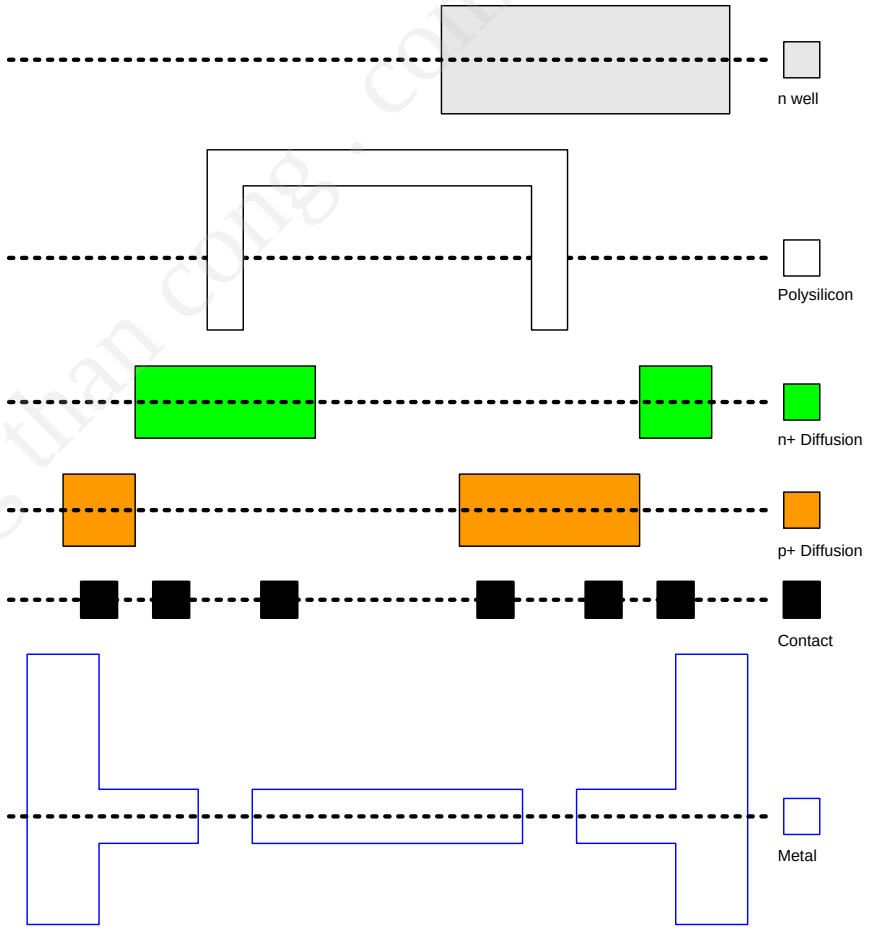
Inverter Mask Set

- Transistors and wires are defined by *masks*
- Cross-section taken along dashed line



Detailed Mask Views

- Six masks
  - n-well
  - Polysilicon
  - n+ diffusion
  - p+ diffusion
  - Contact
  - Metal

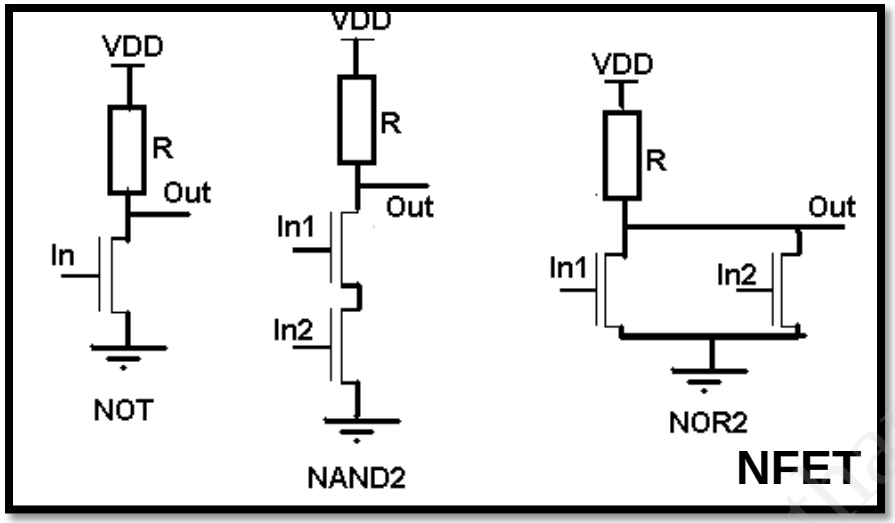


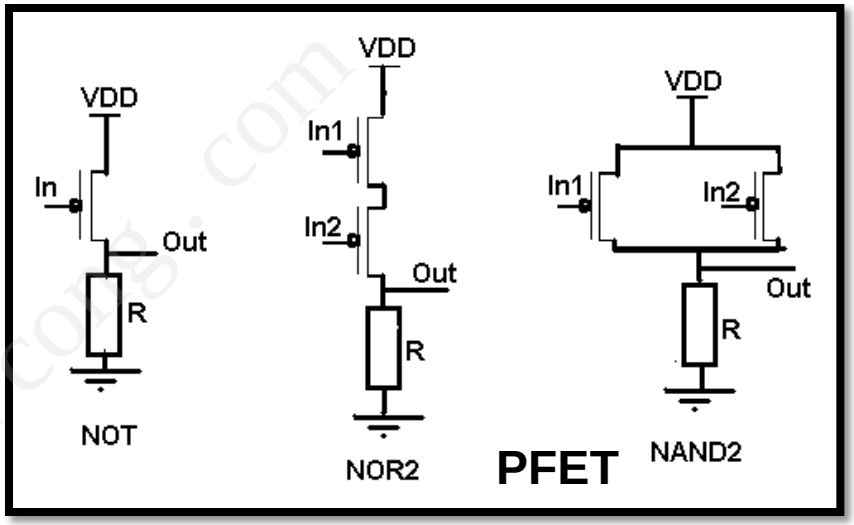
Fabrication

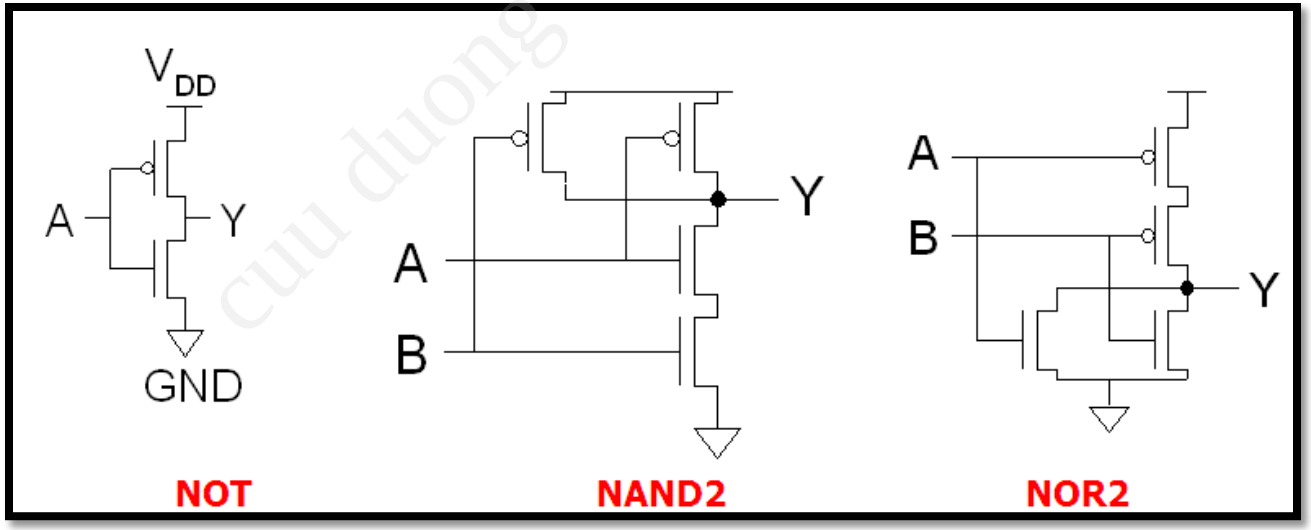
- Chips are built in huge factories called fabs
- Contain clean rooms as large as football fields

Courtesy of International Business Machines Corporation. Unauthorized use not permitted.

Logic gates



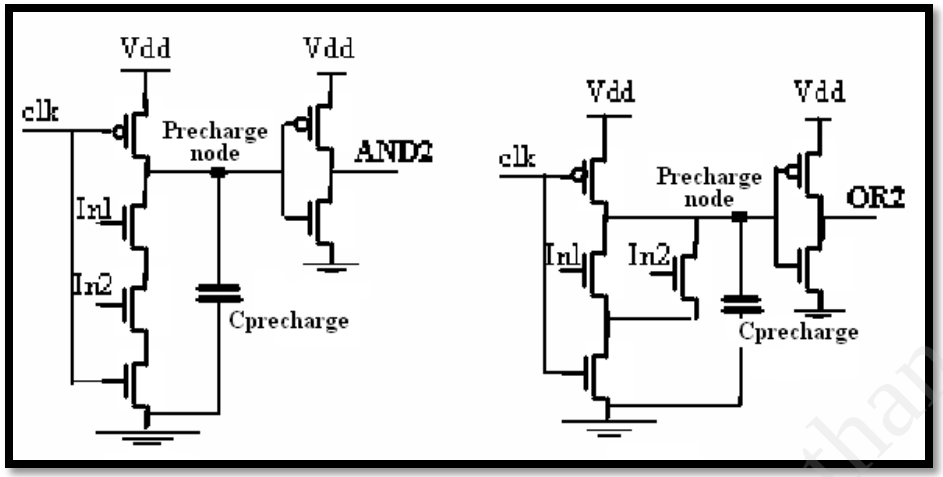


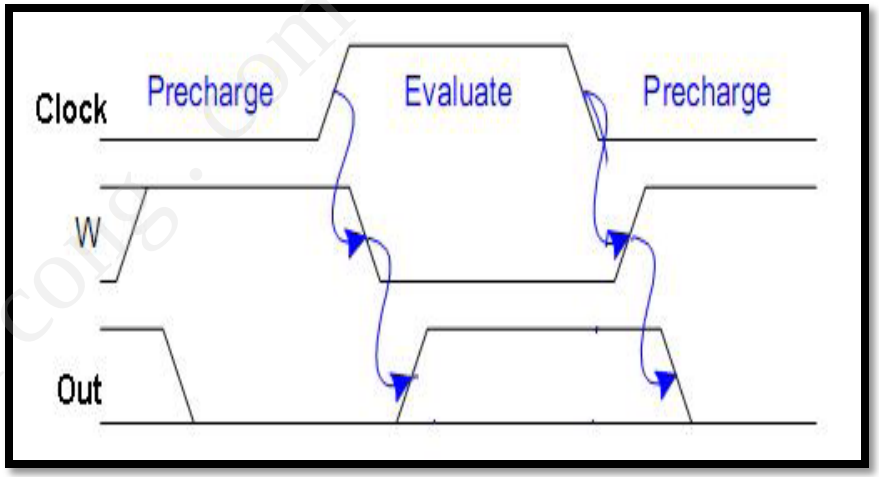


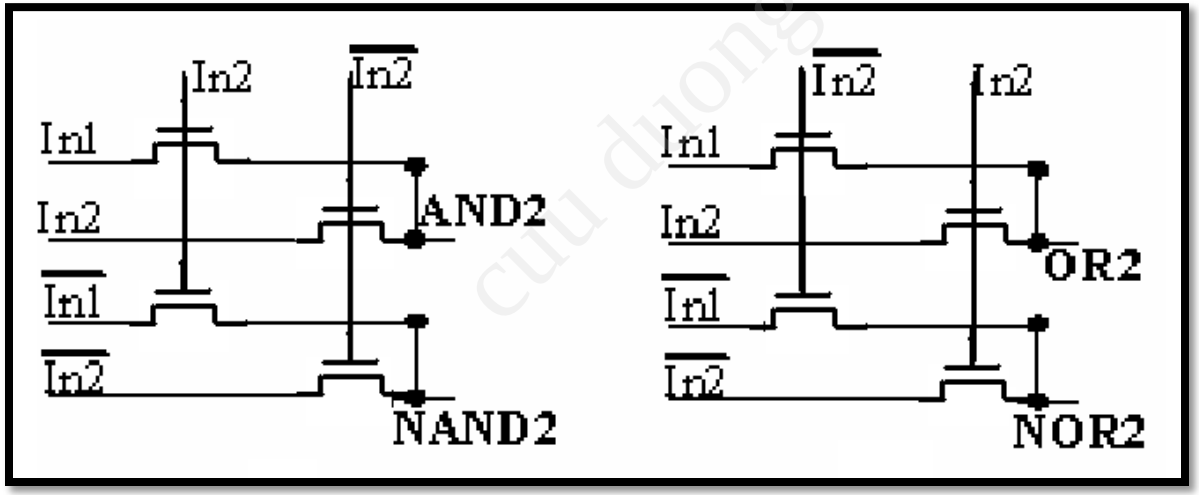
CMOS

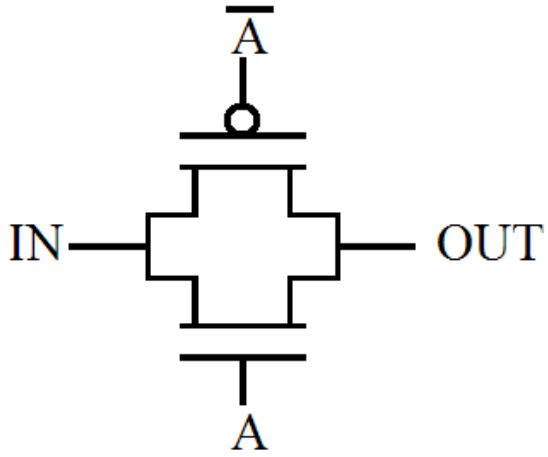
Logic Gates

- Domino





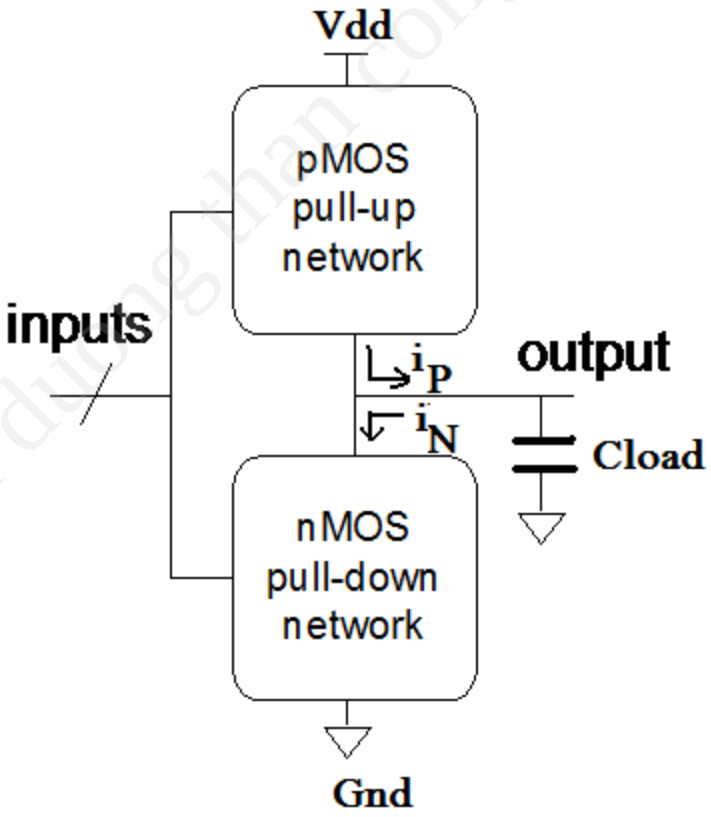




Pass-transistor

Logic Gates

- Generalized CMOS logic gates

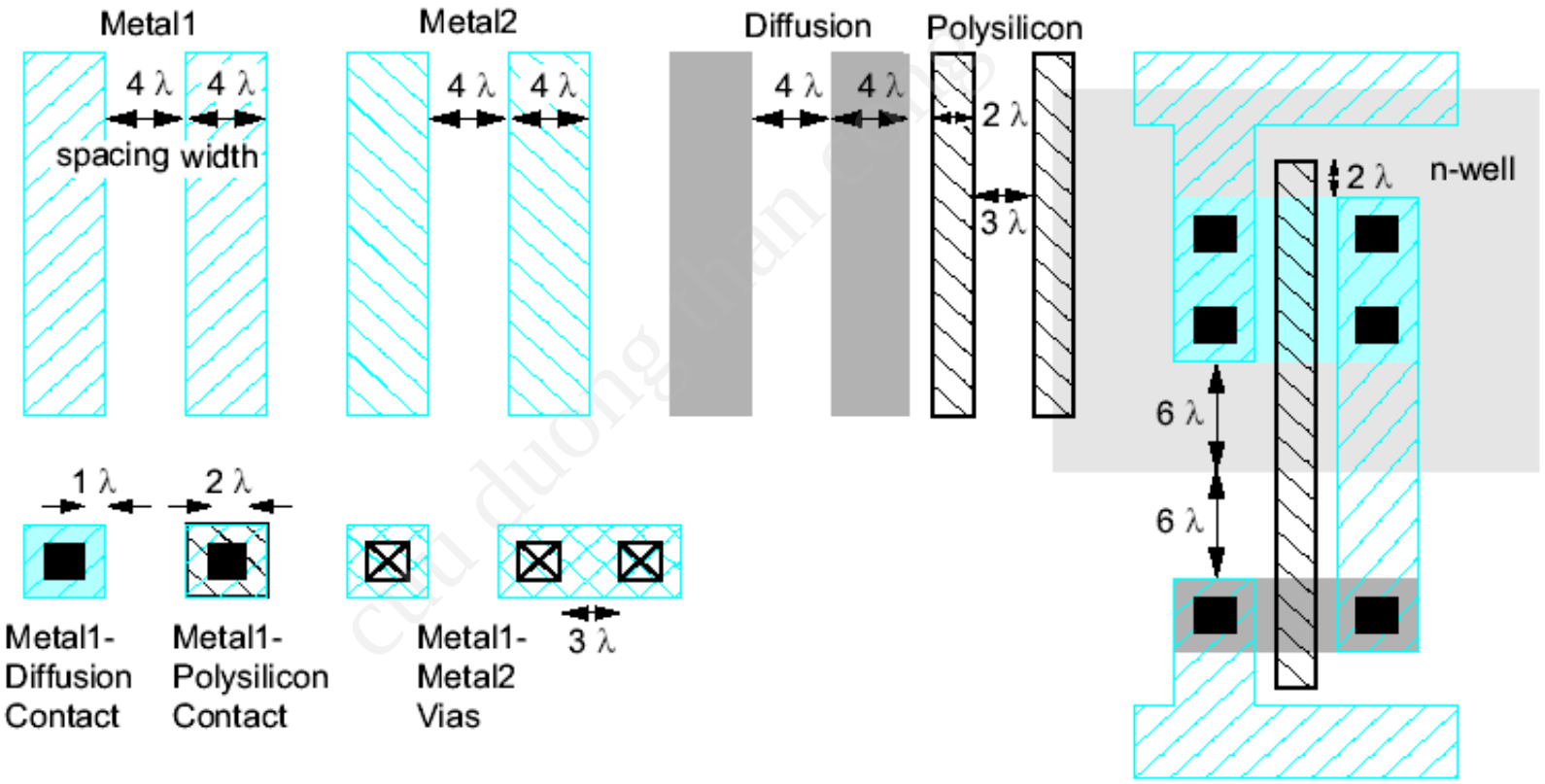


2.3 Layout

- Chips are specified with set of masks
- Minimum dimensions of masks determine transistor size (and hence speed, cost, and power)
- Feature size f = distance between source and drain
  - Set by minimum width of polysilicon
- Feature size improves 30% every 3 years or so
- Normalize for feature size when describing design rules
- Express rules in terms of $\lambda = f/2$
  - E.g. λ = 0.3 μm in 0.6 μm process

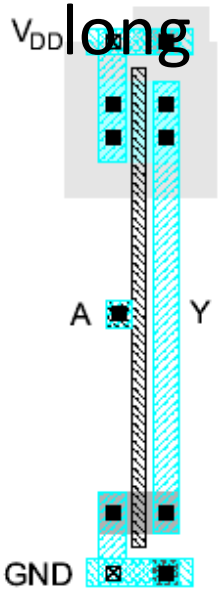
Simplified Design Rules

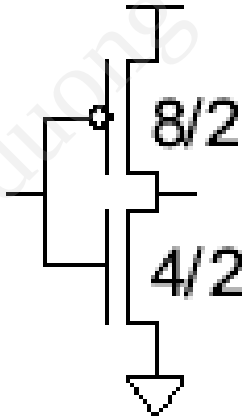
- Conservative rules to get you started

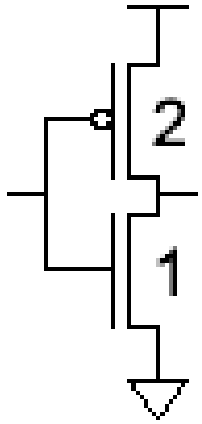


Inverter Layout

- Transistor dimensions specified as Width / Length
  - Minimum size is 4λ / 2λ, sometimes called 1 unit
  - In f = 0.6 μm process, this is 1.2 μm wide, 0.6 μm long



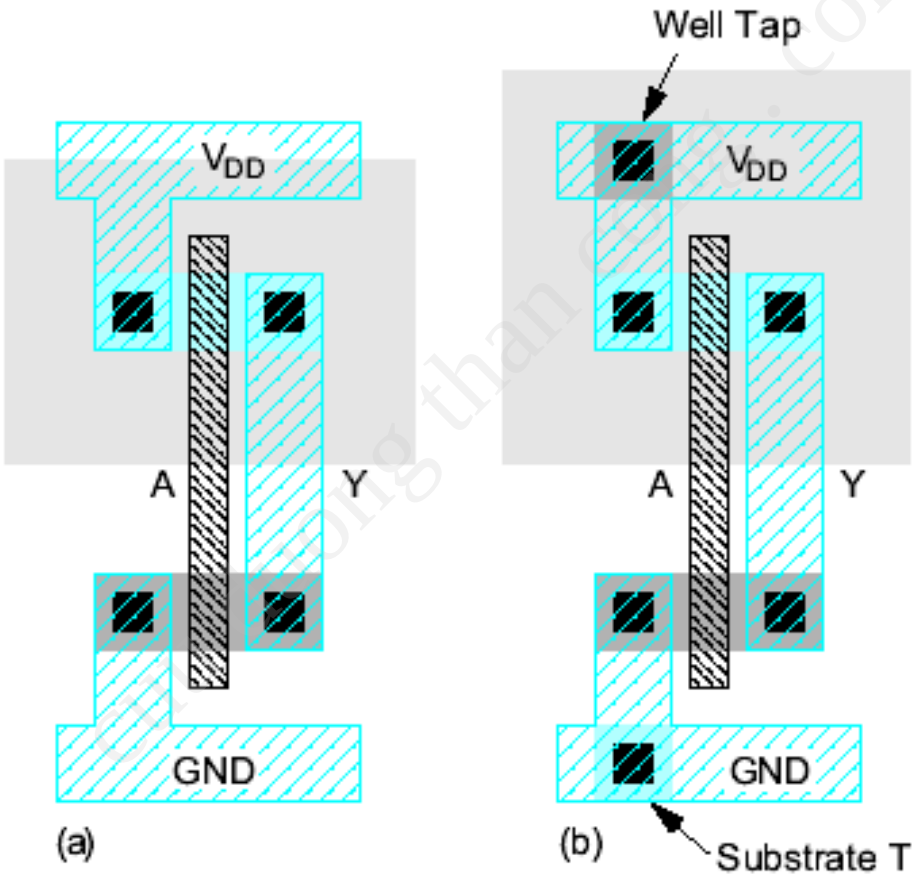




Gate Layout

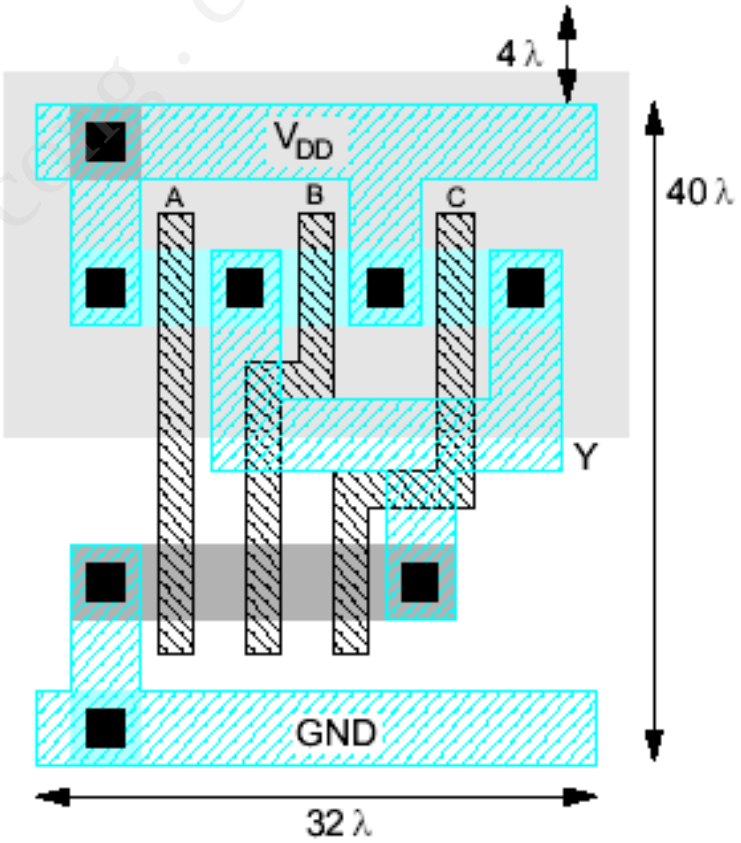
- Layout can be very time consuming
  - Design gates to fit together nicely
  - Build a library of standard cells
- Standard cell design methodology
  - V_{DD} and GND should abut (standard height)
  - Adjacent gates should satisfy design rules
  - nMOS at bottom and pMOS at top
  - All gates include well and substrate contacts

Example: Inverter



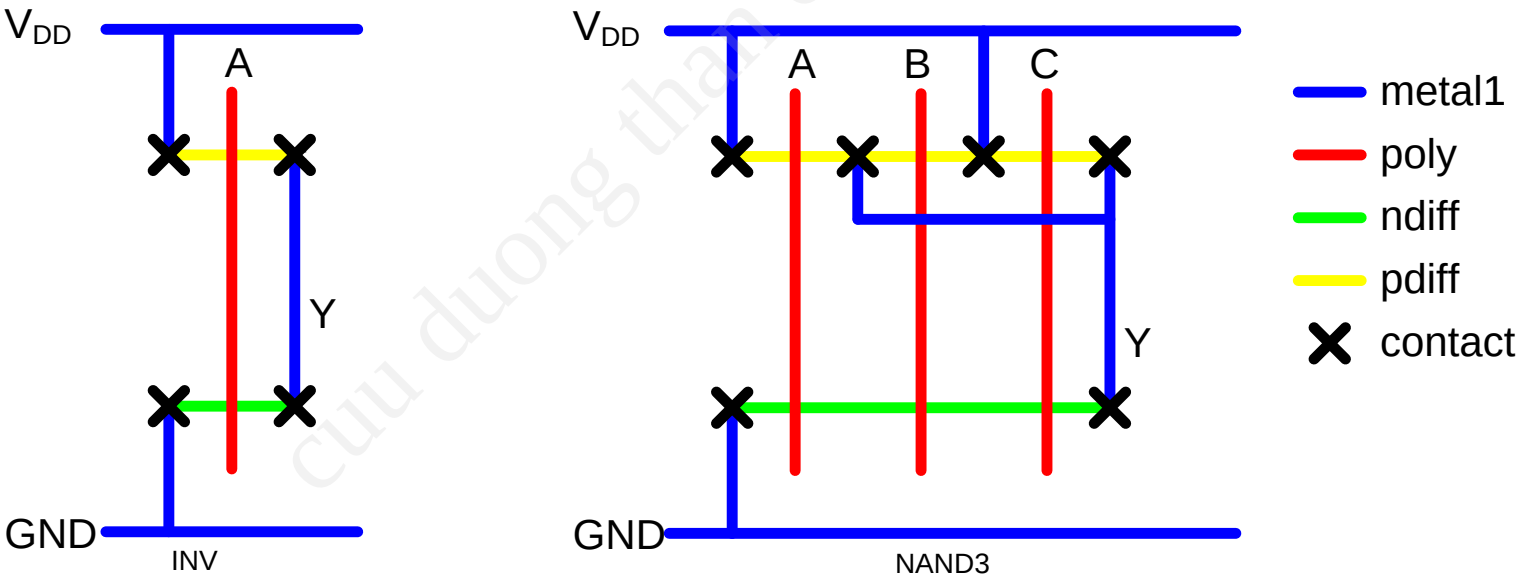
Example: NAND3

- Horizontal N-diffusion and p-diffusion strips
- Vertical polysilicon gates
- Metal1 V_{DD} rail at top
- Metal1 GND rail at bottom
- 32 λ by 40 λ



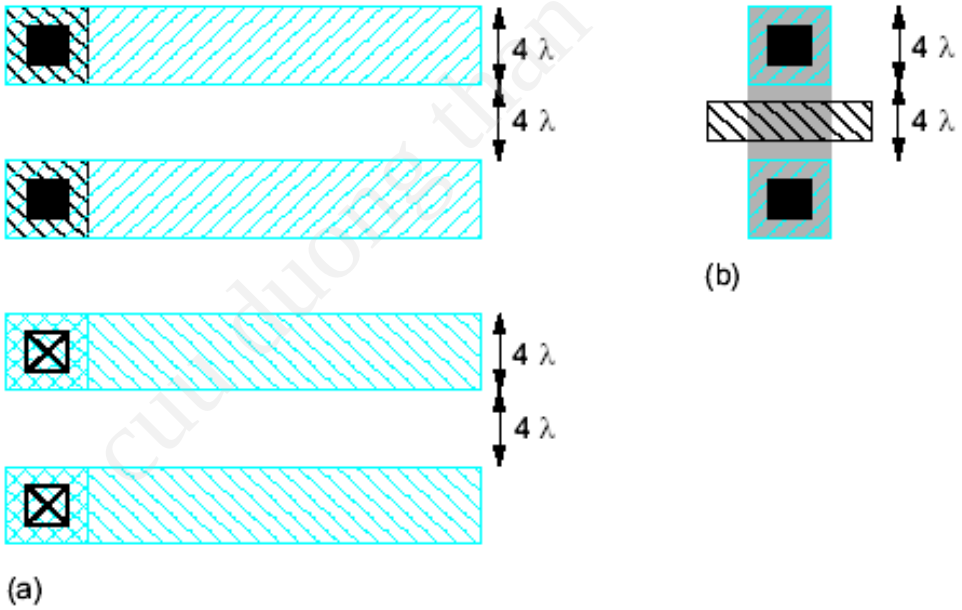
Stick Diagrams

- *Stick diagrams* help plan layout quickly
  - Need not be to scale
  - Draw with color pencils or dry-erase markers



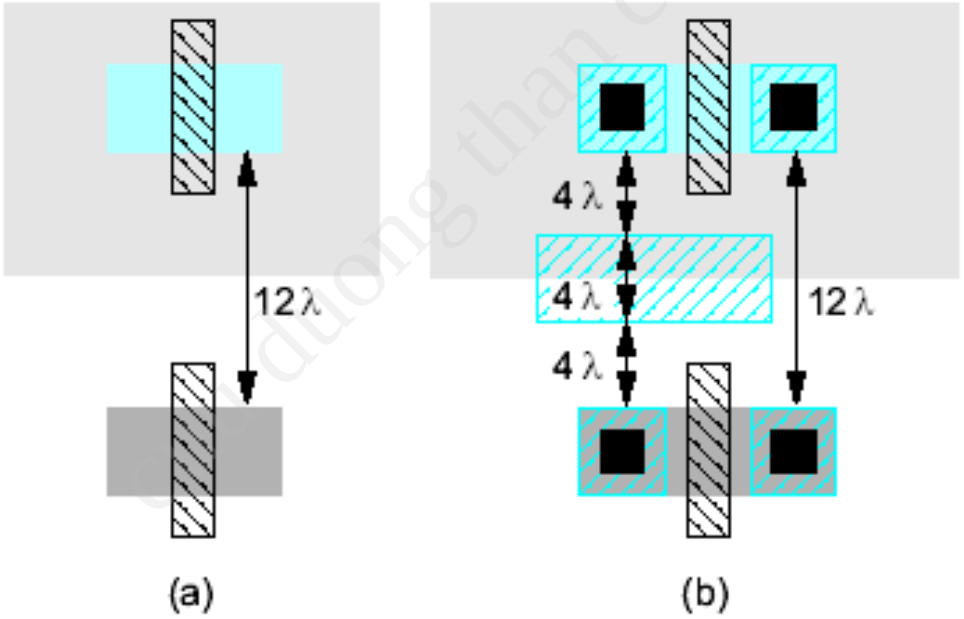
Wiring Tracks

- A *wiring track* is the space required for a wire
  - 4 λ width, 4 λ spacing from neighbor = 8 λ pitch
- Transistors also consume one wiring track



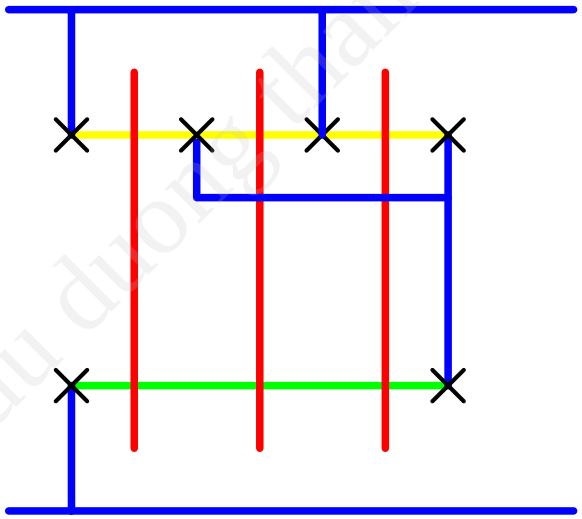
Well spacing

- Wells must surround transistors by 6 λ
  - Implies 12 λ between opposite transistor flavors
  - Leaves room for one wire track



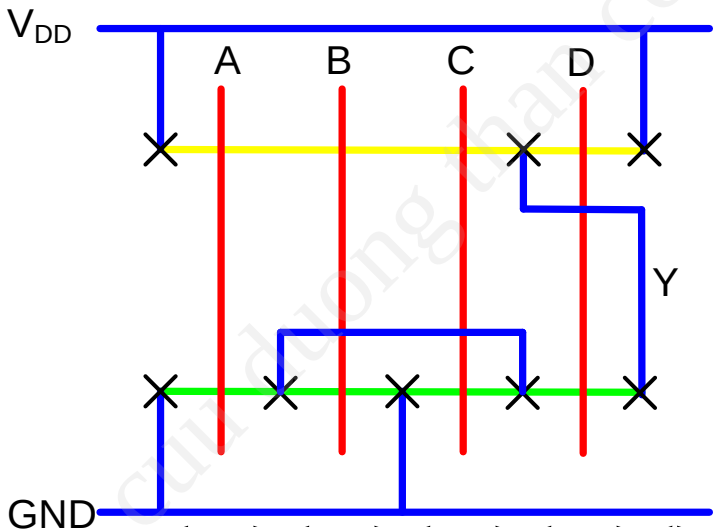
Area Estimation

- Estimate area by counting wiring tracks
  - Multiply by 8 to express in λ



Example: O3AI

- Sketch a stick diagram for O3AI and estimate area
  - $Y = \overline{(A + B + C) \cdot D}$



2.3 Design Tools

- Leader companies in the Electronic Design Automation industry
  - Synopsys
  - Cadence
  - Mentor Graphic
  - Magma Design Automation

Synopsys

- History
  - founded in 1986 by Dr. Aart J. de Geus, David Gregory and a team of engineers from General Electric
  - acquired many companies: Synplicity, Chipidea, CoWare, Virage Logic, Magma Design Automation, …

Building on the Hillsboro, Oregon, campus

Synopsys Tools

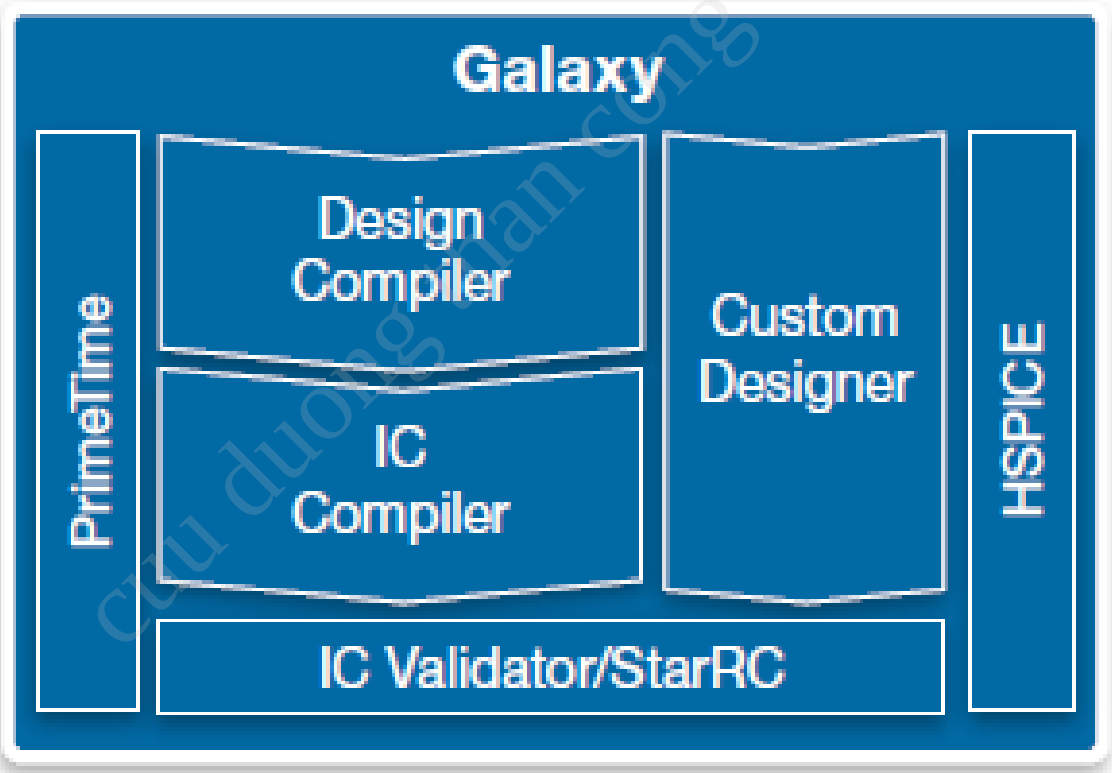
- Categories by Design Phase

System-Level Design High-level block design, architecture design, virtual and FPGA-based prototyping, and, power electronics and wiring harness solutions	**Manufacturing** Mask synthesis and data prep, lithography simulation and verification and yield management
Verification High-performance system, RTL, equivalence checking, mixed-signal verification solutions, and Verification IP	**TCAD** Process and device simulation solutions for technology development and manufacturing
Implementation & Signoff Advanced digital and custom IC and FPGA design solutions, including synthesis, physical implementation, test and signoff	**Optical Design** Optical design and analysis software and engineering services

Synopsys tools

- http://www.synopsys.com

Implementation and Signoff



Design Compiler

- Synopsys provides an integrated RTL synthesis solution.
  - Produce fast, area-efficient ASIC designs
  - Translate designs from one technology to another
  - Explore design tradeoffs involving design constraints
  - Synthesize and optimize finite state machines
  - Integrate netlist inputs and netlist outputs into third-party environments
  - Create and partition hierarchical schematics automatically

Design Compiler Family

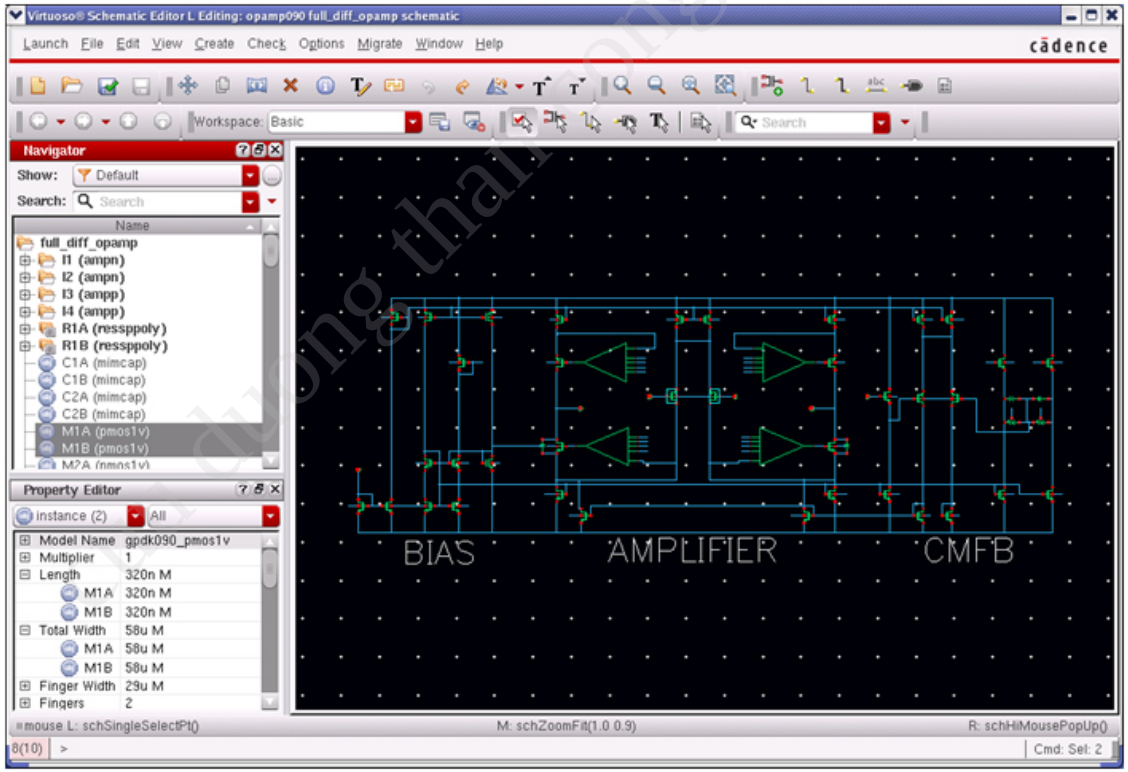
Design Compiler Family	Description
DC Expert	applied to high-performance ASIC and IC designs.
DC Ultra	applied to high-performance deep submicron ASIC and IC designs,
DC Explorer	perform early RTL exploration, leading to a better starting point for RTL synthesis and accelerating design implementation.
HDL Compiler	reads HDL files and performs translation and architectural optimization of the designs.
DesignWare Library	is a collection of reusable circuit-design building blocks
DFT Compiler	provides integrated design-for-test capabilities, including constraint-driven scan insertion during compile.
Power Compiler	offers a complete methodology for power, including analyzing and optimizing designs for static and dynamic power consumption.
Design Vision	is a graphical user interface (GUI) to the Synopsys synthesis environment and an analysis tool for viewing and analyzing designs

Cadence Design Systems

- **Virtuoso Platform** - Tools for designing full-custom integrated circuits;[2] includes schematic entry, behavioral modeling
- **Encounter Platform** - Tools for creation of digital integrated circuits.
- **Incisive Platform** - Tools for simulation and functional verification of RTL including Verilog, VHDL and SystemC
- **Verification IP** (VIP) Cadence provides the broadest set of commercial VIP available with over 30 protocols in its VIP Portfolio.
- **Integration Optimized IP** (Design IP) Cadence offers Vertically Integrated IP, inclusive of Digital Controller, Serdes Layer, and Device Driver.
- **Allegro Platform** - Tools for co-design of integrated circuits, packages, and PCBs
- **OrCAD/PSpice** - Tools for smaller design teams and individual PCB designers

Virtuoso Platform

- Virtuoso Schematic Editor
- Virtuoso Analog Design Environment
- Virtuoso Visualization and Analysis



Virtuoso Schematic Editor

Open Source Software for IC Design

Open source software	Description	Web site
toped	Micron based layout editor with extensive scripting capabilities. Under active development and part of Fedora Electronic Lab.	http://www.toped.org.uk
microwind3	Lambda based layout editor especially adapted for interactive design with Spice. This used to be completely free, but now only a Lite version is.	http://www.microwind.org
magic	Lambda based layout editor with good options for writing CIF and/or GDS files. Supports scripting. Large user base. Part of Fedora Electronic Lab. Used for extraction and CIF/GDS creation by the pharosc libraries	http://opencircuitdesign.com/magic
lasi	LASI stands for LAyout Software for Individuals. It is designed to run on Windows, though it also runs on Linux under Crossover Office. Actively used software with frequent updates.	http://lasihomesite.com
kic	Part of open source packages released by Whiteley Research.	http://wrcad.com/freestuff.html

- http://www.vlsitechnology.org/html/ic_software.html

Questions

1. Describe IC fabrication process
2. Describe nMOS transistor
3. Describe CMOS fabrication
4. Draw the following gates by stick diagram:
   a) 3-input NOR
   b) 3-input NAND
   c) 2-input XOR
   d) 2-input XNOR
5. Draw a NOT gate by LEdit tool