ĐẠI HỌC QUỐC GIA TP.HỒ CHÍ MINH
TRƯỜNG ĐẠI HỌC BÁCH KHOA
KHOA ĐIỆN-ĐIỆN TỬ
BỘ MÔN KỸ THUẬT ĐIỆN TỬ

# ASIC CHIP AND IP CORE DESIGN

Chapter 5: Physical Design

5.1 System partitioning
5.2 Floorplanning and placement
5.3 Routing

5.1 System Partitioning

- System partitioning requires goal and objectives
  - A maximum size of each ASIC
  - A maximum number of ASICs
  - A maximum number of connections for each ASIC
  - A maximum number of total connections between all ASICs
- Example
  - Use no more than 3 ASICs
  - Each ASIC contains no more than 4 logic cells
  - Use the minimum number of external connections for each ASIC
  - Use the minimum total number of external connections
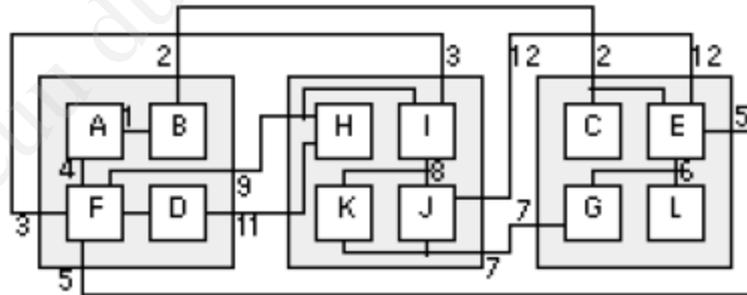
Partitioning Example

- Example
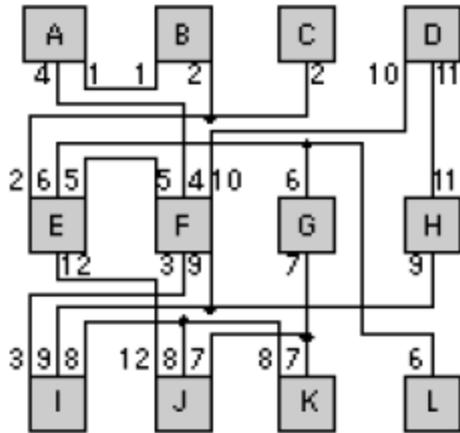
A design to be partitioned
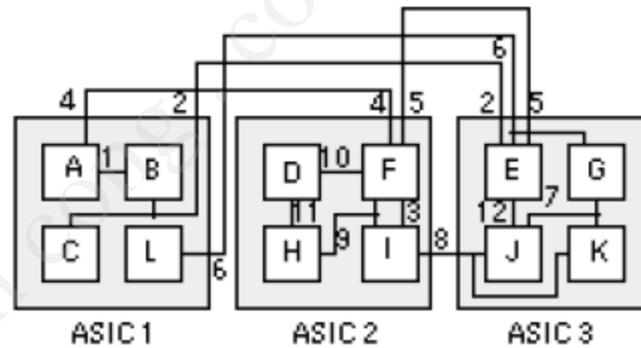
A partitioning with 5 connections
(nets 2, 4, 5, 6, 8)

A constructed partitioning using logic
cell C as a seed

5.2 Floorplanning and Placement

- ## Floorplanning:
  - ### Goals:
    - Arrange the blocks on a chip
    - Decide the location of the IO pads
    - Decide the location and number of the power pads
    - Decide the location and type of clock distribution
  - ### Objectives:
    - Minimize the chip area
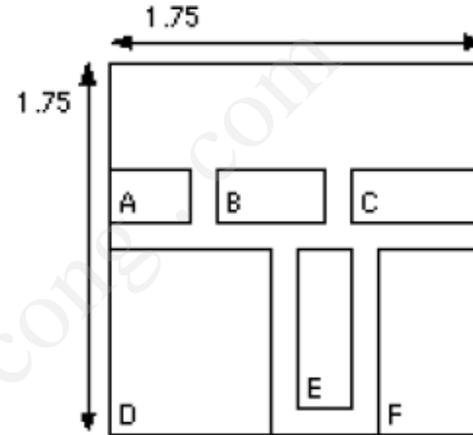   - Minimize delay

Floorplanning Examples
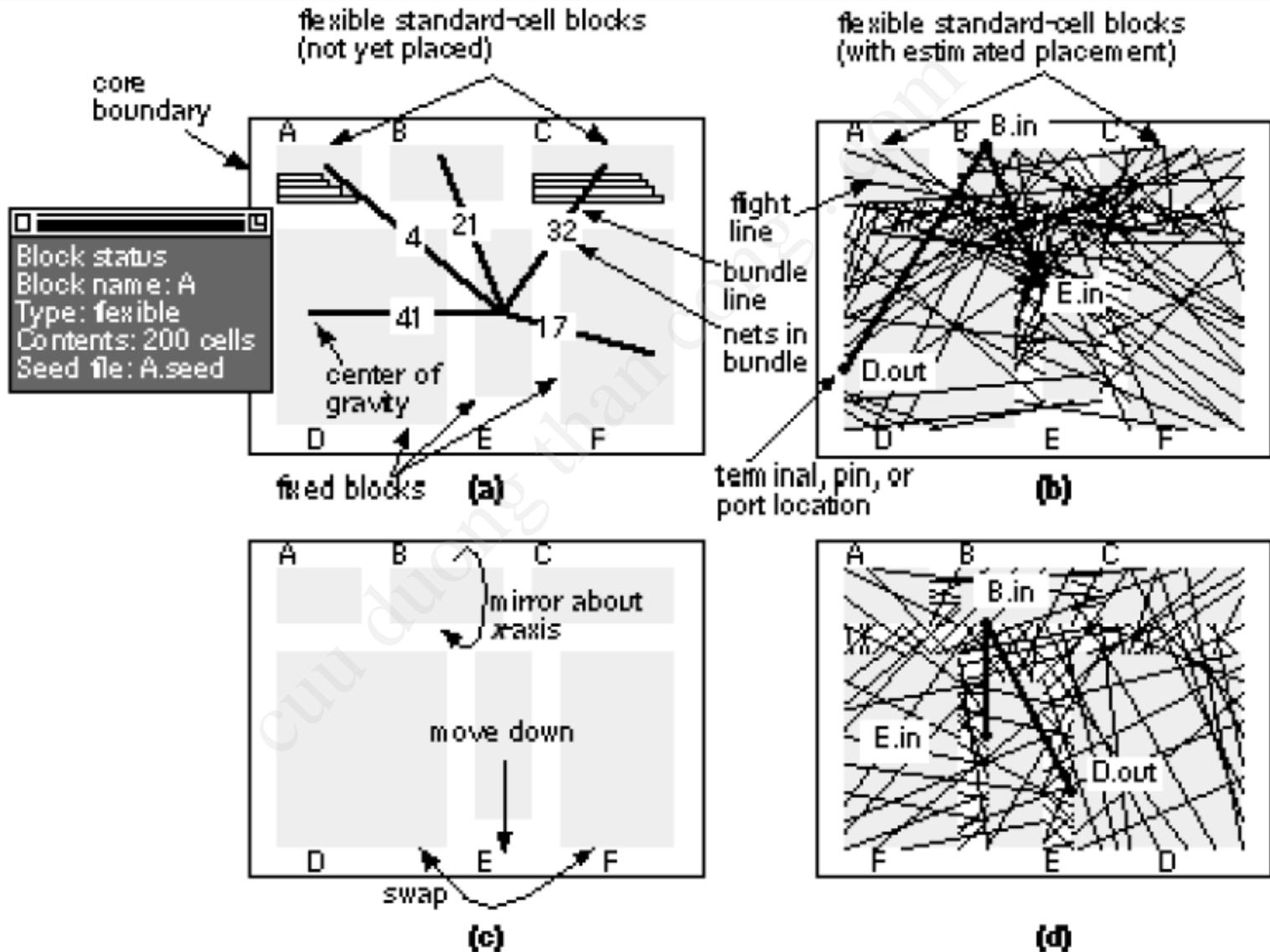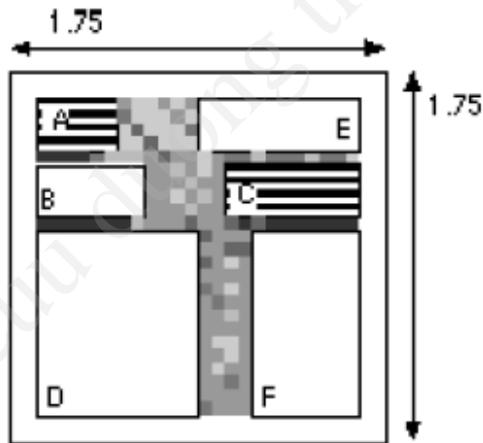
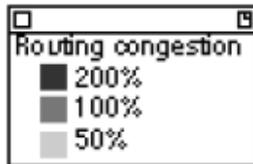# Floorplanning Examples
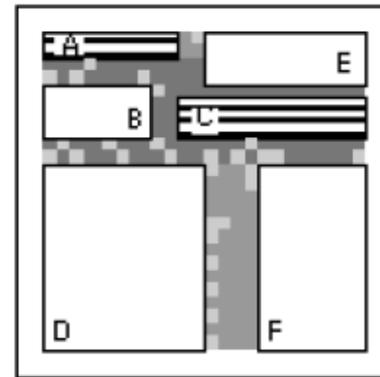

Initial floorplanning with 2:1.5 ratio
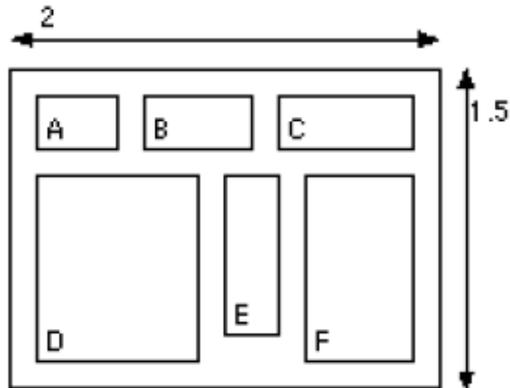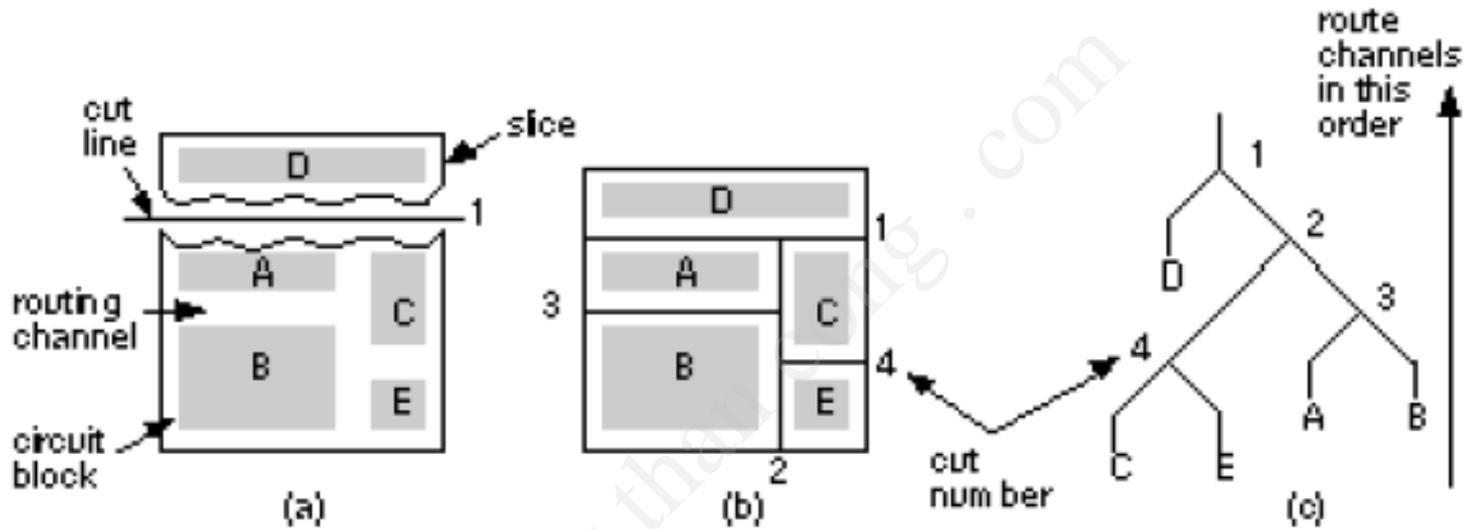
(a)

Floorplanning with 1:1 ratio

(b)

A trial floorplanning

(c)

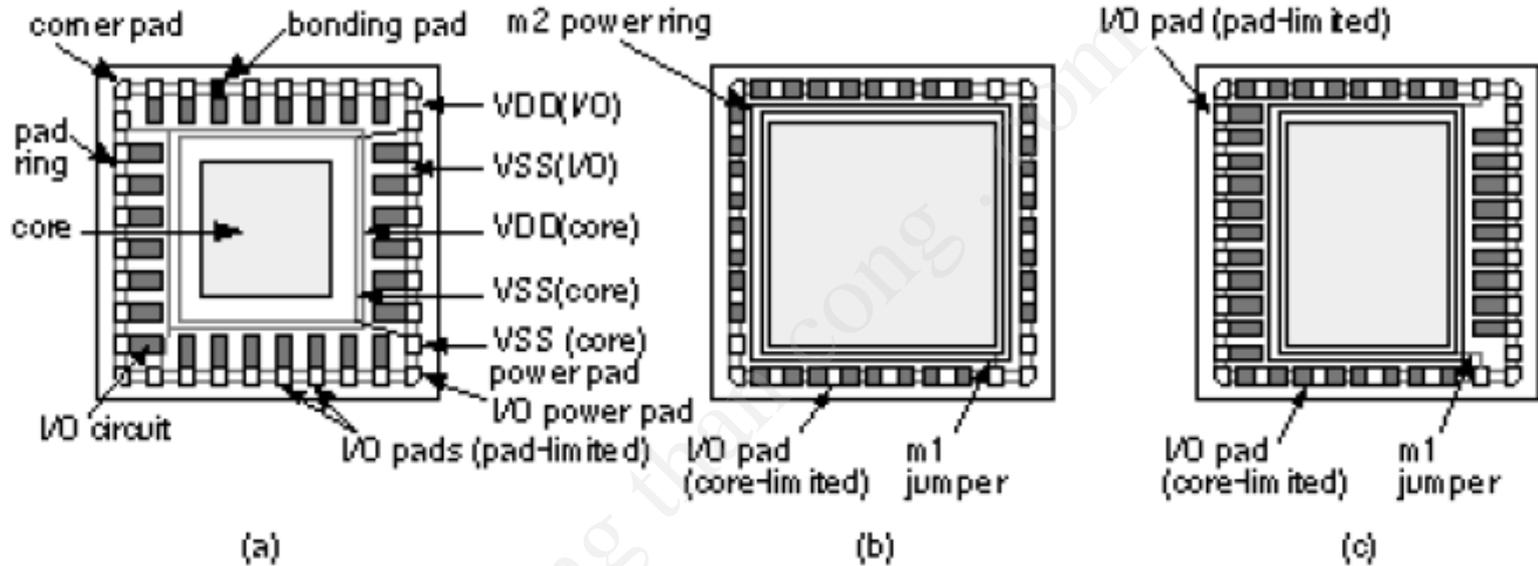Resizing block A and C

(d)

Make a cut for
the first routing

A sequence of
cuts

A slicing tree

IO and Power Planning

(a) A pad-limited die
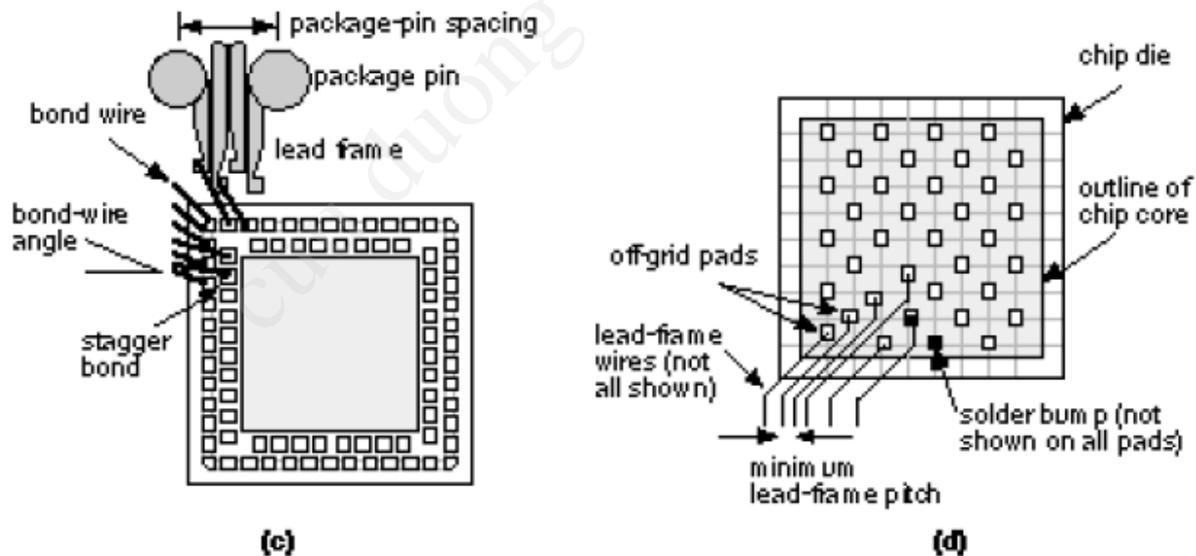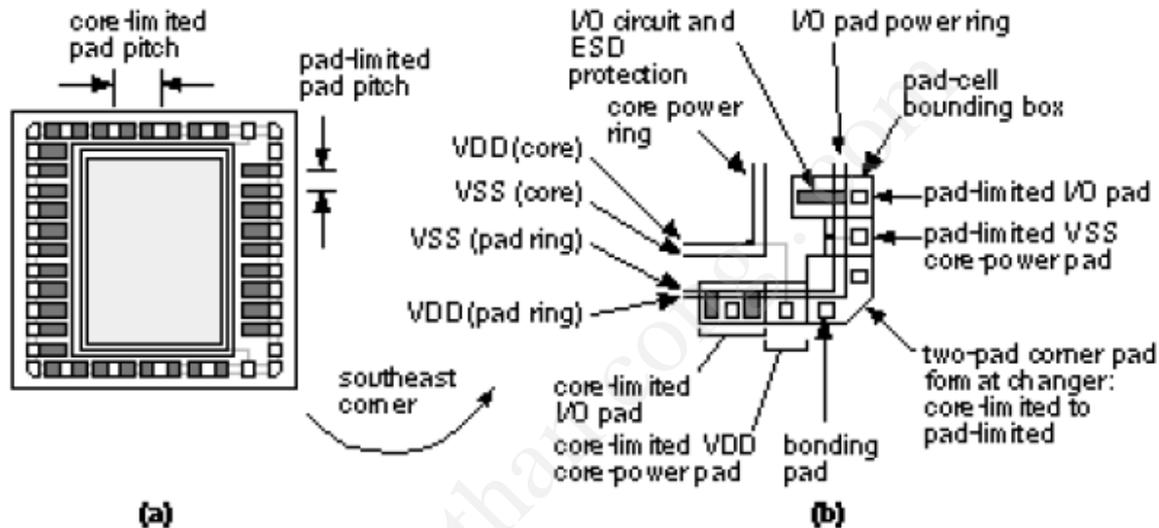(The number of pads determines the die size)

=> Use tall, thin pads

(b) A core-limited die
(The core logic determines the die size)

=> Use short, wide pads

(c) Using both pad-limited pads and core-limited pads for square die
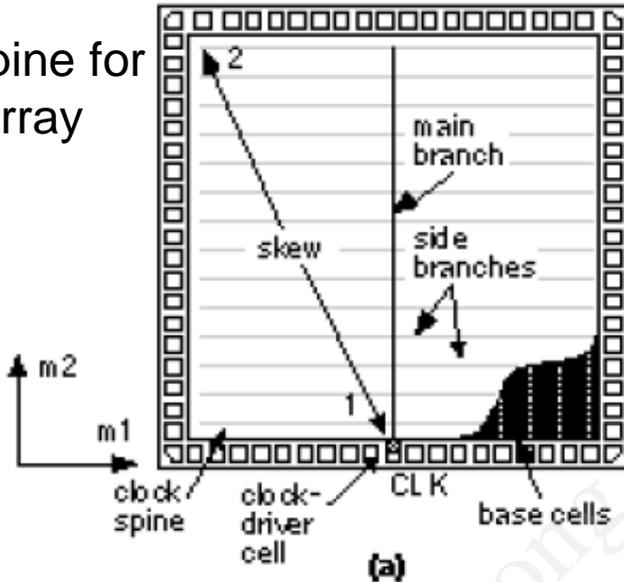
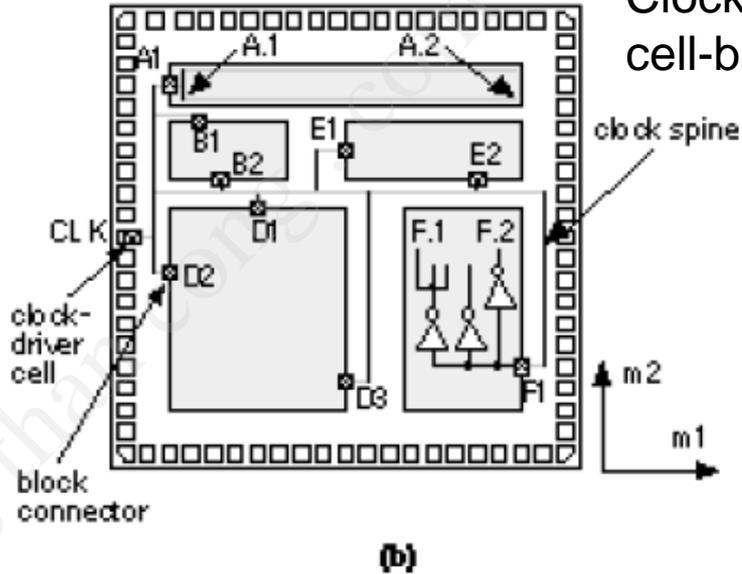# Bonding Pads

Floorplanning Process

- Define and create core area
- Create/assign IO pin
- Place pins or IO pads
- Make connect pins, standard cell
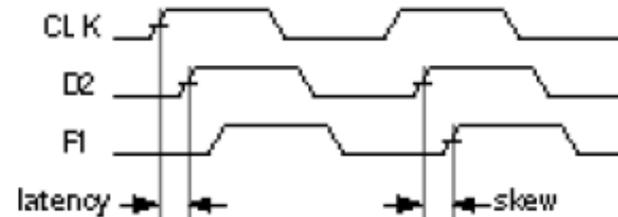- Create power ring, strap, grid
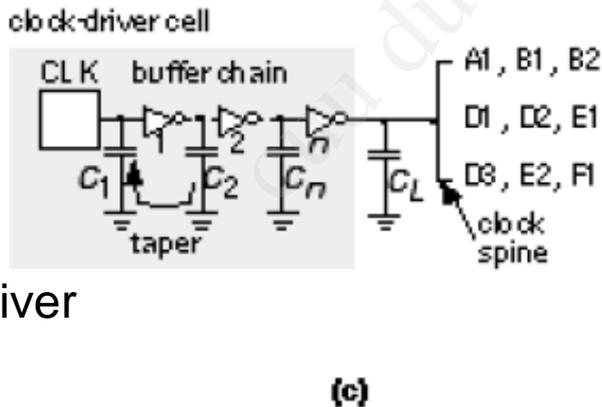- Check floorplanning

Clock spine for a gate array
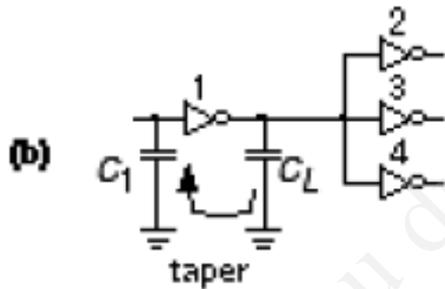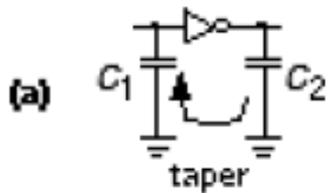
Clock spine for a cell-based ASIC
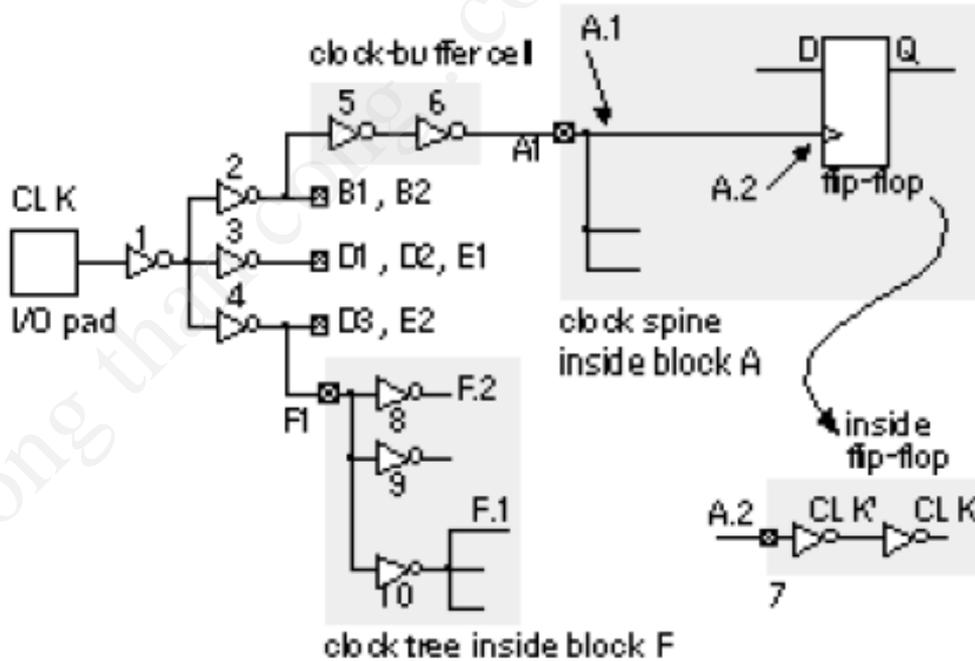
Delay in driver cell

Clock latency and Clock skew

Clock Tree

Minimum delay

(a)

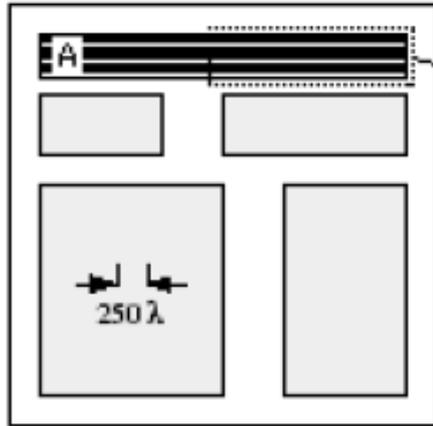Using a fanout of the three at successive nodes

Clock tree for the cell-based ASIC
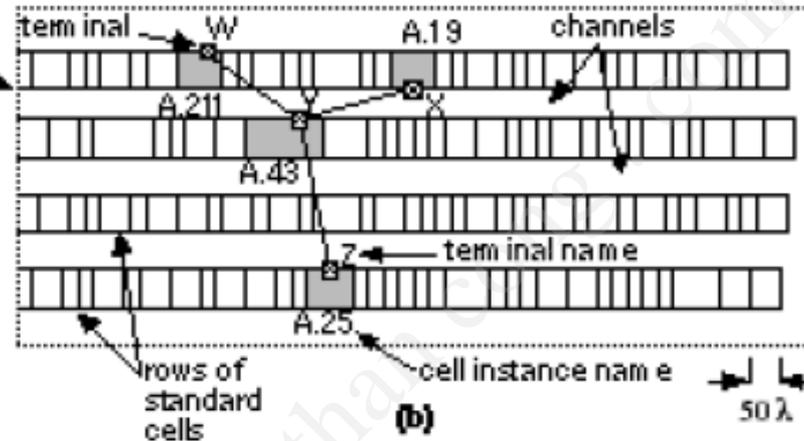
Placement

- Objectives
  - Guarantee the router can complete the routing step
  - Minimize all the critical net delays
  - Make the chip as dense as possible
  - Minimize power dissipation
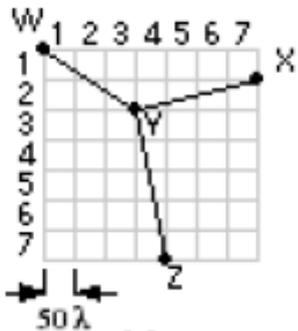 - Minimize cross talk between signals

Placement Example

(a)

(b) expanded view of part of flexible block A

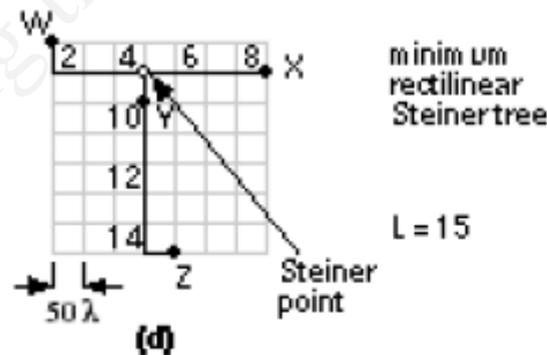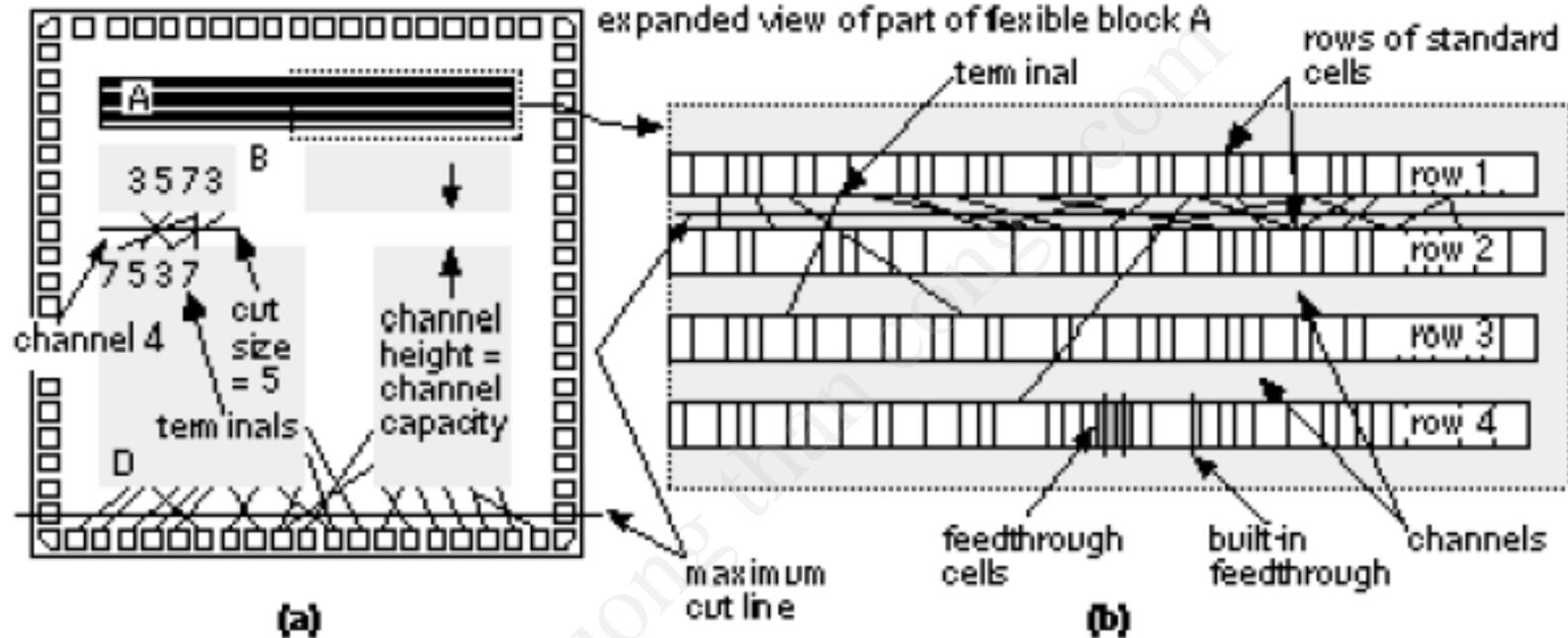Four rows of standard cells

(c) The problem for the net (W, X, Y, Z)

(d) The minimum rectilinear Steiner tree using Manhattan routing

Measurement of Congestion

Measurement of congestion   A expanded view of flexible block A

Placement Process

- Setup placement options
- Auto place
- Congestion-Driven
- Timing-Driven
- Analyze congestion
- Analyze timing

5.3 Routing

- **Global Routing:** determines the channels to be used for each interconnect
  - Minimize the total interconnect length
  - Maximize the probability that the detailed router can complete the routing
  - Minimize the critical path delay
- **Detail Routing:** decides the exact location and layers for each interconnect
  - Minimize the total interconnect length ad area
  - Minimize the number of layers changes that the connections have to make
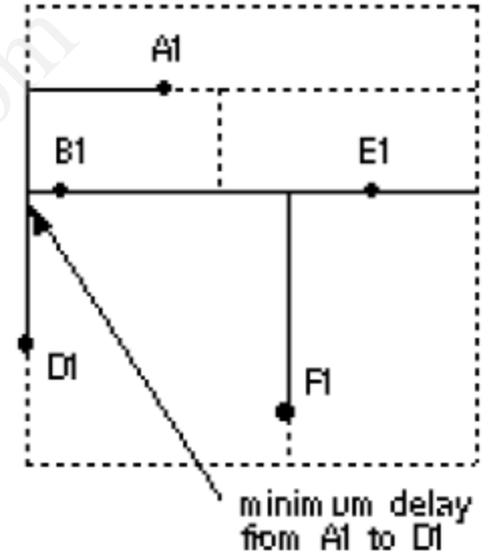 - Minimize the delay of critical paths
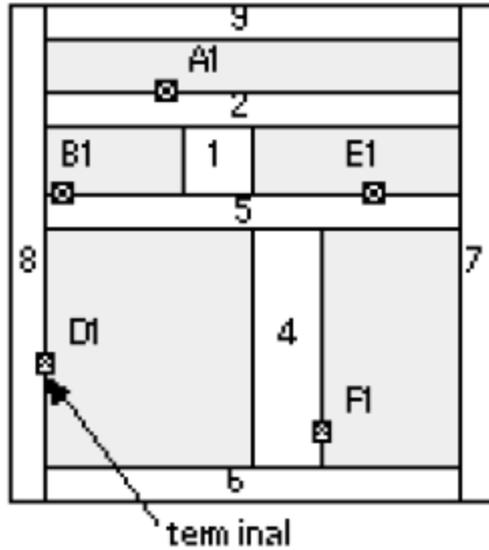
(a)

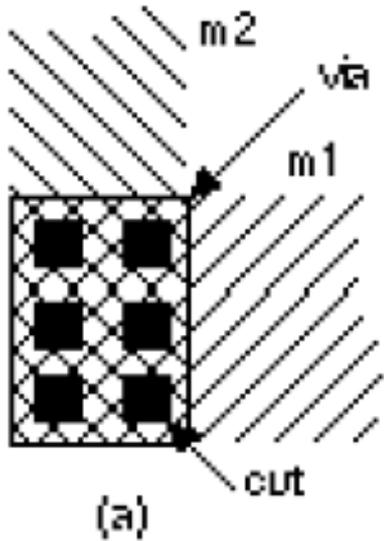A cell-based ASIC showing a single net with a fanout of four
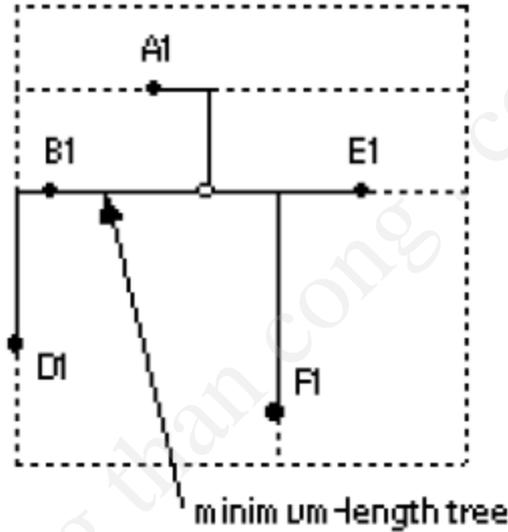
(b)

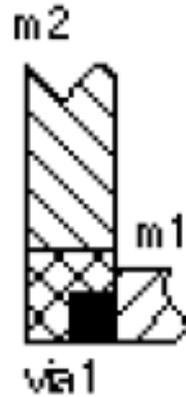Terminals are projected to center of the nearest channel

(c)

The minimum-length tree

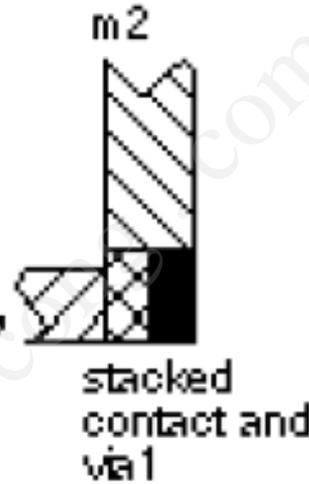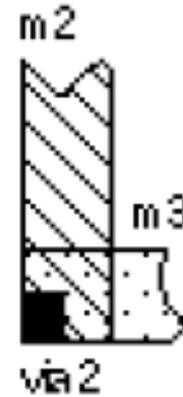# Via and Contact in Detail Routing

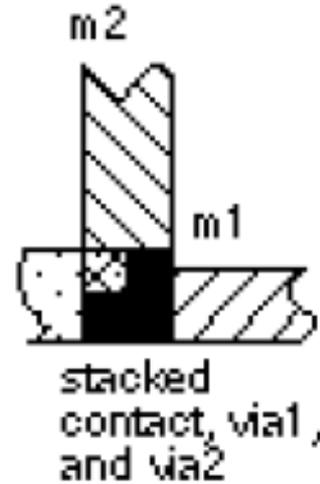(a) A large via

(b) A via 1

(c) A contact from m1

(d) A via 1 placed over a contact

(e) A via 2

(f) A via 2 stacked over a via 1

Routing Process

- Setup up for routing

- Global route, track assign, detail route

- Route clock

- Route signal

- Optimize post route

- Report timing

- Report DRC/LVS

Physical Design Tools

- ## Ploorplanning/placement/routing tools:
  - ### Design compiler:
    - IC Compiler: for netlist-to-GDSII
    - IC Compiler-XP: for the process 130nm and above
    - IC Compiler-PC: for netlist-to-clock-tree-synthesis
    - IC Compiler-DP: for design planning

- ## Timing analysis tool
  - ### Prime Time
    - Post-layout timing verification

IC Design Compiler Flow