Course : ASIC & IP Core Design
Instructor : Dr. Truong Quang Vinh

Homework 1

(Deadline 15/3/2014)

Design an IP core by using Verilog/VHDL, select **two IP cores** of the following list:

- Adder
- Subtractor
- Multiplier
- Divider

Requirements:

- Design for reuse
  - Apply coding guidelines
- Configurable parameters
  - Width of input data
  - Reset level
  - Unsigned / signed number
- Required deliverable set
  - Behavior model code
  - RTL code
  - Testbench