BÁO CÁO THÍ NGHIỆM KĨ THUẬT SỐ

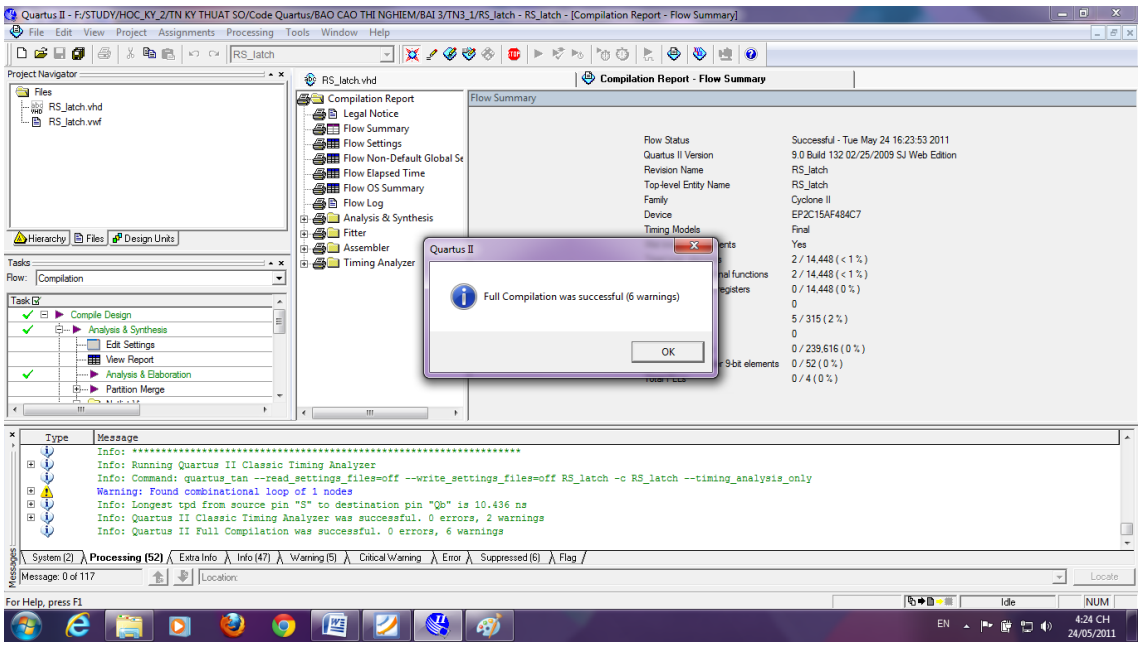
BÀI THÍ NGHIỆM 3

I. Thí nghiệm 3.1:

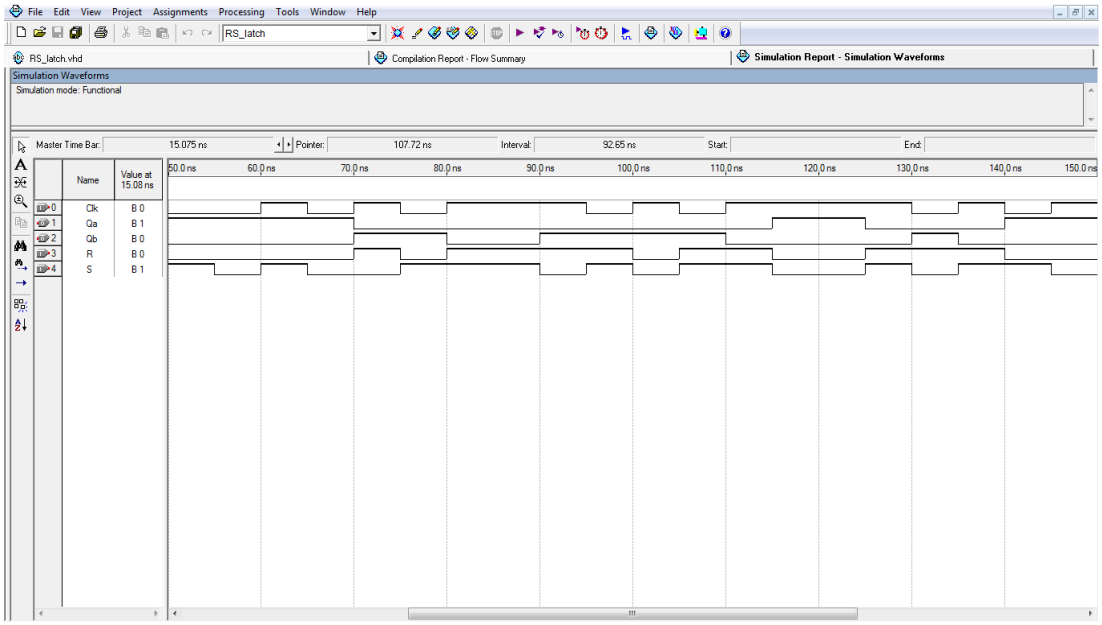
1. Code:

```
library ieee;
use ieee.std_logic_1164.all;
entity RS_latch is
port (
        R, S, Clk : in std_logic;
        Qa, Qb: out std_logic
        );
end RS_latch;
architecture dataflow of RS_latch is
signal R_g, S_g, Qa_g, Qb_g : std_logic;
begin
        R_g <= R and Clk;
        S_g <= S and Clk;
        Qa_g <= Qb_g nor R_g;
        Qb_g <= Qa_g nor S_g;
        Qa <= Qa_g;
        Qb <= Qb_g;
end dataflow;
```

2. Biên dịch:



3. Mô phỏng:

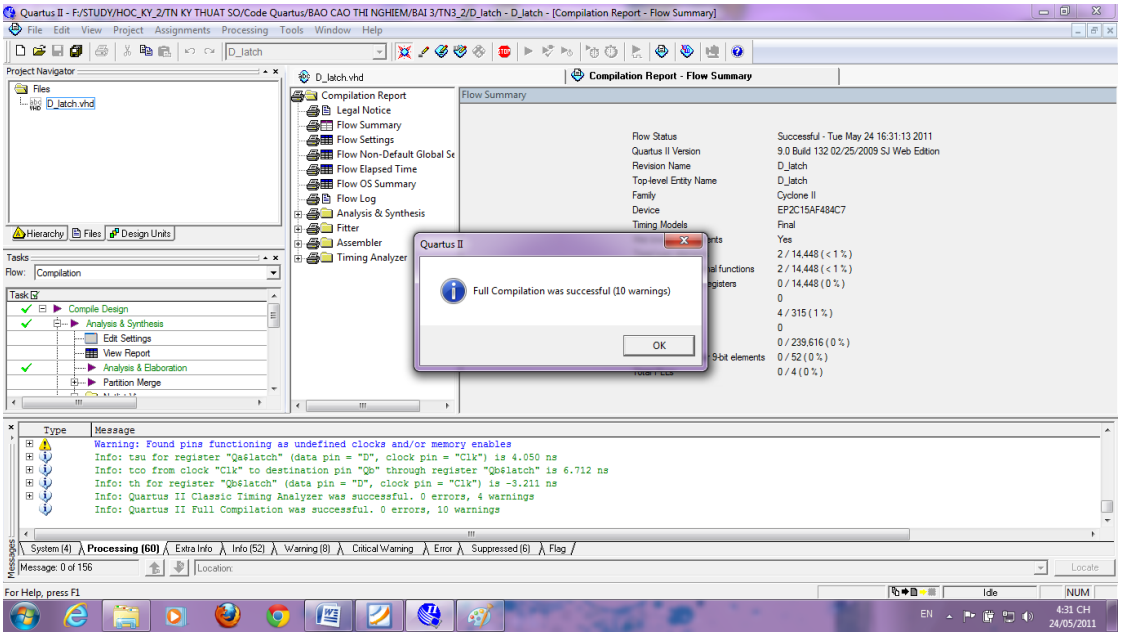


II. Thí nghiệm 3.2:

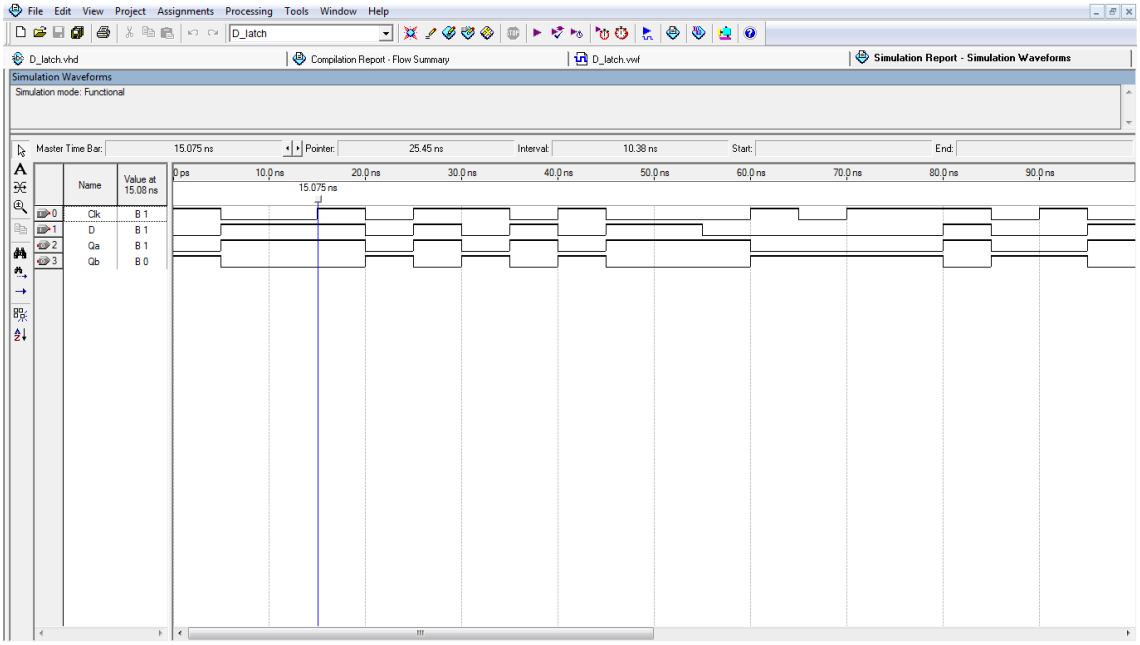
1. Code:

```
library ieee;
use ieee.std_logic_1164.all;
entity D_latch is
port (
        D, Clk :in std_logic;
        Qa, Qb: out std_logic
        );
end D_latch;
architecture behavior of D_latch is
begin
        process (D, Clk)
        begin
                if (Clk = '1') then
                        Qa <= D;
                        Qb <= not D;
                end if;
        end process;
end behavior;
```

2. Biên dịch:



3. Mô phỏng:



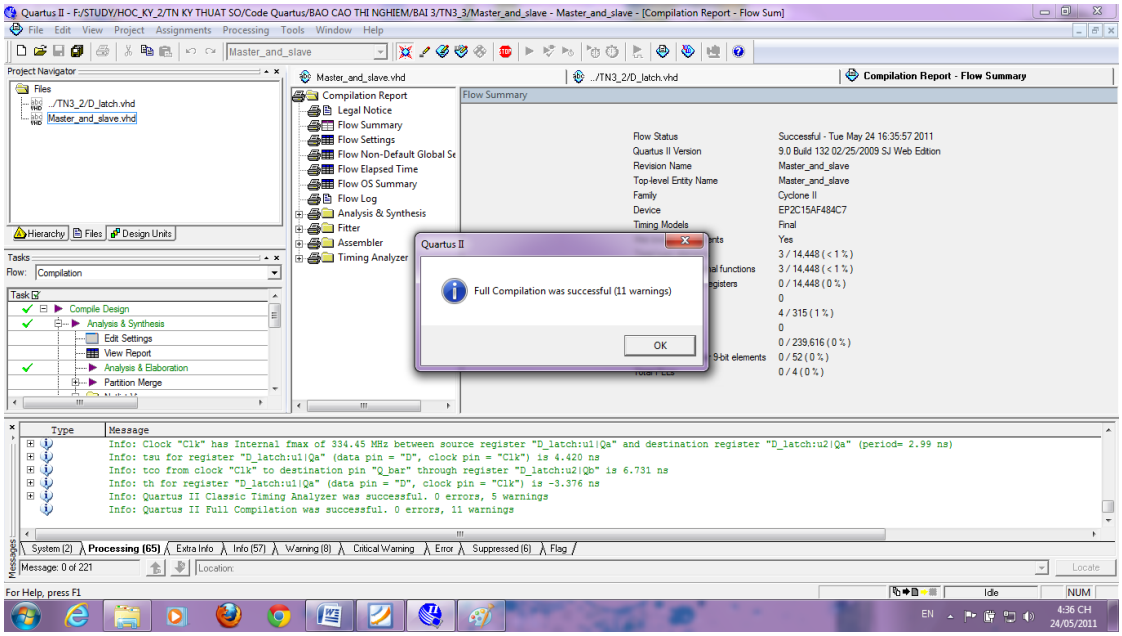
III. Thí nghiệm 3.3:

1. Code:

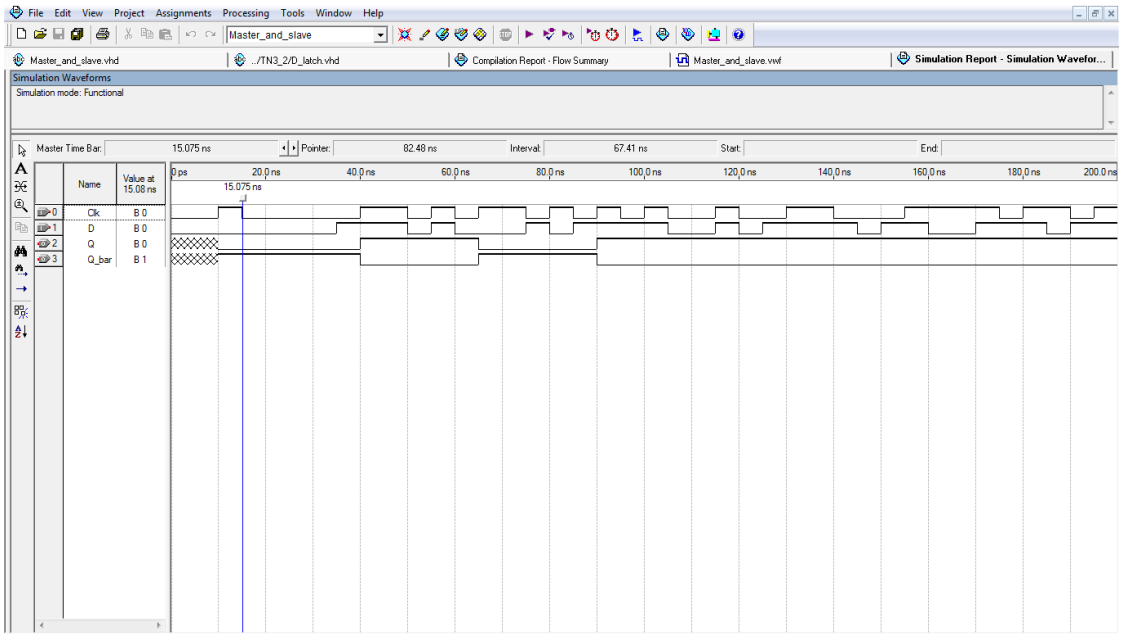
```
library ieee;
use ieee.std_logic_1164.all;
entity Master_and_slave is
port (
        D, Clk: in std_logic;
        Q, Q_bar: out std_logic
        );
end Master_and_slave;
architecture structrural of Master_and_slave is
signal Q_m , Clk_bar: std_logic;
```

```
component D_latch
port (
        D, Clk :in std_logic;
        Qa, Qb: out std_logic
        );
end component;
begin
        Clk_bar <= not Clk;
        u1: D_latch port map ( D, Clk_bar,Q_m);
        u2: D_latch port map (Q_m, Clk, Q, Q_bar);
end structrural;
```

2. Biên dịch:



3. Mô phỏng:

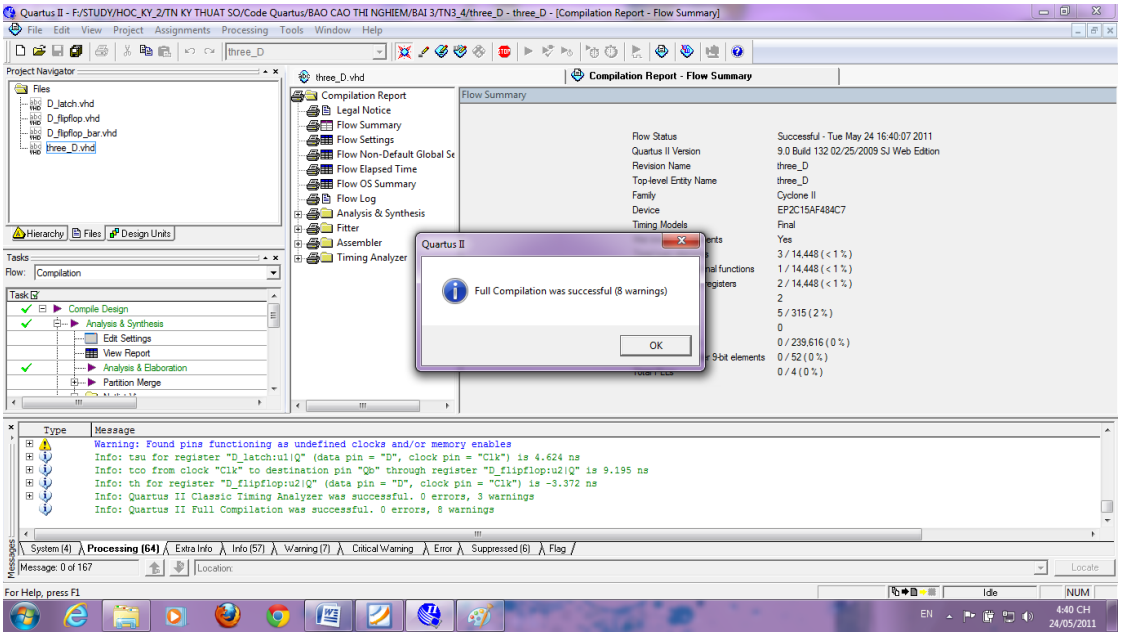


IV. Thí nghiệm 3.4:

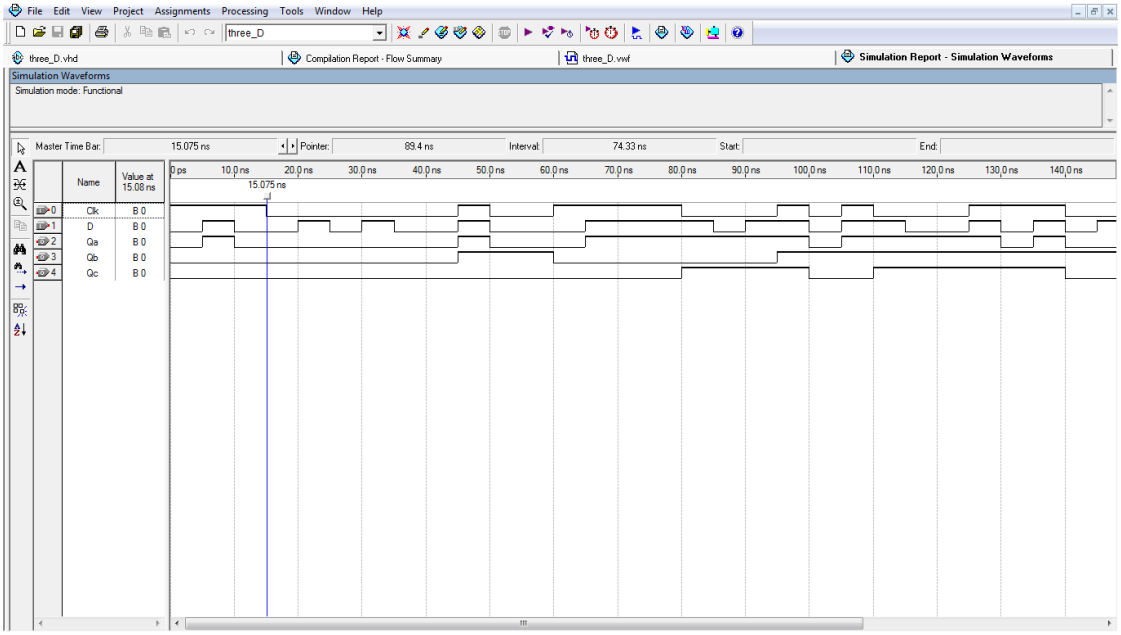
1. Code:

```
library ieee;
use ieee.std_logic_1164.all;
entity three_D is
port (
        D, Clk : in std_logic;
        Qa, Qb, Qc: out std_logic
        );
end three_D;
architecture behavior of three_D is
component D_latch
port (
        D, Clk : in std_logic;
        Q: out std_logic
        );
end component;
component D_flipflop
port (
        D, Clk : in std_logic;
        Q: out std_logic
        );
end component;
component D_flipflop_bar is
port (
        D, Clk : in std_logic;
        Q: out std_logic
        );
end component;
begin
        u1: D_latch port map ( D, Clk, Qa);
        u2: D_flipflop port map ( D, Clk, Qb);
        u3: D_flipflop_bar port map ( D, Clk, Qc);
end behavior;
```

2. Biên dịch:


Quartus II - F:/STUDY/HOC_KY_2/TN KY THUAT SO/Code Quartus/BAO CAO THI NGHIEM/BAI 3/TN3_4/three_D - three_D - [Compilation Report - Flow Summary]
File Edit View Project Assignments Processing Tools Window Help
Project Navigator
Files
D_latch.vhd
D_flipflop.vhd
D_flipflop_bar.vhd
three_D.vhd
Hierarchy Files Design Units
Tasks
Flow: Compilation
Task
Compile Design
Analysis & Synthesis
Edit Settings
View Report
Analysis & Elaboration
Partition Merge
three_D.vhd
Compilation Report - Flow Summary
Compilation Report
Legal Notice
Flow Summary
Flow Settings
Flow Non-Default Global Se
Flow Elapsed Time
Flow OS Summary
Flow Log
Analysis & Synthesis
Fitter
Assembler
Timing Analyzer
Flow Summary
Flow Status Successful - Tue May 24 16:40:07 2011
Quartus II Version 9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name three_D
Top-level Entity Name three_D
Family Cyclone II
Device EP2C15AF484C7
Timing Models Final
Yes
3 / 14,448 (< 1 %)
1 / 14,448 (< 1 %)
2 / 14,448 (< 1 %)
2
5 / 315 (2 %)
0
0 / 239,616 (0 %)
0 / 52 (0 %)
0 / 4 (0 %)
Quartus II
Full Compilation was successful (8 warnings)
OK
Type Message
Warning: Found pins functioning as undefined clocks and/or memory enables
Info: tsu for register "D_latch:u1|Q" (data pin = "D", clock pin = "Clk") is 4.624 ns
Info: tco from clock "Clk" to destination pin "Qb" through register "D_flipflop:u2|Q" is 9.195 ns
Info: th for register "D_flipflop:u2|Q" (data pin = "D", clock pin = "Clk") is -3.372 ns
Info: Quartus II Classic Timing Analyzer was successful. 0 errors, 3 warnings
Info: Quartus II Full Compilation was successful. 0 errors, 8 warnings
System (4) Processing (64) Extra Info Info (57) Warning (7) Critical Warning Error Suppressed (6) Flag
Message: 0 of 167
Location:
Locate
For Help, press F1
Idle
NUM
EN
4:40 CH
24/05/2011

3. Mô phỏng:


File Edit View Project Assignments Processing Tools Window Help
three_D
three_D.vhd
Compilation Report - Flow Summary
three_D.vwf
Simulation Report - Simulation Waveforms
Simulation Waveforms
Simulation mode: Functional
Master Time Bar: 15.075 ns
Pointer: 89.4 ns
Interval: 74.33 ns
Start:
End:
Name
Value at 15.08 ns
0 ps 10.0 ns 20.0 ns 30.0 ns 40.0 ns 50.0 ns 60.0 ns 70.0 ns 80.0 ns 90.0 ns 100.0 ns 110.0 ns 120.0 ns 130.0 ns 140.0 ns
15.075 ns
0 Clk B 0
1 D B 0
2 Qa B 0
3 Qb B 0
4 Qc B 0