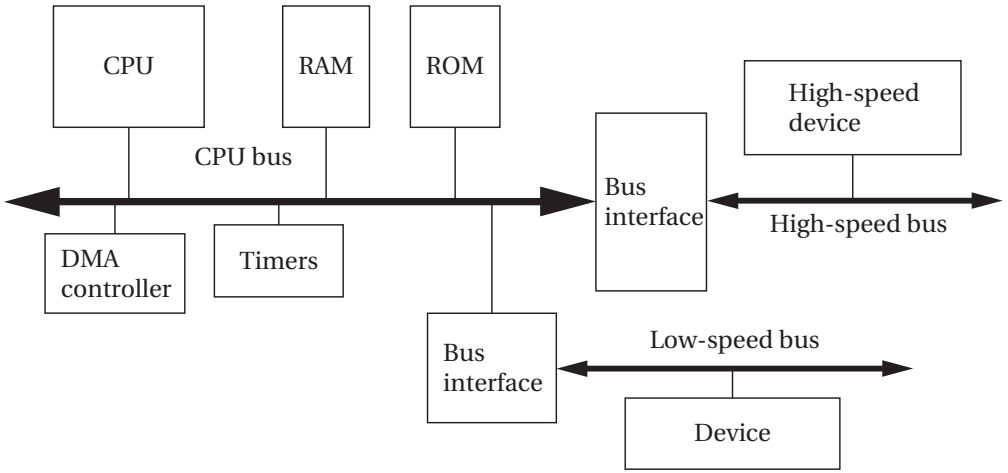
Computing Platforms

- Platform organization.
- Busses.
- Memory devices.

Computing platform architecture



- DMA provides direct memory access.
- Timers used by OS, devices.
- Multiple busses connect CPU, memory to devices.

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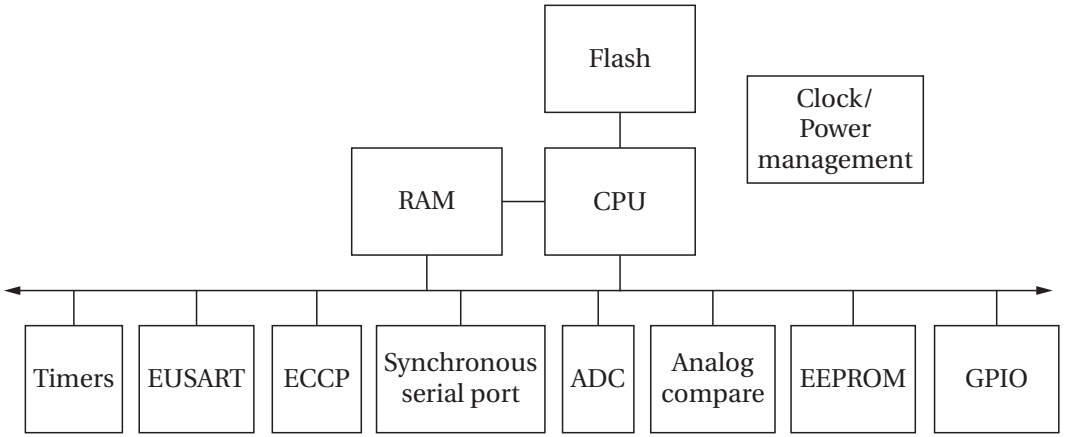
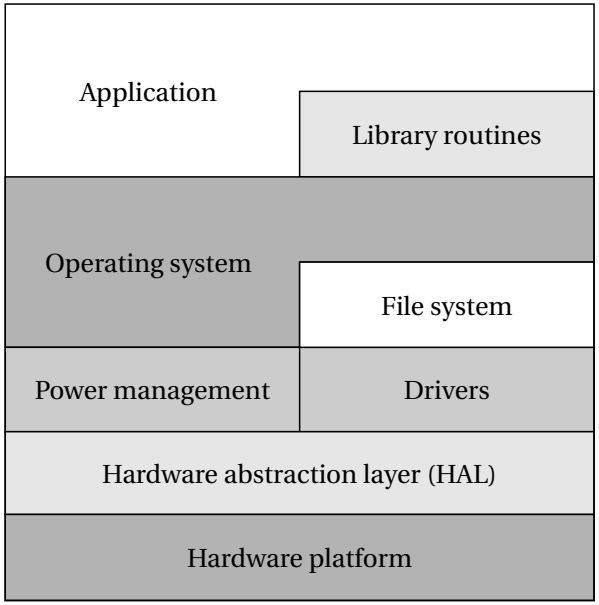


- Harvard architecture---flash memory separately programmed.
- Multiple I/O devices.

Platform software

- Platform software provides core functions, utilities.
- Low-level functions depend on architecture---interrupt vectors, etc.



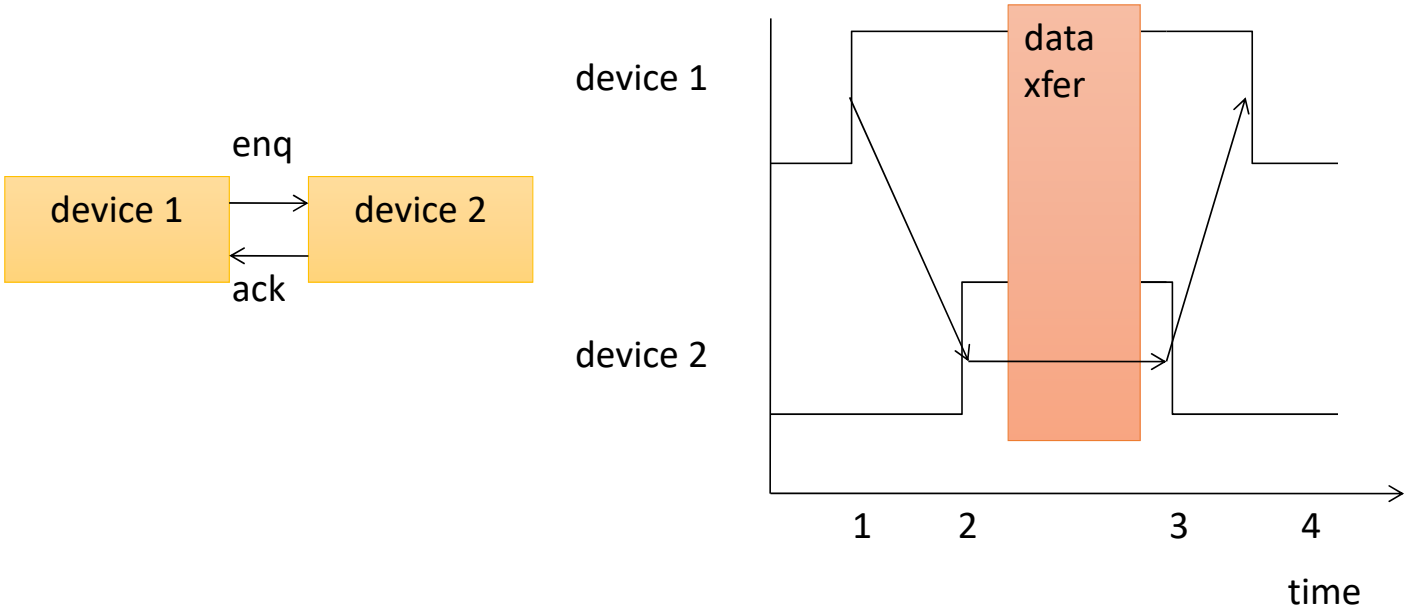
CPU buses

- Bus allows CPU, memory, devices to communicate.
  - Shared communication medium.
- A bus is:
  - A set of wires.
  - A communications protocol.

Bus protocols

- Bus protocol determines how devices communicate.
- Devices on the bus go through sequences of states.
  - Protocols are specified by state machines, one state machine per actor in the protocol.
- May contain asynchronous logic behavior.

Four-cycle handshake

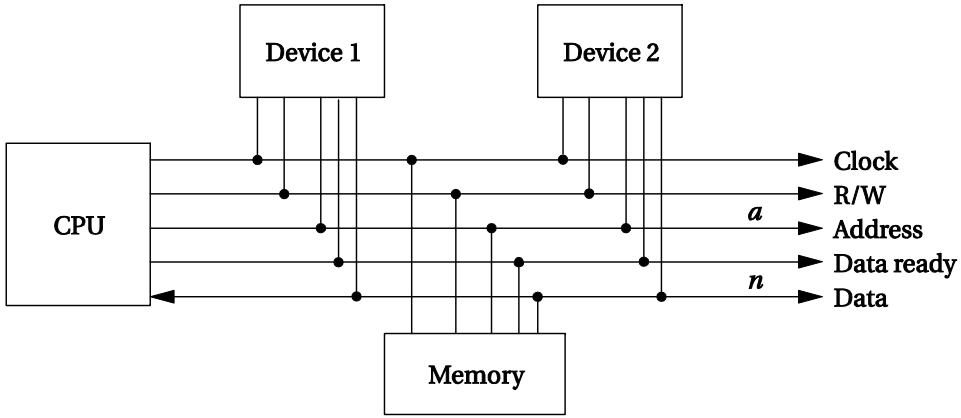


Four-cycle handshake, cont'd.

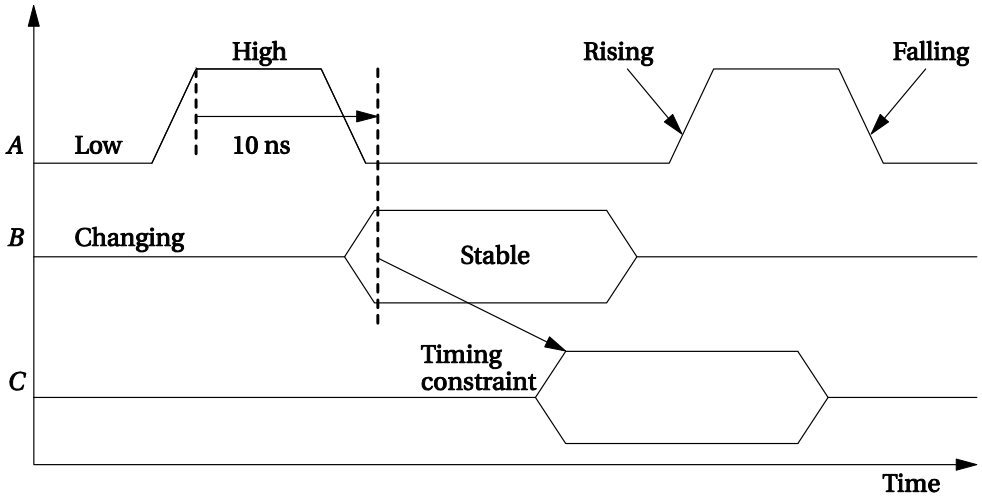
1. Device 1 raises enq.
2. Device 2 responds with ack.
3. Device 2 lowers ack once it has finished.
4. Device 1 lowers enq.

Microprocessor busses

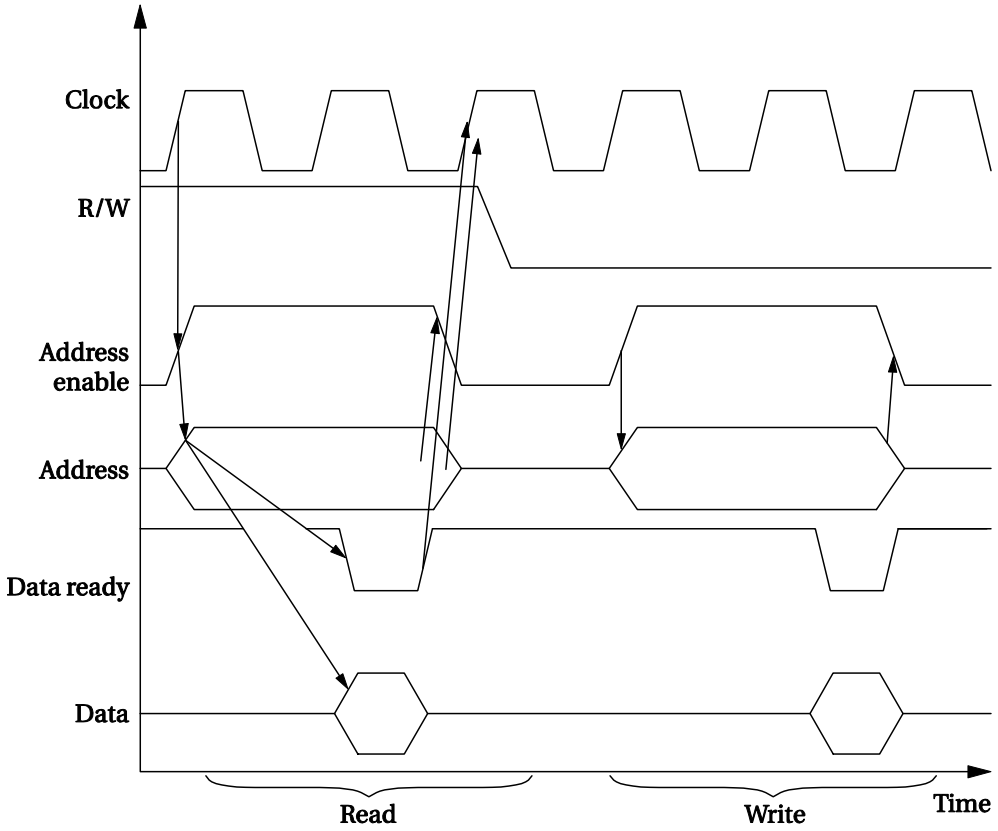
- Clock provides synchronization.
- R/W is true when reading (R/W' is false when reading).
- Address is a-bit bundle of address lines.
- Data is n-bit bundle of data lines.
- Data ready signals when n-bit data is ready.



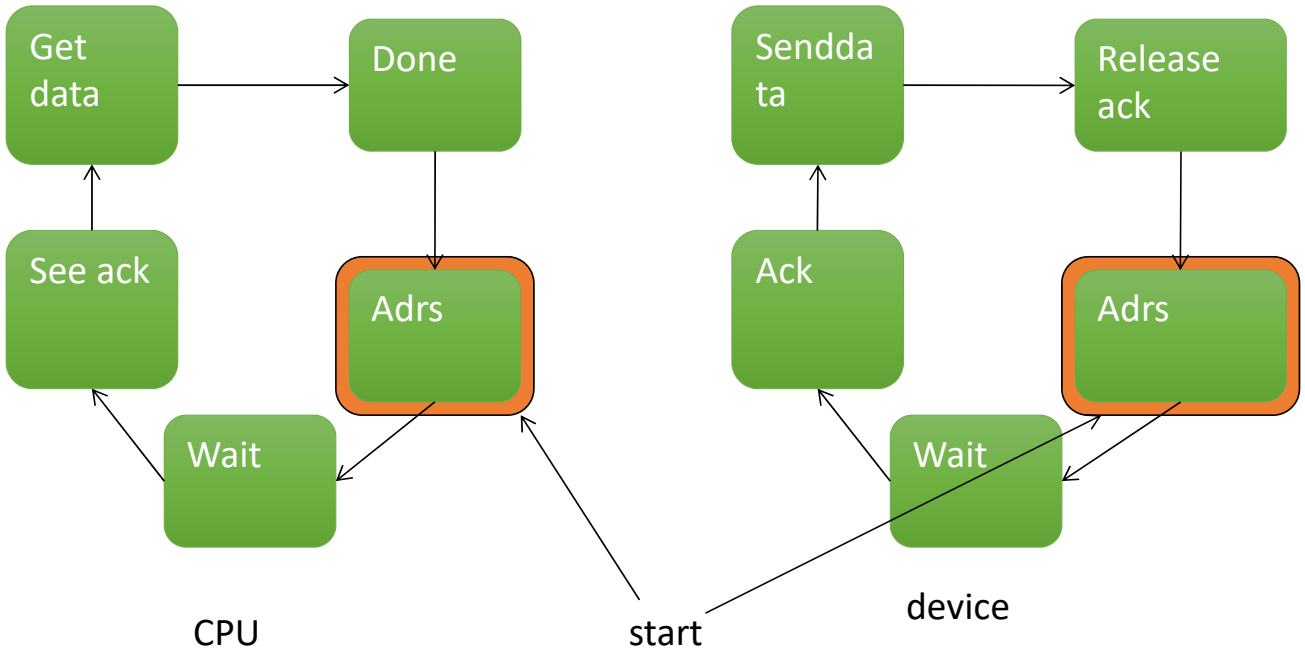
Timing diagrams



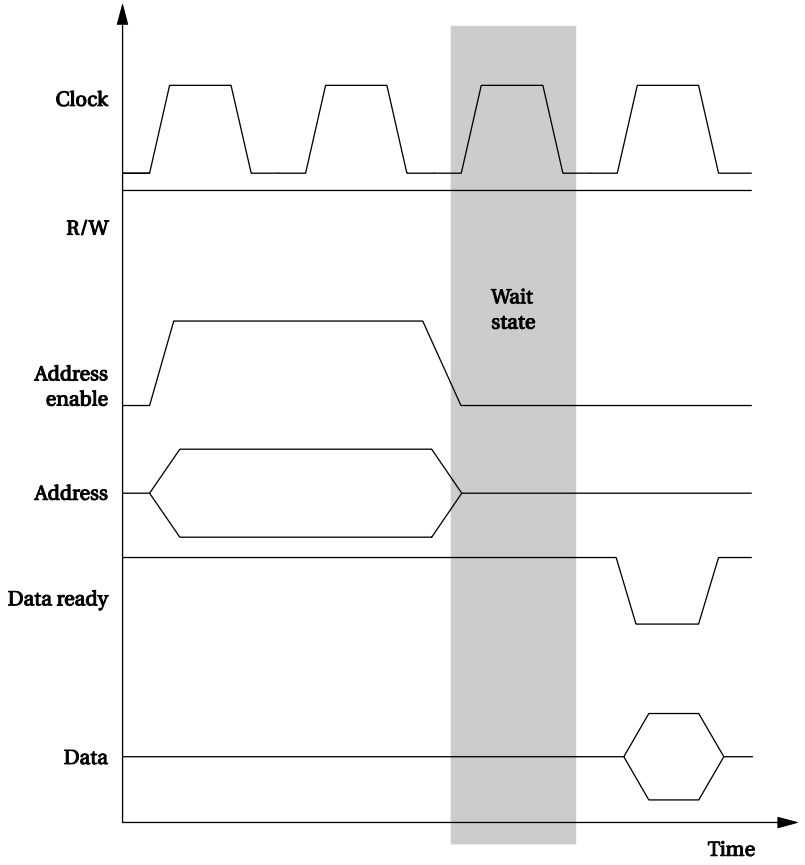
Bus read



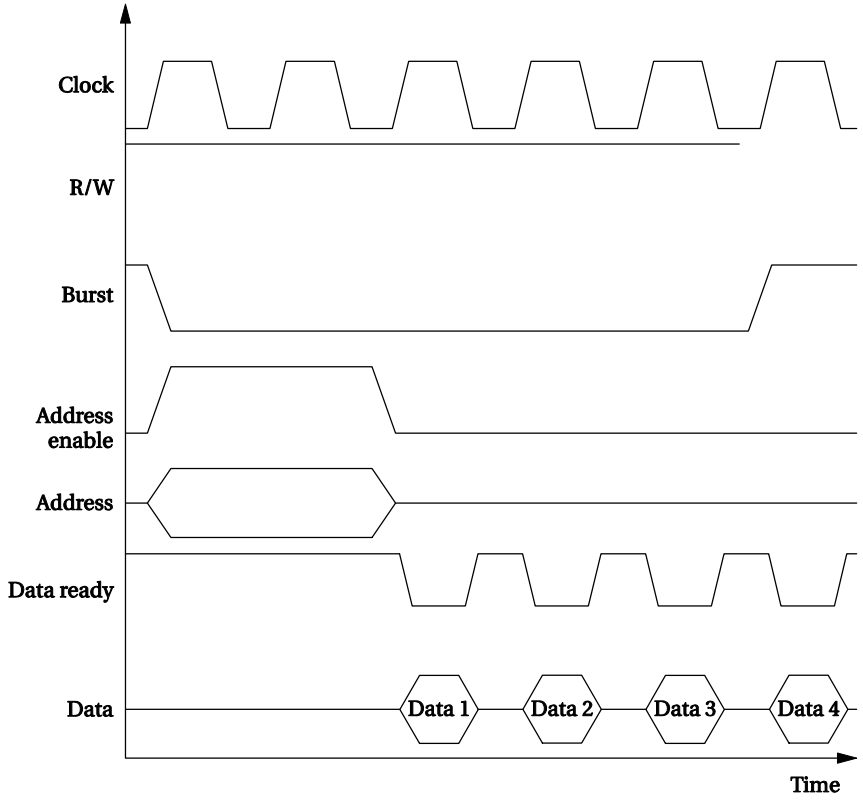
State diagrams for bus read



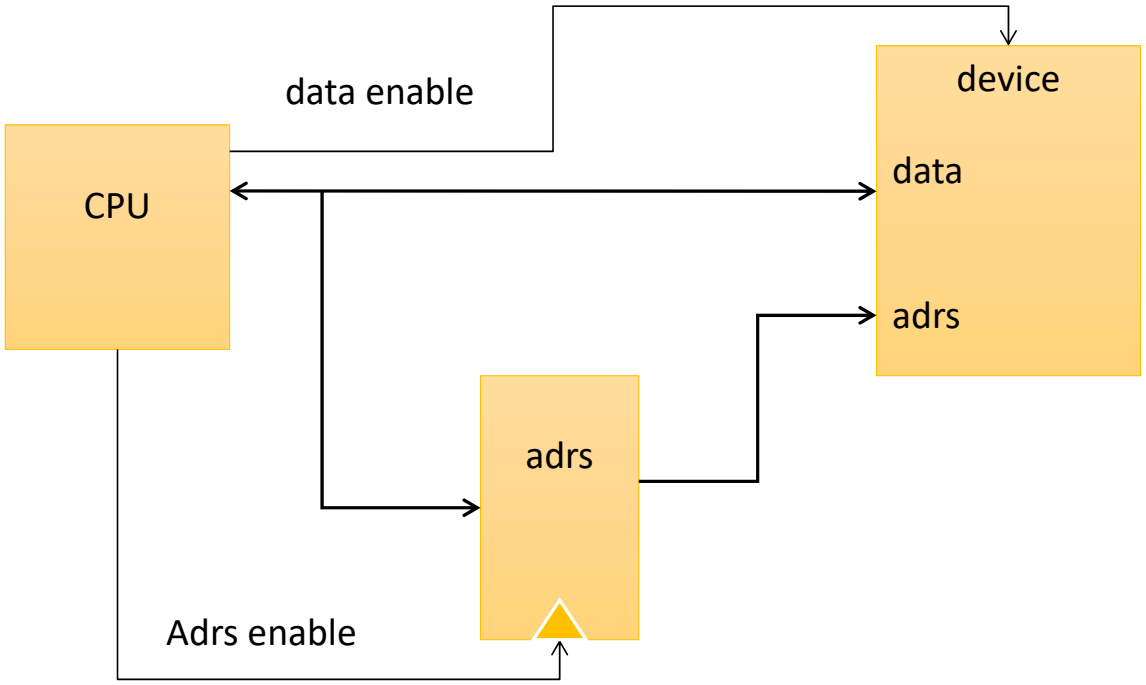
Bus wait state



Bus burst read

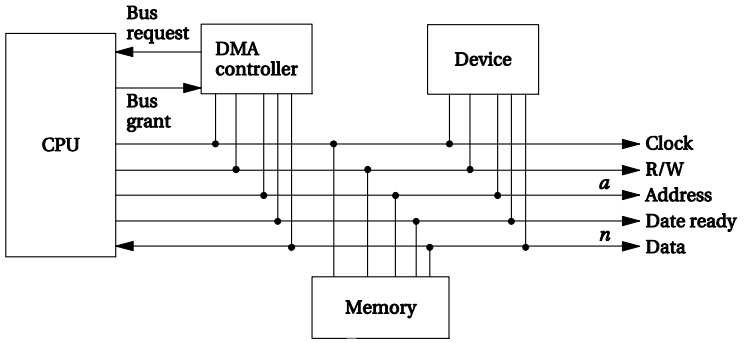


Bus multiplexing



DMA

- Direct memory access (DMA) performs data transfers without executing instructions.
  - CPU sets up transfer.
  - DMA engine fetches, writes.
- DMA controller is a separate unit.

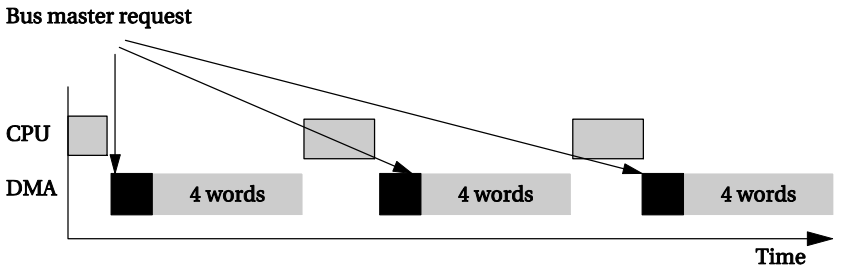


Bus mastership

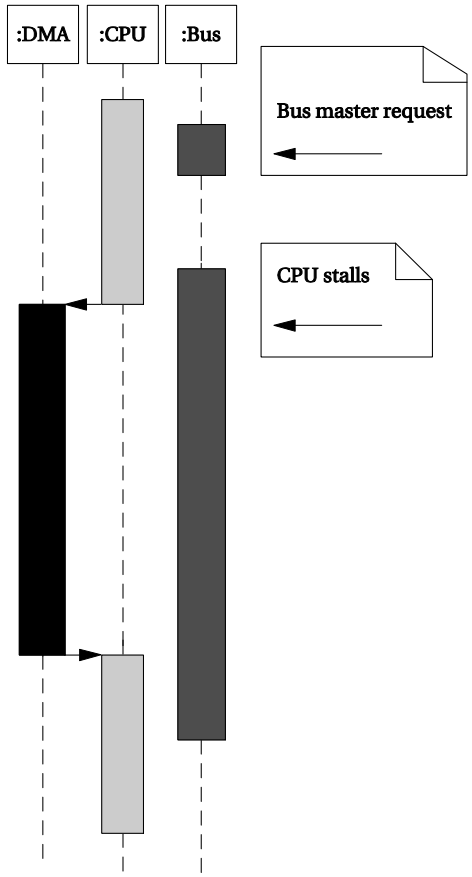
- By default, CPU is bus master and initiates transfers.
- DMA must become bus master to perform its work.
  - CPU can’t use bus while DMA operates.
- Bus mastership protocol:
  - Bus request.
  - Bus grant.

DMA operation

- CPU sets DMA registers for start address, length.
- DMA status register controls the unit.
- Once DMA is bus master, it transfers automatically.
  - May run continuously until complete.
  - May use every n^{th} bus cycle.

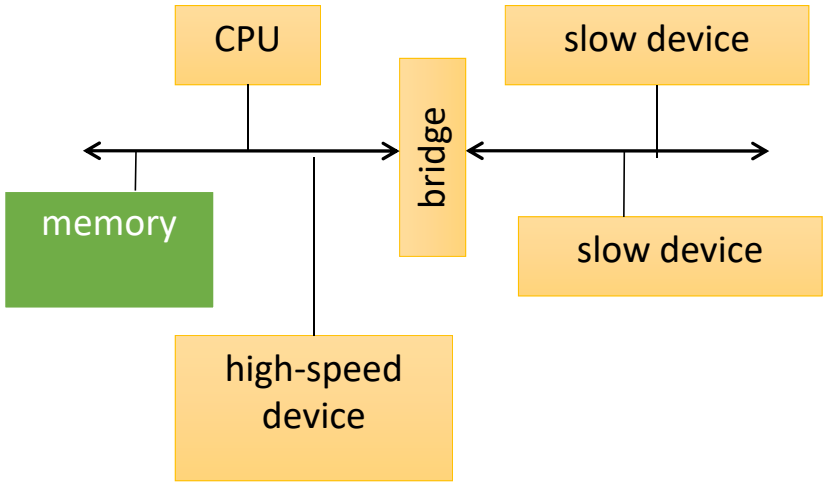


Bus transfer sequence diagram

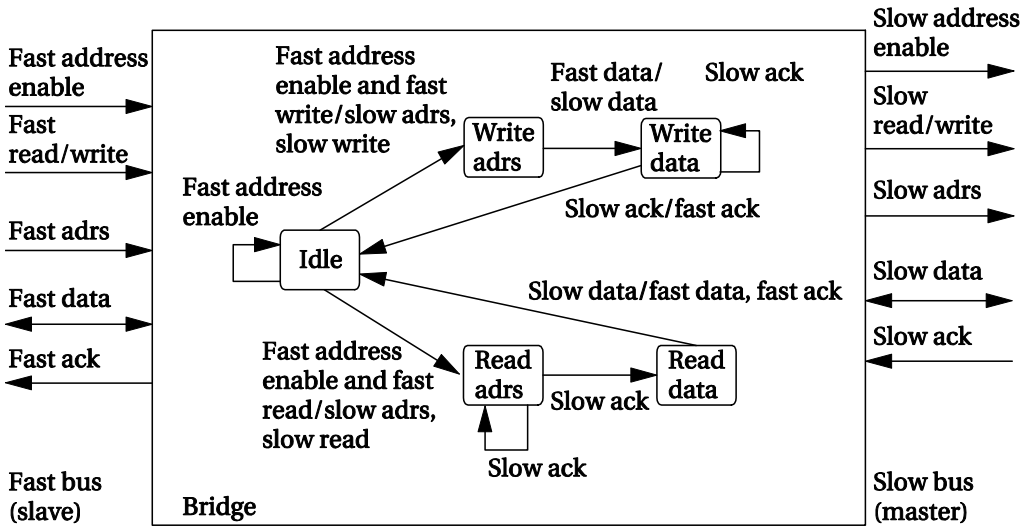


System bus configurations

- Multiple busses allow parallelism:
  - Slow devices on one bus.
  - Fast devices on separate bus.
- A bridge connects two busses.

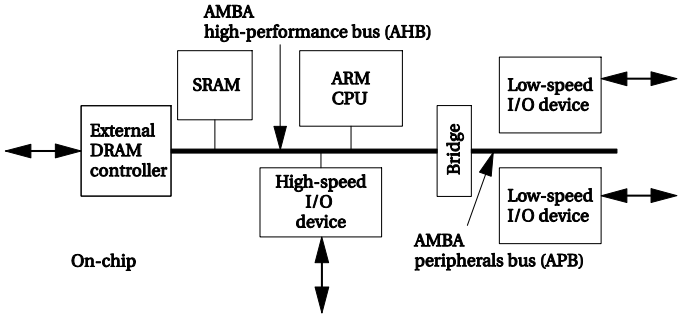


Bridge state diagram



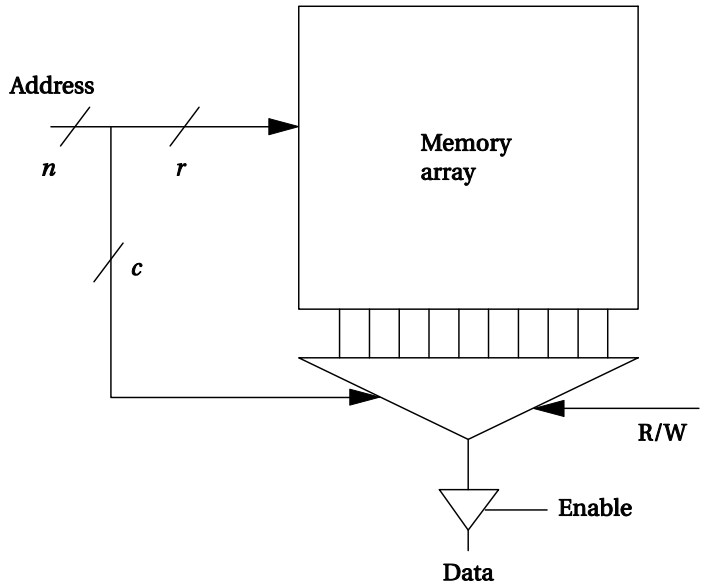
ARM AMBA bus

- Two varieties:
  - AHB is high-performance.
  - APB is lower-speed, lower cost.
- AHB supports pipelining, burst transfers, split transactions, multiple bus masters.
- All devices are slaves on APB.



Memory components

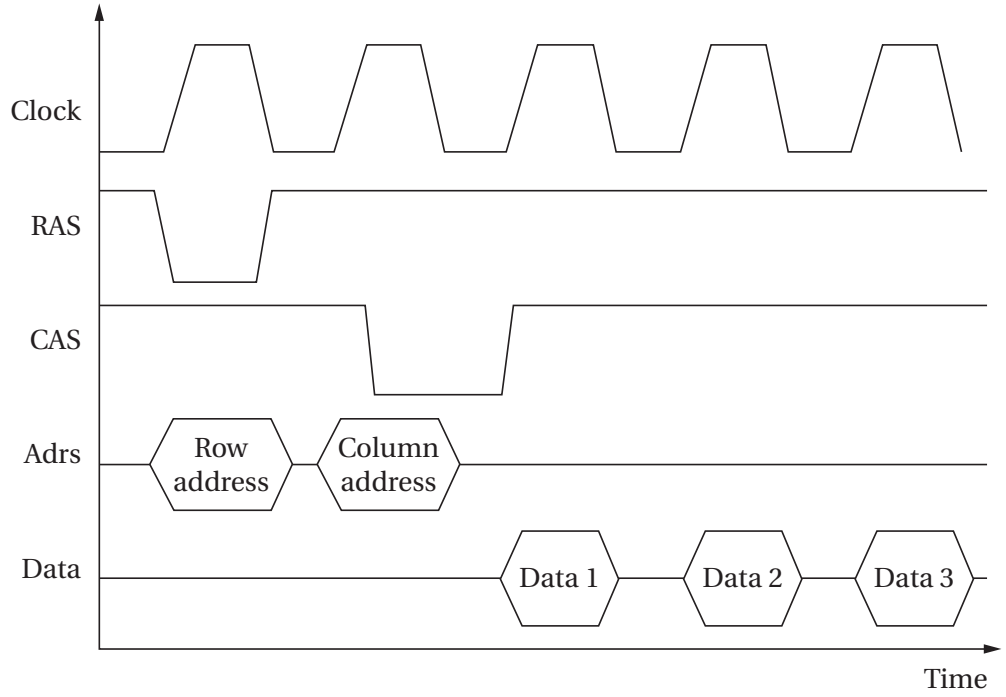
- Several different types of memory:
  - DRAM.
  - SRAM.
  - Flash.
- Each type of memory comes in varying:
  - Capacities.
  - Widths.



Random-access memory

- Dynamic RAM is dense, requires refresh.
  - SDRAM: synchronous DRAM.
  - EDO DRAM: extended data out.
  - FPM DRAM: fast page mode.
  - DDR DRAM: double-data rate.
- Static RAM is faster, less dense, consumes more power.

SDRAM read operation

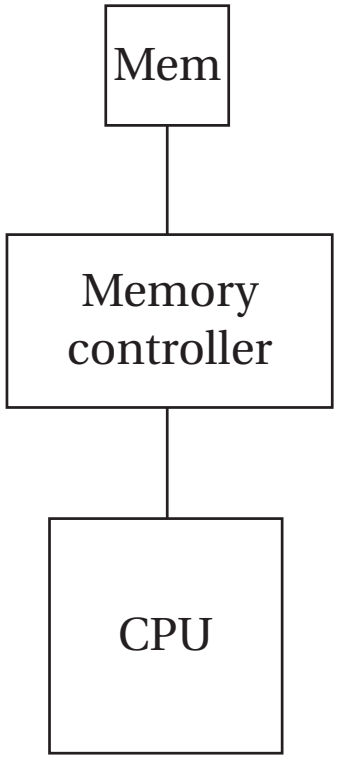


Memory packaging

- SIMM: single in-line memory module.
- DIMM: dual in-ilen memory module.

Memory systems and memory controllers

- Memory has complex internal organization.
- Memory controller hides details of memory interface, schedules transfers to maximize performance.



Channels and banks

- Channels provide separate connections to parts of memory.
- Banks are separate memory arrays.